DDR 7:1 Module

User Guide

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
GDDR	Generic Double Data Rate
GUI	Graphical User Interface
I/O	Input/Output
RTL	Register Transfer Level

1. Introduction

The Lattice Semiconductor Generic Double Data Rate 7:1 Input/Output (GDDR 7:1 I/O) Module is designed to be used mainly for Flat-panel Display interface.

1.1. Features

Key features of the Generic Double Data Rate 7:1 Input/Output Module include:

- Receive and Transmit Interface up to 945 Mbps
- 1-bit to 16-bit data bus width
- Optional bit word alignment and data delay control (for Receive Interface only)
- Optional use of external PLL (for LFMXO5-25 device on Receive Interface only)

1.2. Conventions

1.2.1. Nomenclature

The nomenclature used in this document is based on Verilog HDL.

1.2.2. Signal Names

Signal names that end with:

- _*n* are active low
- _*i* are input signals
- _*o* are output signals
- _*io* are bi-directional input/output signals

2. Functional Description

2.1. Overview

GDDR 7:1 I/O Module is a specific case of Generic DDR I/O Module designed to be used for Flat-panel Display interface.

Table 2.1 provides a summary of GDDR 7:1 I/O Interfaces.

Table 2.1. Available GDDR 7:1 I/O Module Interfaces

Feature	Description	Comments
GDDRX71_RX.ECLK	Generic DDR 7:1 Receive Interface	Supports bypassed and dynamic data path delay when BW_ALIGN is enabled. Optional BW_ALIGN support soft logic. Required GDDR_SYNC support soft logic.
GDDRX71_TX.ECLK	Generic DDR 7:1 Transmit Interface	Supports bypassed and dynamic data path delay. Required GDDR_SYNC support soft logic.

Notes:

- G – Generic
- _RX – Receive interface
- _TX – Transmit interface
- ECLK – Uses edge clock clocking resource

The following Table 2.2 are the Summary of the Soft Logic

The following Soft Logic Modules are utilized by the Generic DDR 7:1 IP for synchronization and alignment. The GDDR_SYNC module is used by all configurations of the IP and automatically included when generating the IP. The module BW_ALIGN, on the other hand is optional but is only available when the interface of the IP is Receive.

Table 2.2. Summary of the Soft Logic

Module	Description
GDDR_SYNC	Needed to tolerate large skew between stop and reset input.
BW_ALIGN	This soft IP is used to perform bit and word alignment using PLL's dynamic phase shift interface and dynamic DELAY adjustment.

Figure 2.1 presents top-level diagram describing GDDR 7:1 I/O Module.

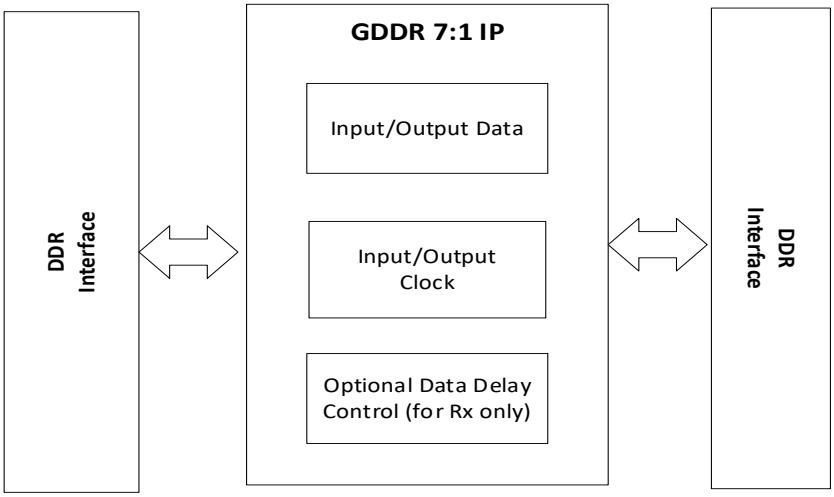

Figure 2.1. GDDR 7:1 I/O Soft IP Top-level Block Diagram

2.2. Functional Diagrams

GDDRX71_RX.ECLK

This is a specialized receive interface (called 7:1 LVDS, FPD-Link, or OpenLDI) using 1:7 gearing and ECLK. The input clock coming in is multiplied 3.5X using a PLL. The multiplied clock is used to capture the data at the receive IDDR71 module. Internal PLL is available on all devices. Optional use of external PLL when using LFMXO5-25 device is also available.

Figure 2.2 shows the GDDR 7:1 I/O Receive Interface only with Bit and Word Alignment, and Data Delay Control options disabled.

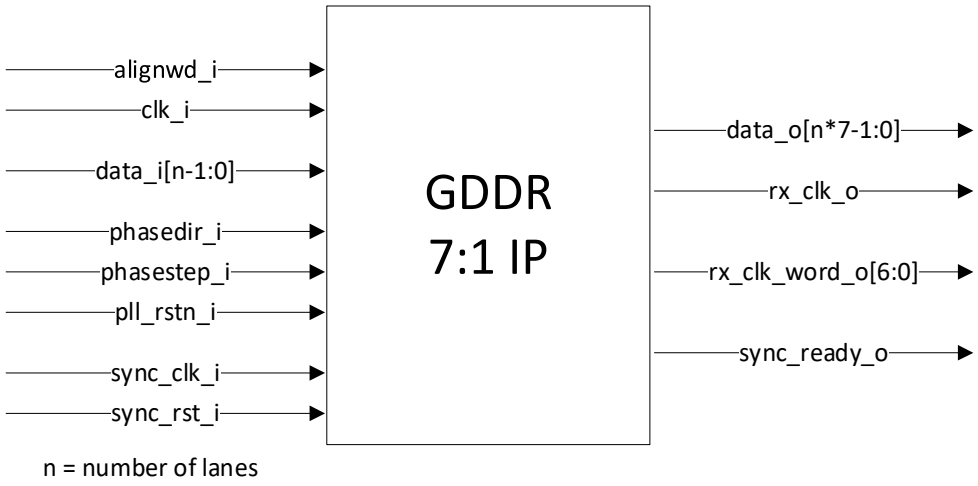

Figure 2.2. GDDRX71_RX.ECLK with GDDR_SYNC and Internal GPLL (without BW_ALIGN) Block Diagram

Described are the components of this configuration:

- PLL IP, which is automatically instantiated on this IP configuration, generates the edge clock from *clk_i*. The frequency of the generated edge clock of clk_i is 3.5x clk_i, This has a dedicated reset input signal, *pll_rstn_i*. This IP configuration provides you the control over clock phase shifting through the *phasedir_i* and *phasestep_i* signals. The value of phasedir_i dictates whether to delay or advance the phase of the output clock; 0 to delay the phase, 1 to advance. To activate these changes in the output clock dictated by phasedir_i, phasestep_i should be asserted.
- Clock IP components provides edge clock alignment. It also derives the slow clock, *rx_clk_o*, from the edge clock divided by 3.5 to support the gearing data ratio. The divided clock is available externally, but its frequency is similar to clk_i. The only difference between rx_clk_o and clk_i is that rx_clk_o is aligned to the edge clock.
- DDR Clock IP component generates the receiver clock word as parallel output.
- DDR Data IP component captures the input data. The edge clock is also the clock used to capture data.
- GDDR_SYNC Soft IP logic performs sequence to synchronize all the resets of the IP components after PLL lock is achieved. The synchronization happens before *RX* operation starts. When done, it asserts *sync_ready_o* signal to indicate that an operation can already be started. This component has its own clock input, sync_clk_i and reset input, *sync_rst_i*.

Figure 2.3 show receive interface type block diagram and interface with external PLL.

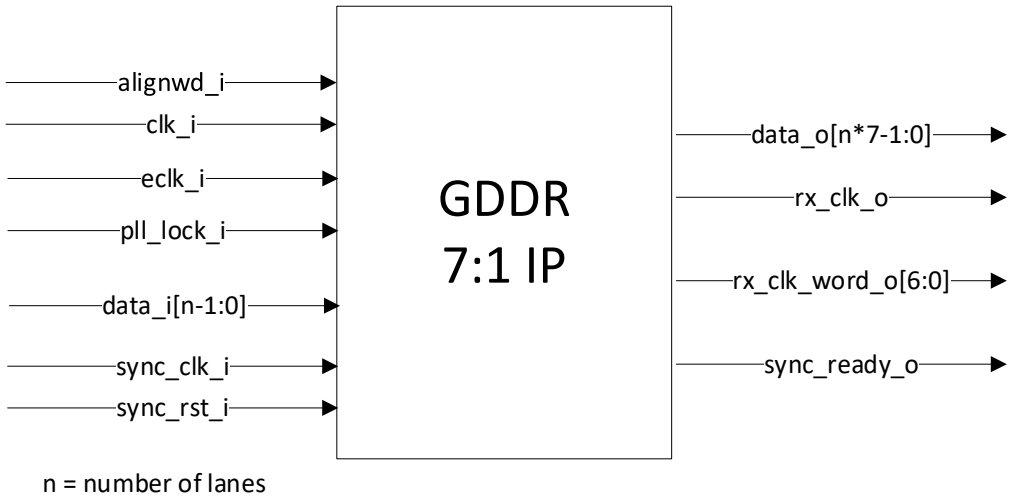

Figure 2.3. GDDRX71_RX.ECLK with GDDR_SYNC and External PLL Enabled Block Diagram

Described are the components of this configuration:

- When *External PLL* is enabled, the external PLL will generate from one of its clock outputs the edge clock to be used for this IP configuration. The PLL lock output is also passed to this IP configuration to signify the GDDR SYNC module to start the clock and reset synchronization.
- Clock IP components provides edge clock alignment. It also derives the slow clock, *rx_clk_o*, from the edge clock divided by 3.5 to support the gearing data ratio. The divided clock is available externally, but its frequency is the similar to clk_i. The only difference between rx_clk_o and clk_i is that rx_clk_o is aligned to the edge clock.DDR Clock IP component generates the receiver clock word as parallel output.
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Figure 2.4 show receive interface type with bit and word alignment block diagram and interface with internal PLL.

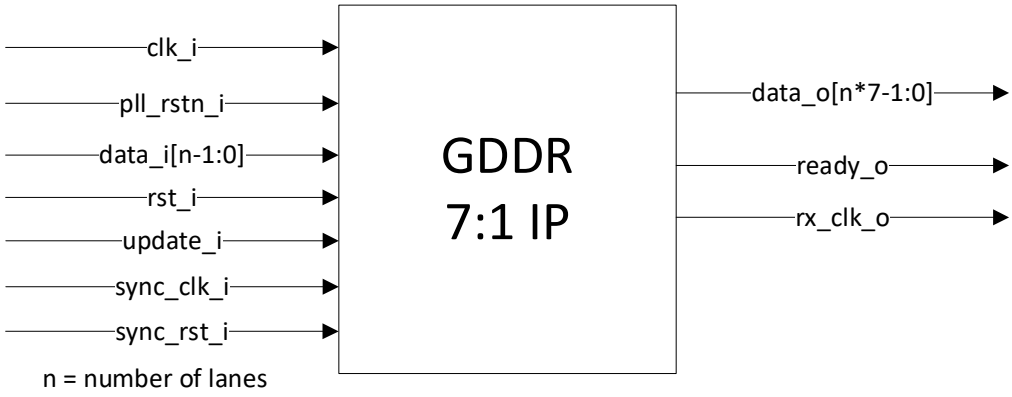

Figure 2.4. GDDRX71_RX.ECLK with GDDR_SYNC, Internal GPLL and BW_ALIGN Block Diagram

When Bit and Word Alignment feature is enabled, the BW_ALIGN Soft IP logic is added on the Receive interface IP components. This component will control the PLL dynamic clock phase shifting, and DDR components align input to perform the bit and word alignment respectively. Notice that on this configuration the phasedir_i, phasestep_i, and alignwd_i signals are no longer available on the interface. During bit alignment, PLL generated edge clock will be placed on the center of the valid window of the DDR clock and data words. Word alignment automatically controls the alignment on the DDR clock component by slipping the clock word until 7'h63 clock word value is achieved. Once synchronization and alignment are performed, ready_o signal will be asserted by the IP.

Figure 2.5 show receive interface type with bit and word alignment block and interface diagram with external PLL.

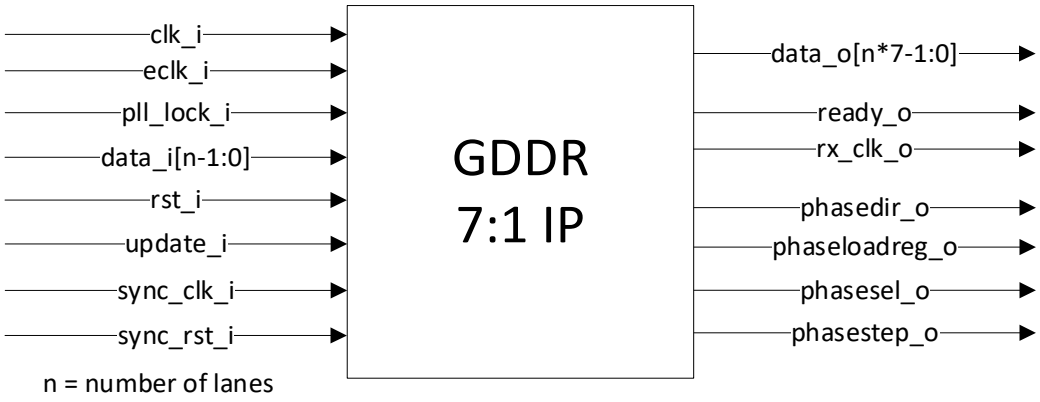

Figure 2.5. GDDRX71_RX.ECLK with GDDR_SYNC, BW_ALIGN and External PLL Enabled Block Diagram

When Bit and Word Alignment feature is enabled, the BW_ALIGN Soft IP logic is added on the Receive interface IP components. This component will control the PLL dynamic clock phase shifting, and DDR components align input to perform the bit and word alignment respectively. When the setting *Use External PLL* is enabled, ports eclk_i, pll_lock_i, phasedir_o, phaseload_reg_o, phasesel_o, and phasestep_o are available. In this case, edge clock signal is generated from any of the external PLL's output clocks while the PLL's lock output is also passed to this IP configuration to signify the GDDR SYNC module to start the clock and reset synchronization. Aside these differences, functionality remains the same.

Figure 2.6 show receive interface type, bit and word alignment and data delay control enabled block diagram and interface with internal PLL.

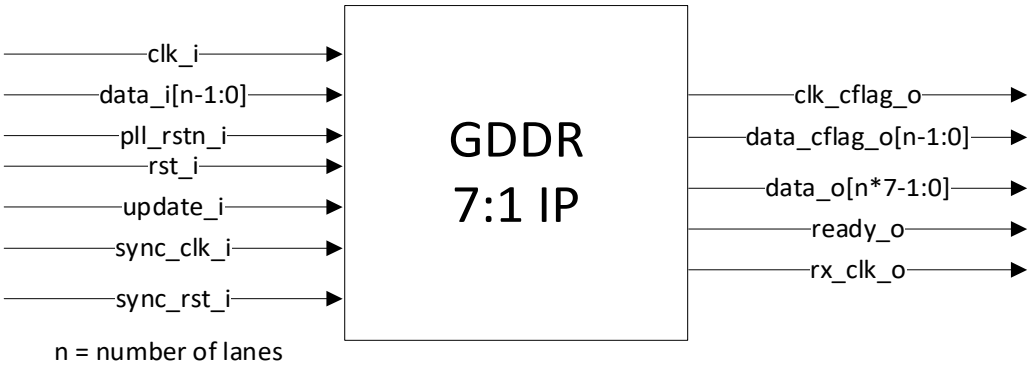

Figure 2.6. GDDRX71_RX.ECLK with GDDR_SYNC, Internal GPLL, BW_ALIGN and Data Delay Control Block Diagram

When data delay control option is enabled, it provides the IP automatic control to add data delay on the DDR data path. For this feature, the IP checks if the data is on the center of the edge clock. It delays the data to determine the valid window then place the data on the center of the window. Once synchronization, alignment and data delay are all performed, ready_o signal will be asserted by the IP.

Figure 2.7 show receive interface type, bit and word alignment and data delay control enabled block diagram and interface with external PLL.

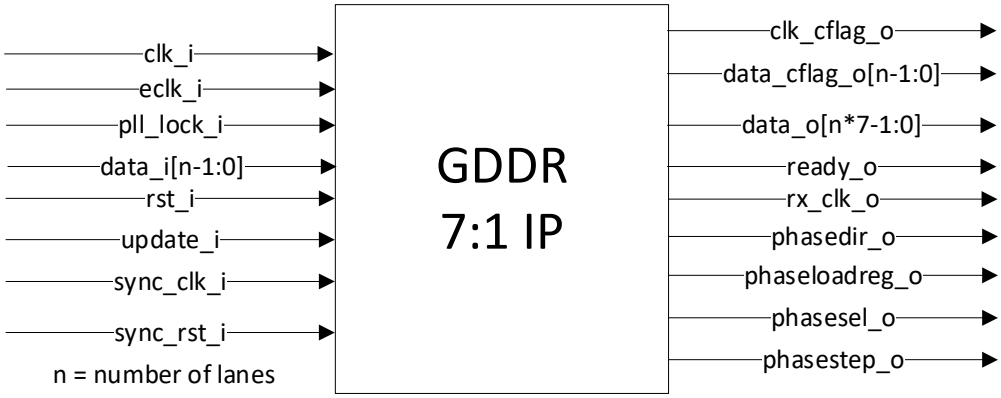

Figure 2.7. GDDRX71_RX.ECLK with GDDR_SYNC, BW_ALIGN, Data Delay Control and External PLL Enabled Block Diagram

When data delay control option is enabled, it provides the IP automatic control to add data delay on the DDR data path. For this feature, the IP checks if the data is on the center of the edge clock. It delays the data to determine the valid window then place the data on the center of the window. Once synchronization, alignment and data delay are all performed, ready_o signal will be asserted by the IP. In this case, edge clock signal is generated from any of the external PLL's output clocks while the PLL's lock output is also passed to this IP configuration to signify the GDDR SYNC module to start the clock and reset synchronization. Aside these differences, functionality remains the same.

2.2.1. RX Output Data Mapping

Bus Width = 2

data_i[1:0] = a[1:0], b[1:0], c[1:0], d[1:0], e[1:0], f[1:0], g[1:0]

data_o[7*2-1:0] = {g[1:0],f[1:0], e[1:0], d[1:0], c[1:0], b[1:0], a[1:0]}

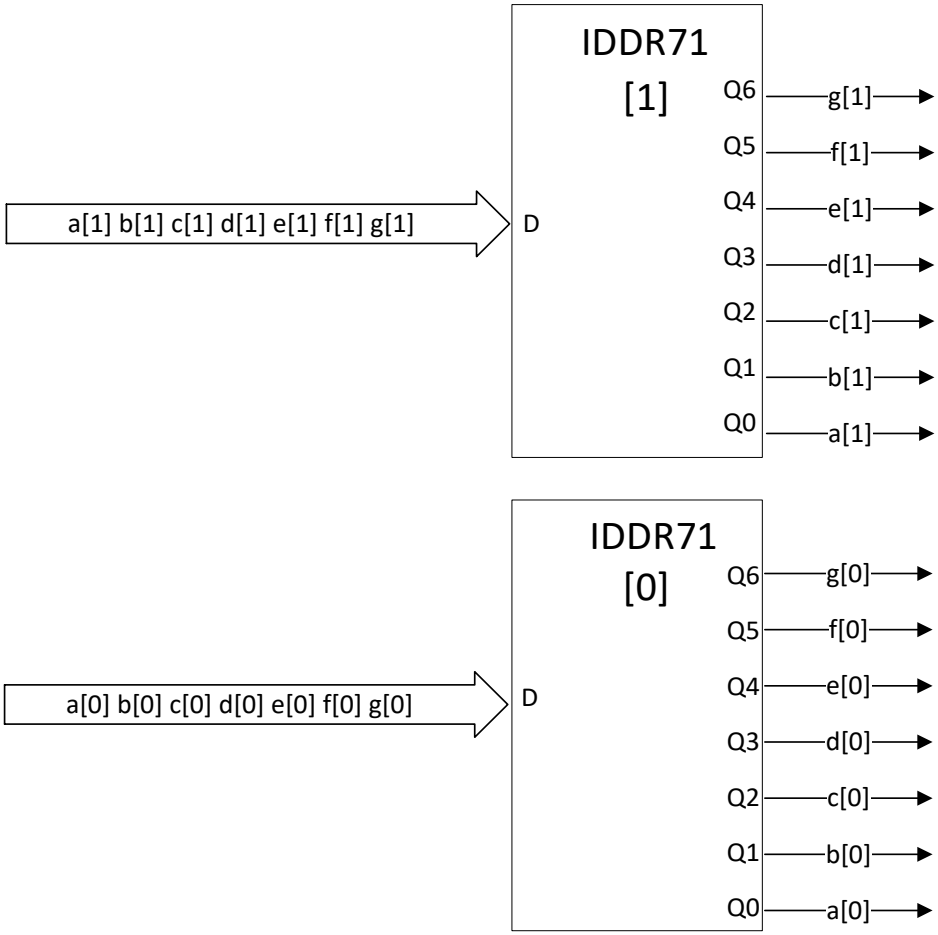

Figure 2.8. Rx Output Data Mapping

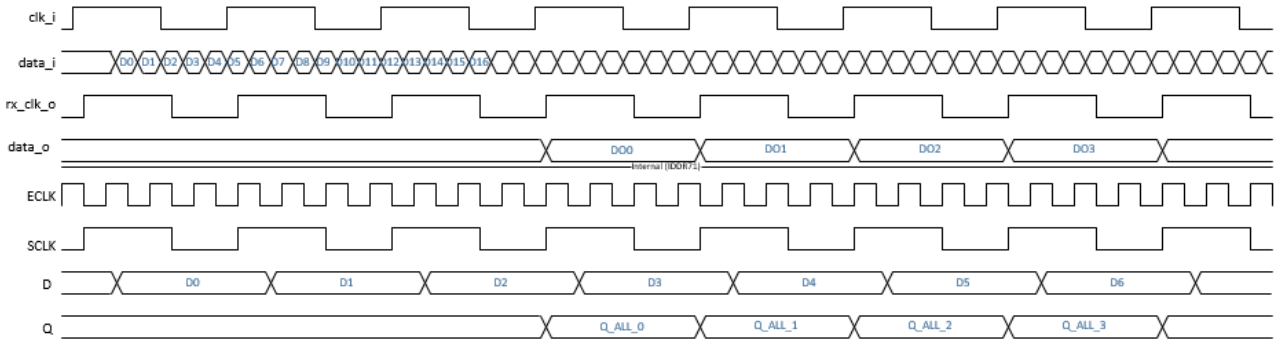

Figure 2.9. Rx Timing Diagram

As shown in Figure 2.8, for GDDR71 Rx configuration, when Bus Width is 2 bits, the IP generates two IDDR71 modules (in our example for X3.5, the number of data_i batches is seven.).

The first batch of incoming data_i[a1:a0] is captured on the rising edge of the fast clock. The next batch of data_i[b1:b0] is captured on the falling edge of the fastest clock and so on. The fast clock in this case is ECLK since it has the greater frequency.

In the figure, this translates to the batch of the input data's slowest bits data_i[g1:g0] being placed on the data_o vector's highest bits [13:12]. Similarly, data_i[f1:f0] bits are placed on data_o[11:10] and so on. The sum of all the IDDR71 outputs is a data_o[13:0] vector.

Figure 2.9 shows the timing diagram of the said example.

2.2.2. GDDRX71_RX Word Alignment Function

The IDDR71 supports slip function for word alignment. This operation stops the clock (SCLK) for one ECLK cycle when the ALIGNWD signal has a transition from low to high. Each time ALIGNWD has a transition from low to high it can skip two bits.

Figure 2.10 shows the Word Alignment Diagram.

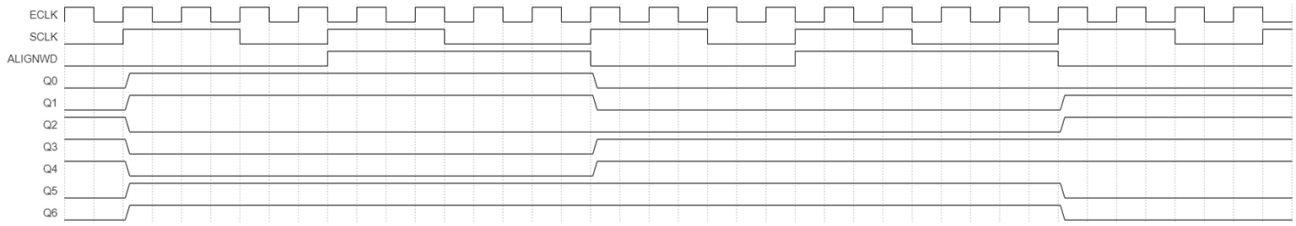

Figure 2.10. GDDRX71_RX Word Alignment Diagram

GDDRX71_TX.ECLK

This is a specialized transmit interface (called 7:1 LVDS, FPD-Link, or OpenLDI) using 7:1 gearing and ECLK. The output clock going out is divided by 3.5 using ECLKDIV. The output clock is used to capture the data at the ODDR71 module. Transmit side for the 7:1 LVDS interface DDR using the 7:1 gearing with ECLK. The clock output is aligned to the data output.

Figure 2.11 show GDDR 7:1 I/O transmit block diagram and interface respectively.

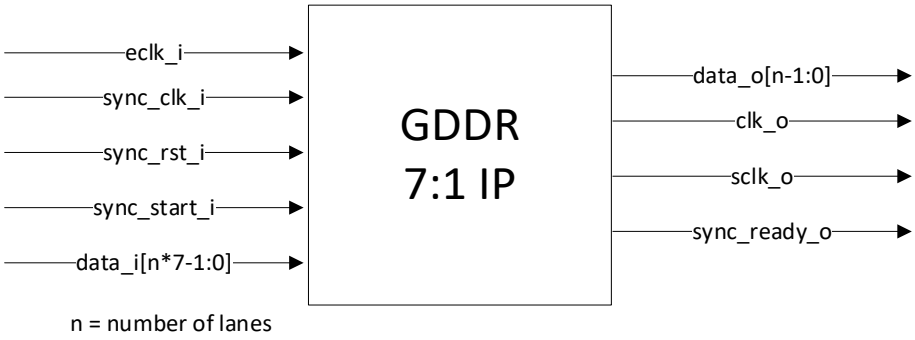

Figure 2.11. GDDRX71_TX.ECLK Static Delay Block Diagram

Described below are the components of this configuration:

- Clock IP components provides edge clock alignment. It also derives the slow clock, sclk_o, from the edge clock divided by 3.5 to support the gearing data ratio. The divided clock is available externally. Like the slow clock, the output clock, clk_o is derived by dividing the edge clock by 3.5.
- DDR Clock IP component generates the receiver clock word as parallel output.

- DDR Data IP component generates the output data. Output is generated with the slow clock.
- GDDR_SYNC Soft IP logic performs sequence to synchronize all the resets of the IP components once sync_start_i signal is asserted. The synchronization happens before TX operation starts. When done, it asserts sync_ready_o signal to indicate that an operation can already be started. This component has its own reset input, sync_rst_i.

2.2.3. TX Input Data Mapping

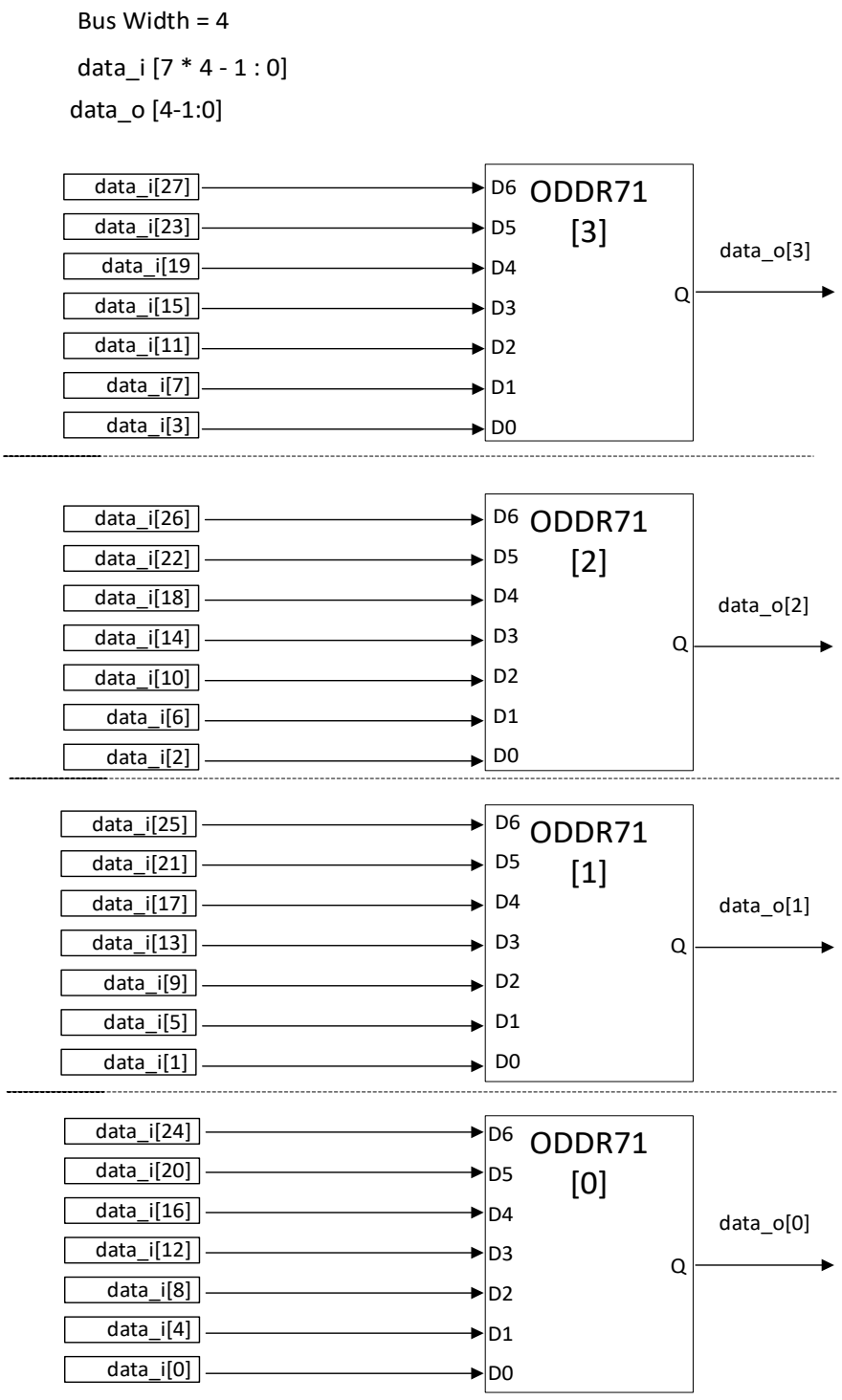

Figure 2.12. Tx Input Data Mapping

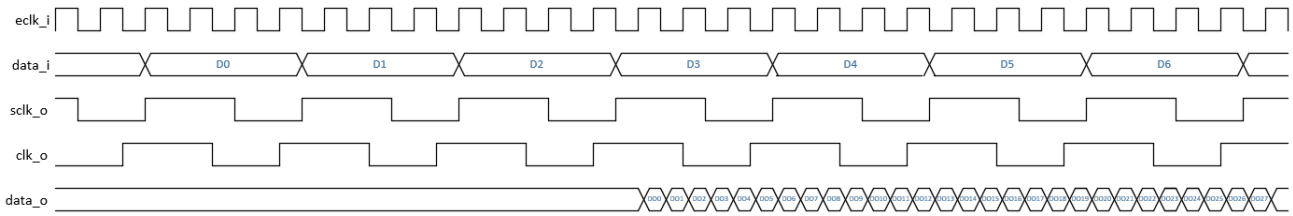

Figure 2.13. Tx Timing Diagram

As shown in Figure 2.12, for GDDR 7:1 Tx configuration, when Bus Width is 4 bits, the IP generates four ODDR71 modules. The entire input data is broken down into 7 groups, each group with the size of 4 bits. The group with the fastest bits data_i[3:0] is transmitted first, followed by data_i[7:4] and so on.

Figure 2.13 shows the timing diagram of the said example.

2.3. Signal Description

Table 2.3. GDDR 7:1 I/O Module Receive Signal Description

Port Name	Direction	Width(bits)	Description
Clock and Reset			
rx_clk_o	OUT	1	Clock output for Receive interface. Divided RX clock form 7:1 RX interface produced by ECLKDIV. This is only available when *Interface Type* is Receive.
sync_clk_i	IN	1	Startup clock. A low-speed continuously running clock input. Its frequency is independent to the input clock but it must be significantly lower.
sync_rst_i	IN	1	Active high reset signal. Can be used asynchronously to the input clock, but it is recommended to be de-asserted synchronously with sync_clk_i.
rst_i	IN	1	Active HIGH reset signal when *Enable Bit and Word Alignment Soft IP* is enabled.
eclk_i	IN	1	Receive data sampling clock. This clock can be from a PLL clock output. This is only available when *Use External PLL* is enabled.
User Interface			
alignwd_i	IN	1	This signal is used for word alignment. It shifts word by one bit. This is only available when *Enable Bit and Word Alignment Soft IP* is disabled.
pll_rstn_i	IN	1	Active low reset of internal PLL. This is available only when *Interface Type* is Receive and *Use External PLL* is disabled.
phasedir_i	IN	1	Phase rotation direction of internal PLL. This is available only when *Interface Type* is Receive, *Enable Bit and Word Alignment Soft IP, Enable Data Delay Control* and *Use External PLL* are all disabled.
phasestep_i	IN	1	Rotate phase of internal PLL. This is available only when *Interface Type* is Receive, *Enable Bit and Word Alignment Soft IP, Enable Data Delay Control* and *Use External PLL* are all disabled.
update_i	IN	1	Start bit and word alignment, or restart procedure if optimization is needed again. This is available only when *Interface Type is* Receive *and Enable Bit and Word Alignment Soft IP* is enabled.
pll_lock_i	IN	1	Starts GDDR_SYNC clock and reset synchronization. This can be the PLL lock output. This is only available when *Use External PLL* is enabled.
data_cflag_o	OUT	n	Underflow or overflow flag to indicate minimum or maximum data path delay adjustment is reached. This is available only when *Interface Type* is Receive *and Enable Data Delay Control* is enabled.
clk_cflag_o	OUT	1	Underflow or overflow flag to indicate minimum or maximum clock path delay adjustment is reached. This is available only when *Interface Type* is Receive *and Enable Data Delay Control* is enabled.
data_o	OUT	n*7	Received input data to fabric.
sync_ready_o	OUT	1	Indicate that startup is finished, and RX circuit is ready to operate. Only available when *Enable Bit and Word Alignment Soft IP* is disabled.
ready_o	OUT	1	Indicates alignment is done, startup is finished, and RX circuit is ready to operate. This is only available when *Enable Bit and Word Alignment Soft IP* is enabled.
rx_clk_word_o	OUT	7	Valid receiver clock word size allowance. Parallel data output. Only available when *Enable Bit and Word Alignment Soft IP* is disabled.
phasedir_o	OUT	1	BW_ALIGN module output signal to control the direction of rotate phase for dynamic phase shift of external PLL clock output. This is only available when *Use External PLL* and *Enable Bit and Word Alignment Soft IP* are both enabled.

Port Name	Direction	Width(bits)	Description
phasestep_o	OUT	1	BW_ALIGN module output signal to control the rotate phase for dynamic phase shift of external PLL clock output. This is only available when *Use External PLL* and *Enable Bit and Word Alignment Soft IP* are both enabled.
phaseloadreg_o	OUT	1	BW_ALIGN module output signal to initiate the dynamic phase shift of external PLL. This is only available when *Use External PLL* and *Enable Bit and Word Alignment Soft IP* are both enabled.
phasesel_o	OUT	3	BW_ALIGN module output signal, which specifies the clock output to where dynamic phase shift of external PLL will be applied. This is only available when *Use External PLL* and *Enable Bit and Word Alignment Soft IP* are both enabled.
I/O Pad Interface			
clk_i	IN	1	Clock input signal from I/O.
data_i	IN	n	Data input signal from I/O.

Note: n = number of lanes.

Table 2.4. GDDR 7:1 I/O Module Transmit Signal Description

Port Name	Direction	Width(bits)	Description
Clock and Reset			
eclk_i	IN	1	Transmit data sampling clock.
sclk_o	OUT	1	Clock output for *Interface Type* is Transmit.
sync_clk_i	IN	1	Low speed continuously running clock input.
sync_rst_i	IN	1	Active HIGH reset signal.
User Interface			
data_i	IN	n*7	Transmit output data going to I/O.
sync_ready_o	OUT	1	Indicate that startup is finished, and TX circuit is ready to operate.
sync_start_i	IN	1	Waits for the PLL lock signal to start the synchronization.
I/O Pad Interface			
clk_o	OUT	1	Clock output signal to I/O.
data_o	OUT	n	Data output signal to I/O. Value range is [1, 16].

Note: n = number of lanes

2.4. Attribute Summary

Table 2.5 provides a list of user-configurable attributes for the GDDR 7:1 I/O Module. Attributes settings are specified using GDDR 7:1 I/O Module Configuration user interface in Lattice Radiant.

Table 2.5. Attributes Table

Attribute	Selectable Values	Default	Dependency on other Attributes	Additional Requirements
Interface Type	Receive, Transmit	Receive	—	—
Bus Width	1–16	8	—	—
Interface Bandwidth (Mbps)	126-945 (Receive) 70-945 (Transmit)	945	—	—
Use External PLL	Checked, Unchecked	Unchecked	*Interface Type = Receive*	Device used is LFMXO5-25.
Clock Frequency (MHz)	18–135 (Receive) 10-945 (Transmit)	135	*Bandwidth/7*	Display for information only
External PLL Reference Clock and Primary Clock Output Frequency	18–135	135	*Interface Type = Receive* *Bandwidth/7*	Display for information only when device used is LFMXO5-25
External PLL Secondary Clock Output Frequency	63–472.5	472.5	*Interface Type = Receive* *Bandwidth/2*	Display for information only when device used is LFMXO5-25
Enable Bit and Word Alignment Soft IP	Checked, Unchecked	Unchecked	*Interface Type = Receive*	—
Enable Data Delay Control	Checked, Unchecked	Unchecked	*Interface Type = Receive* and *Enable Bit and Word Alignment Soft IP* is checked	—
Reference Clock from I/O Pin	Checked, Unchecked	Unchecked	*Interface Type = Transmit*	—
Reference Clock Input Buffer Type	(Legal Combination Table)	LVDS	*Reference Clock from I/O Pin* is checked	—

Note: The attributes can be configured from the General Tab of the Lattice Radiant Software user interface.

Table 2.6 below presents attribute description.

Table 2.6. Attributes Description

Attribute Name	Description
Interface Type	RECEIVE or TRANSMIT interface type
Bus Width	Total number of lanes/bus width
Interface Bandwidth (Mbps)	Interface Clock Frequency
Use External PLL	Option to use external PLL on Receive interface type
External PLL Reference Clock and Primary Clock Output Frequency	Value for both external PLL reference clock and primary clock output frequencies. The PLL primary clock output will control the edge clock input of Receive interface type.
External PLL Secondary Clock Output Frequency	Value of external PLL secondary clock output frequency to be used as input to Receive interface type. This can be dynamically phase-shifted manually or automatically depending on BW_ALIGN Soft IP setting.
Enable Bit and Word Alignment Soft IP	Optional bit and word alignment Soft IP (BW_ALIGN) module. The bit alignment module centers the edge clock to the middle of the data eye and the word alignment module is used to achieve the 7-bit word alignment.
Enable Data Delay Control	When enabled, BW_ALIGN Soft IP module automatically controls the movement of the data on DELAY module.
Reference Clock from I/O Pin	Reference Clock from I/O Pin
Reference Clock Input Buffer Type	List of Single-ended or Differential I/O supported

3. IP Generation, Simulation, and Validation

This section provides information on how to generate the IP using the Lattice Radiant Software and how to run simulation and synthesis. For more details on the Lattice Radiant Software, refer to the Lattice Radiant software user guide.

3.1. Generating the IP

The Lattice Radiant Software allows you to customize and generate modules and IPs and integrate them into the device's architecture. The procedure for generating the GDDR 7:1 I/O module in Lattice Radiant Software is described below.

To generate GDDR 7:1 I/O Module:

1. Create a new Lattice Radiant Software project or open an existing project.

In the **IP Catalog** tab, double-click on **GDDR 7:1** under **Module, Architecture_Modules, I/O** category. The **Module/IP Block Wizard** opens as shown in Figure 3.1. Enter values in the **Component name** and the **Create in** fields and click **Next**.

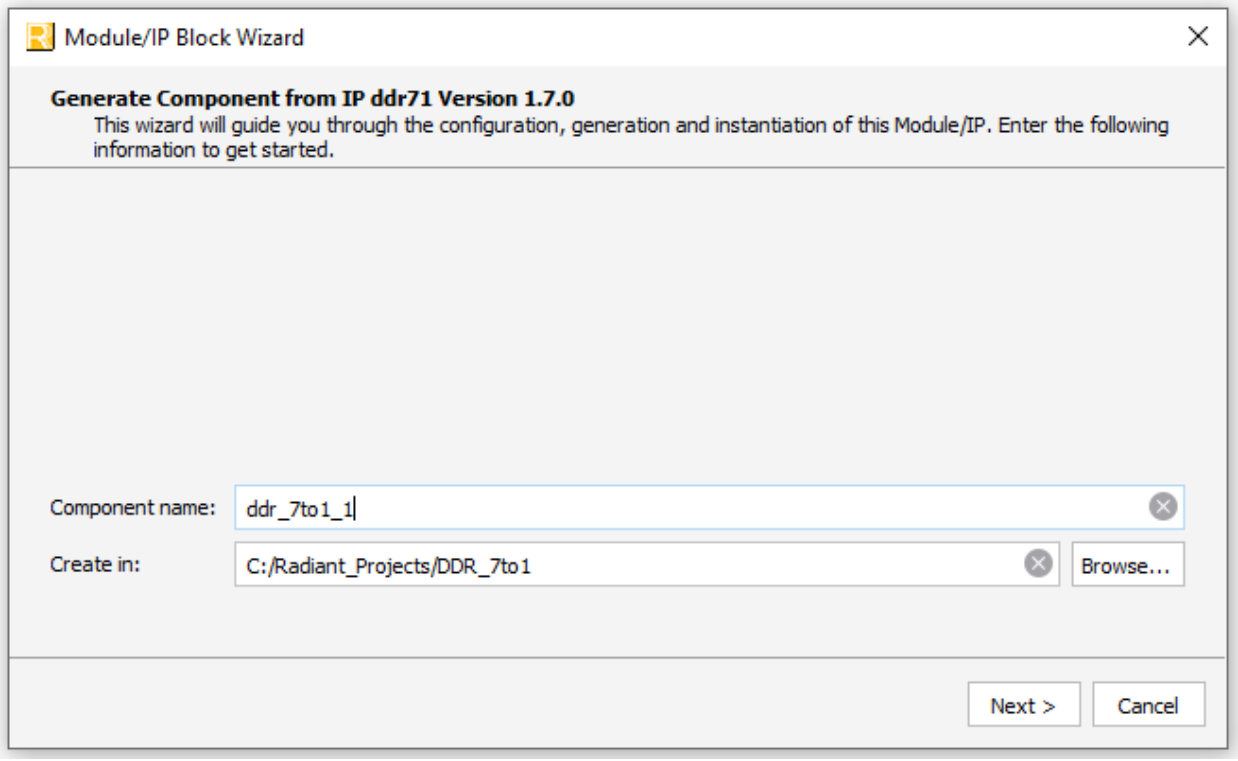

Figure 3.1. Module/IP Block Wizard

2. In the module's dialog box of the **Module/IP Block Wizard** window, customize the selected GDDR 7:1 I/O module using drop-down menus and check boxes. As a sample configuration, see Figure 3.2. For configuration options, see the Attribute Summary section.

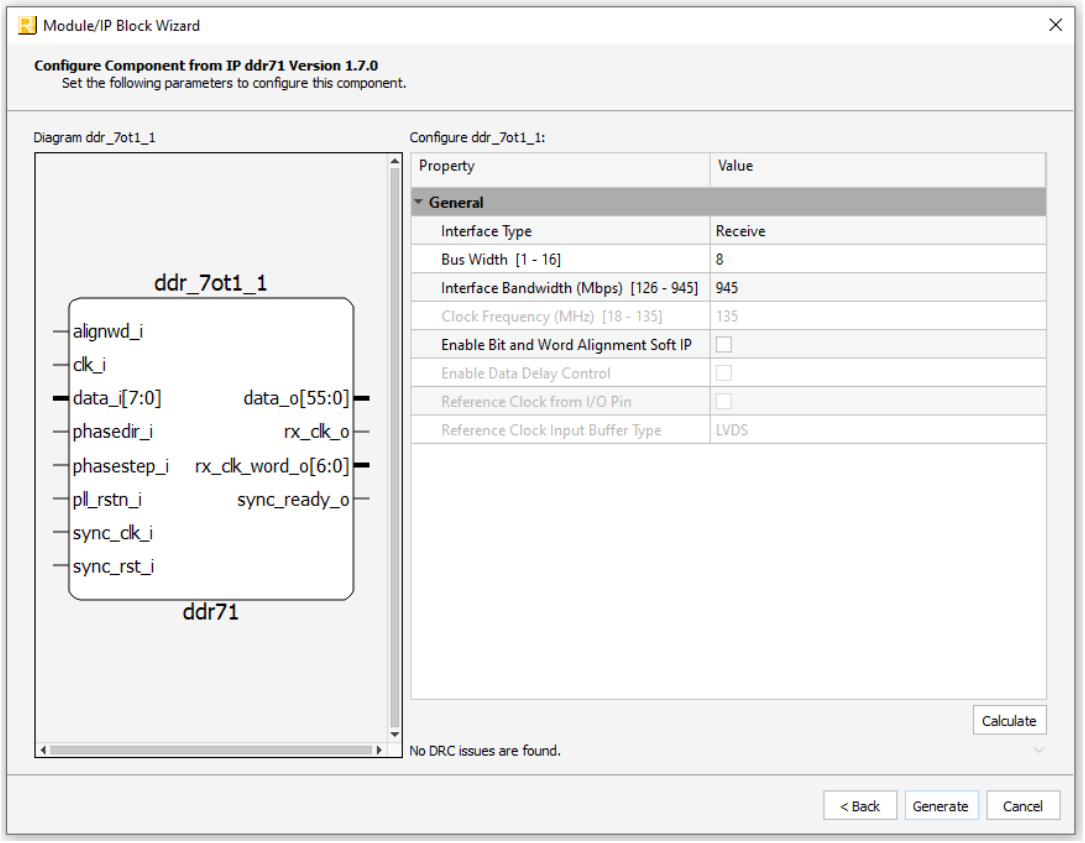

Figure 3.2. Configure Block of GDDR 7:1 I/O Module

3. Click **Generate**. The **Check Generated Result** dialog box opens, showing design block messages and results as shown in Figure 3.3.

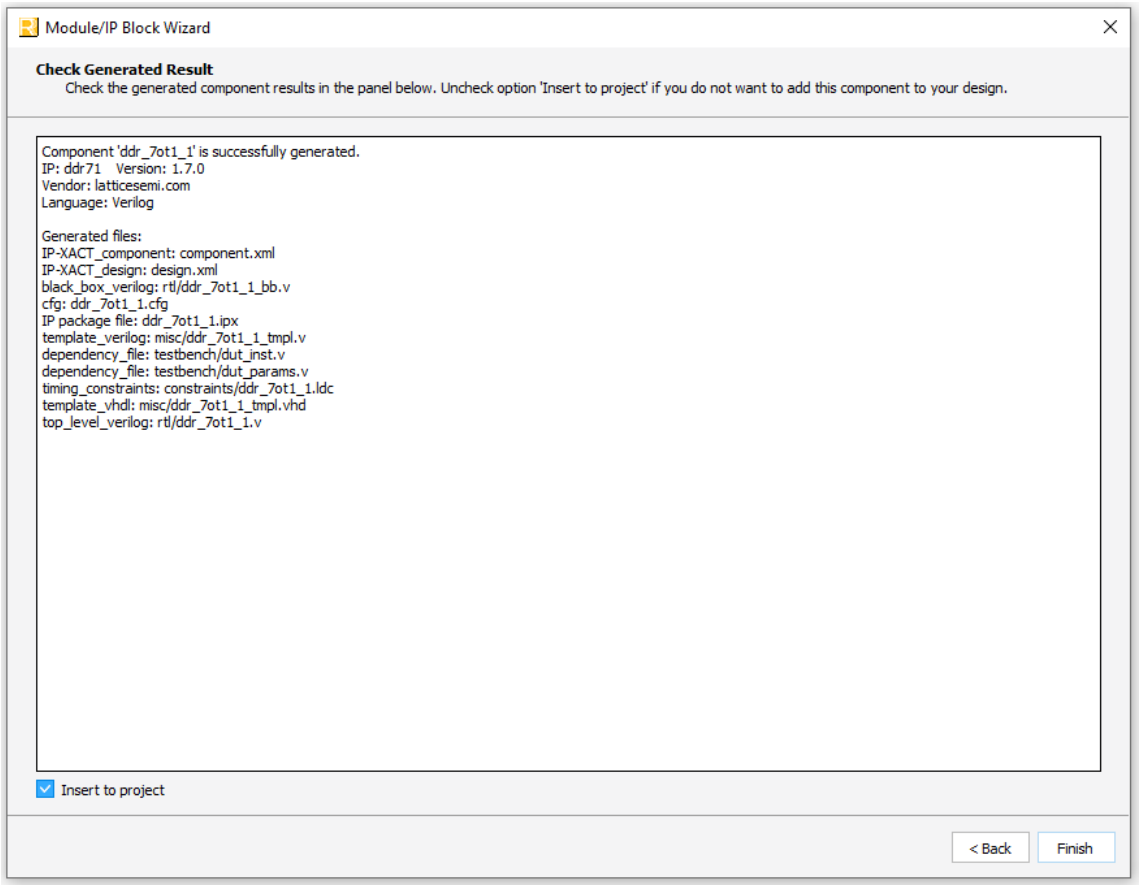

Figure 3.3. Check Generated Result

4. Click the **Finish** button. All the generated files are placed under the directory paths in the **Create in** and the **Component name** fields shown in Figure 3.1.

The generated GDDR 7:1 I/O module package includes the black box (<Instance Name>_bb.v) and instance templates (<Instance Name>_tmpl.v/vhd) that can be used to instantiate the module in a top-level design. An example RTL top-level reference source file (<Instance Name>.v) that can be used as an instantiation template for the module is also provided. You may also use this top-level reference as the starting template for the top-level for their complete design. The generated files are listed in Table 3.1.

Table 3.1. Generated File List

Attribute	Description
<Instance Name>.ipx	This file contains the information on the files associated to the generated IP.
<Instance Name>.cfg	This file contains the parameter values used in IP configuration.
component.xml	Contains the ipxact:component information of the IP.
design.xml	Documents the configuration parameters of the IP in IP-XACT 2014 format.
rtl/<Instance Name>.v	This file provides an example RTL top file that instantiates the module.
rtl/<Instance Name>_bb.v	This file provides the synthesis black box.
misc/<Instance Name>_tmpl.v misc /<Instance Name>_tmpl.vhd	These files provide instance templates for the module.

3.2. Running Functional Simulation

After the IP is generated, running functional simulation can be performed using different available simulators. The default simulator already has pre-compiled libraries ready for simulation. Choosing a non-default simulator, however, may require additional steps.

To run functional simulation using the default simulator:

1. Click the  button located on the **Toolbar** to initiate **Simulation Wizard**, as shown in Figure 3.4.

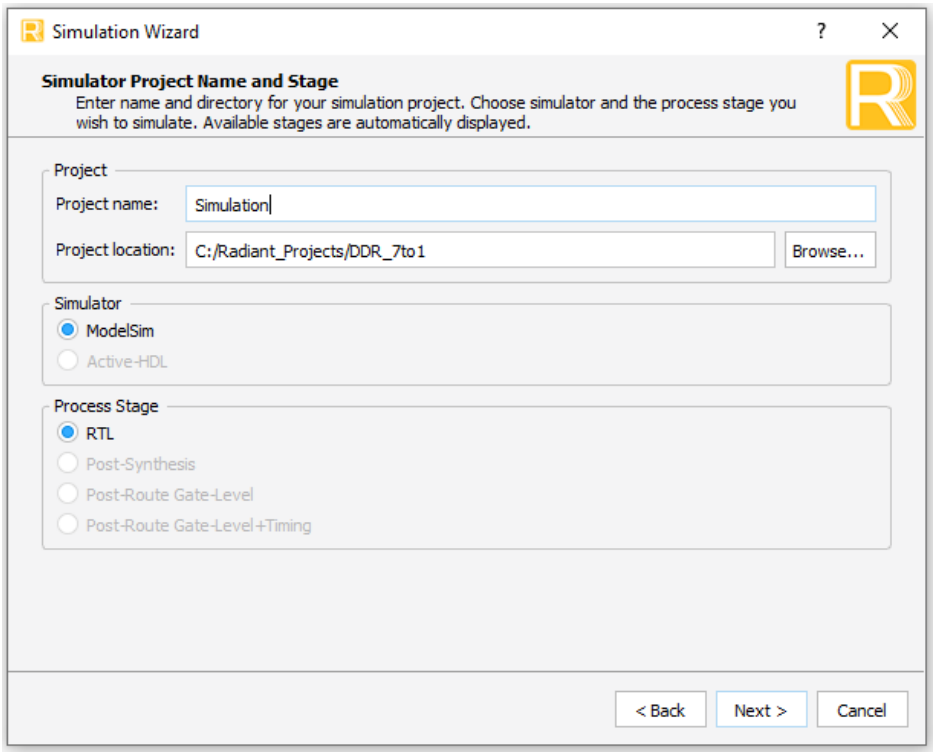

Figure 3.4. Simulation Wizard

2. Click **Next** to open the **Add and Reorder Source** window as shown in Figure 3.5.

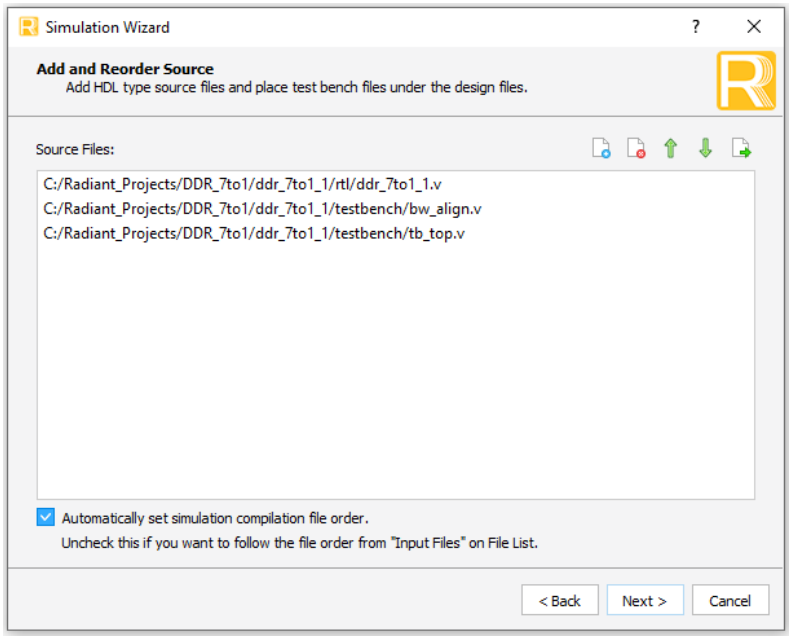

Figure 3.5. Adding and Reordering Source

3. Click **Next**. The Summary window is shown. Click **Finish** to run the simulation.

Note: It is necessary to follow the procedure above until it is fully automated in the Lattice Radiant Software Suite.

The results of the simulation in our example are provided in Figure 3.6.

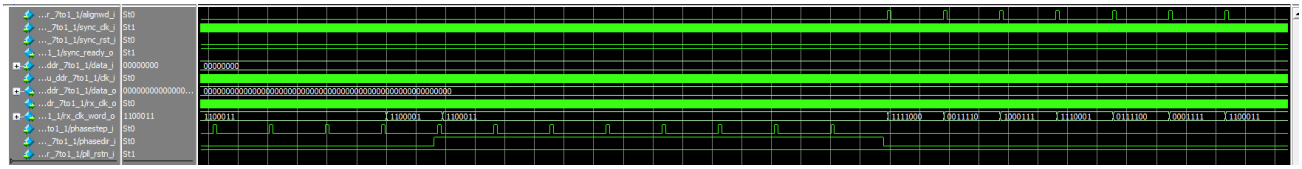

Figure 3.6. Simulation Waveform

3.3. Constraining the IP

You need to provide proper timing and physical design constraints to ensure that your design meets the desired performance goals on the FPGA. Add the content of the following IP constraint file to your design constraints:

<IP_Instance_Path>/<IP_Instance_Name>/eval/constraints.pdc.

The constraint file has been verified during IP evaluation with the IP instantiated directly in the top-level module. You can modify the constraints in this file with thorough understanding of the effect of each constraint.

To use this constraint file, copy the content of *constraints.pdc* to the top-level design constraint for post-synthesis.

Refer to Lattice Radiant Timing Constraints Methodology (FPGA-AN-02059) for details on how to constraint your design.

3.4. IP Evaluation

There is no restriction on the IP evaluation of this module.

Appendix A. Resource Utilization

DDR 7:1 module resource utilization are shown on Table A.1 and Table A.2 using LIFCL-40-9BG400I, and LFCPNX-100-9LFG672I device with Lattice Synthesis Engine of Lattice Radiant software 3.1. The default configuration is used and some attributes are changed from the default value to show the effect on the resource utilization.

Table A.1. Resource Utilization (LIFCL)

Configuration	Clk Fmax (MHz)[1]	Registers	LUTs[2]	EBRs	DSPs
Default	135	12	34	0	0
Interface Type = Transmit, others = Default	135	12	33	0	0

Notes:

1. Fmax s generated when the FPGA design only contains the DDR 7:1 module and target frequency is 135 MHz. FPGA can run up to 200 MHz, but the DDR 7:1 module can be used up to 945 MHz ECLK and 135 MHz SCLK only. These values may be reduced when user logic is added to the FPGA design.
2. The *distributed RAM* utilization is accounted for in the total LUT4s utilization. The actual LUT4 utilization is distribution among *logic, distributed RAM*, and *ripple logic*.

Table A.2. Resource Utilization (LFCPNX)

Configuration	Clk Fmax (MHz)[1]	Registers	LUTs[2]	EBRs	DSPs
Default	135	12	34	0	0
Interface Type = Transmit, others = Default	135	12	33	0	0

Notes:

1. Fmax is generated when the FPGA design only contains the DDR 7:1 module and target frequency is 135 MHz. FPGA can run up to 250 MHz, but the DDR 7:1 module can be used up to 945 MHz ECLK and 135 MHz SCLK only. These values may be reduced when user logic is added to the FPGA design.
2. The *distributed RAM* utilization is accounted for in the total LUT4s utilization. The actual LUT4 utilization is distribution among *logic, distributed RAM*, and *ripple logic*.

References

- Lattice Radiant Software web page
- Lattice Solutions IP Cores web page
- Lattice Radiant Timing Constraints Methodology (FPGA-AN-02059)
- Lattice Insights web page for Lattice Semiconductor training courses and learning plans

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/en/Support/AnswerDatabase.

Revision History

Revision 1.8, June 2024

Section	Change Summary
All	• Update title from *DDR 7:1 Module - Lattice Radiant Software* to *DDR 7:1 Module.* • Made editorial fixes.
Introduction	Added option to use external PLL in the Features section.

Functional Description	• Overview:
	  • Added description for Table 2.2. Summary of the Soft Logic.
	• Functional Diagrams:
	  • Added description for Figure 2.2. GDDRX71_RX.ECLK with GDDR_SYNC and Internal GPLL (without BW_ALIGN) Block Diagram.
	  • Removed the following figures and updated the figures numbers of remaining figures accordingly:
	  • Removed Figure 2.3 GDDRX71_RX.ECLK with GDDR_SYNC and Internal GPLL (without BW_ALIGN) Interface
	  • Figure 2.5 GDDRX71_RX.ECLK with GDDR_SYNC and External PLL Enabled Interface
	  • Figure 2.7 GDDRX71_RX.ECLK with GDDR_SYNC, Internal GPLL and BW_ALIGN Interface
	  • Figure 2.9 GDDRX71_RX.ECLK with GDDR_SYNC, BW_ALIGN and External PLL Enabled Interface
	  • Figure 2.11 GDDRX71_RX.ECLK with GDDR_SYNC, Internal GPLL, BW_ALIGN and Data Delay Control Interface
	  • Figure 2.13 GDDRX71_RX.ECLK with GDDR_SYNC, BW_ALIGN and Data Delay Control and External PLL Enabled Interface
	  • Figure 2.14 Internal GPLL Control of GDDRX71_RX.ECLK with BW_ALIGN Interface
	  • Figure 2.15 Internal GPLL Control of GDDRX71_RX.ECLK without BW_ALIGN Interface
	  • Figure 2.19 GDDRX71_RX.ECLK Static Delay Interface
	  • Added description for Figure 2.11. GDDRX71_TX.ECLK Static Delay Block Diagram.
	  • Added new figure:
	  • Figure 2.9. Rx Timing Diagram.
	  • Figure 2.13. Tx Timing Diagram.
	• Signal Description:
	  • Updated the descriptions for the following ports in Table 2.3. GDDR 7:1 I/O Module Receive Signal Description:
	  • *sync_clk_i*
	  • *sync_rst_i*
	• Attribute Summary:
	  • Updated the *Selected Values* for the following *attributes* in Table 2.5. Attributes Table:
	  • *Interface Bandwidth (Mbps)*
	  • *Clock Frequency (Mhz)*

IP Generation, Simulation, and Validation	• Removed Required Post Synthesis Constraints section. • Newly added section Constraining the IP.
Reference	Updated the reference list.

Revision 1.7, March 2023

Section	Change Summary
Acronyms in This Document	Updated the GDDR definition.
Introduction	Added option to use external PLL in the Features section.

Functional Description	• Functional Diagrams:
	  • updated description adding the support of external PLL in the section;
	  • added new interface and block diagrams Figure 2.4. GDDRX71_RX.ECLK with GDDR_SYNC and External PLL Enabled Block Diagram,
	  • Figure 2.5. GDDRX71_RX.ECLK with GDDR_SYNC and External PLL Enabled Interface, Figure 2.8. GDDRX71_RX.ECLK with GDDR_SYNC, BW_ALIGN and External PLL Enabled Block Diagram, Figure 2.9. GDDRX71_RX.ECLK with GDDR_SYNC, BW_ALIGN and External PLL Enabled Interface,
	  • Figure 2.12. GDDRX71_RX.ECLK with GDDR_SYNC, BW_ALIGN, Data Delay Control and External PLL Enabled Block Diagram, and Figure 2.13. GDDRX71_RX.ECLK with GDDR_SYNC, BW_ALIGN, Data Delay Control and External PLL Enabled Interface.
	• Signal Description:
	  • Table 2.3. GDDR 7:1 I/O Module Receive Signal Description: newly added eclk_i, pll_lock_i, phasedir_o, phasestep_o, phaseloadreg_o, and phasesel_o signals and their related data.
	• Attribute Summary:
	  • Table 2.5. Attributes Table: newly added *Use External PLL*, *External PLL Reference Clock and Primary Clock Output Frequency*, and *External PLL Secondary Clock Output Frequency* attributes and their related data.
	  • Table 2.6. Attributes Description: newly added *Use External PLL*, *External PLL Reference Clock and Primary Clock Output Frequency*, and *External PLL Secondary Clock Output Frequency* attributes and their related description.

IP Generation, Simulation, and Validation	Updated Figure 3.1. Module/IP Block Wizard, Figure 3.2. Configure Block of GDDR 7:1 I/O Module, Figure 3.3. Check Generated Result reflecting the most recent Lattice Radiant software user interface.
Technical Support Assistance	Added the Frequently Asked Questions website link.

Revision 1.6, October 2022

Section	Change Summary
Functional Diagrams	• Updated Figure 2.16. Rx Output Data Mapping. Updated from “The entire input data is broken down into four groups, each group with the size of 7 bits. The group with the fastest bits [24, 20, 16, 12, 8, 4, 0] is transmitted first, and so on.” to “The entire input data is broken down into 7 groups, each group with the size of 4 bits. The group with the fastest bits data_i[3:0] is transmitted first, followed by data_i[7:4] and so on.” in TX Input Data Mapping section. • Added user interface signals in Signal Description section. • Updated Selectable values in Attribute Summary section.
IP Generation, Simulation, and Validation	Updated the heading of Section 3 from “IP Generation and Evaluation” to “IP Generation, Simulation, and Validation”. • Removed “Licensing the IP” section. Updated the heading of Section 3.1 from “Generation and Synthesis” to “Generating the IP”. • Updated Figure 3.1. Module/IP Block Wizard, Figure 3.2. Configure Block of GDDR 7:1 I/O Module, Figure 3.3. Check Generated Result. Updated the heading of Section 3.3 from “Hardware Evaluation” to “IP Evaluation”.

Revision 1.5, December 2021

Section	Change Summary
Appendix A. Resource Utilization	Updated section content including adding table for LFCPNX.

Revision 1.4, June 2021

Section	Change Summary
Introduction	• Revised introductory paragraph. • Removed Quick Facts section.
IP Generation and Evaluation	• Revised reference to Lattice Radiant Software User Guide and removed link. • Updated the procedures/user interfaces in the Generation and Synthesis and the Running Functional Simulation sections.
Appendix A. Resource Utilization	Added this section.
References	Revised reference to Lattice Radiant Software User Guide and removed link.

Revision 1.2, June 2020

Section	Change Summary
Introduction	• Added Certus-NX support. • Updated Table 1.1 to add LFD2NX-40 as targeted device. • Updated Lattice Implementation to Lattice Radiant 2.1.
Functional Description	Added the GDDRX71_RX Word Alignment Function.
All	Updated references to Lattice Radiant Software 2.1 User Guide.

Revision 1.1, February 2020

Section	Change Summary
Acronyms in this Document	Updated the table.
Introduction	Updated Table 1.1 to add LIFCL-17 as targeted device.
Functional Description	Updated Figure 2.7.
IP Generation and Evaluation	Updated content of the Generation and Synthesis section.
Appendix	Removed this section.

Revision 1.3, October 2020

Section	Change Summary
Functional Description	In GDDRX71_RX.ECLK, updated statement to "The multiplied clock is used to capture the data at the receive IDDR71 module." • In GDDRX71_RX Word Alignment Function, corrected reference to Figure 2.11. In GDDRX71_TX.ECLK, updated statements to "The output clock going out is divided by 3.5X using ECLKDIV. The multiplied clock is used to capture the data at the ODDR71 module." • Set attributes to italics in Table 2.5. Attributes Table. • Updated description of Enable Bit and Word Alignment Soft IP and Enable Data Delay Control in Table 2.6. Attributes Description.
IP Generation and Evaluation	• Added Required Post Synthesis Constraints sub-section. • Updated introductory paragraph in Running Functional Simulation sub-section.

Revision 1.0, December 2019

Section	Change Summary
All	Changed document status from Preliminary to final.
Quick Facts	Updated the table details.
IP Generation and Evaluation	• Updated details and illustrations. • Removed Licensing and Evaluation and merged contents with this section.
Functional Diagrams	• Added RX Output Data Mapping and TX Input Data Mapping subsections. Added GDDR 7:1 interface diagrams.
Appendix	Added this section.

Revision 0.80, October 2019

Section	Change Summary
All	Preliminary release

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