ADC Sequencer Module - Lattice Radiant Software

User Guide

FPGA-IPUG-02062-1.8

February 2023

Disclaimers

Lattice makes no warranty, representation, or guarantee regarding the accuracy of information contained in this document or the suitability of its products for any particular purpose. All information herein is provided AS IS, with all faults and associated risk the responsibility entirely of the Buyer. Buyer shall not rely on any data and performance specifications or parameters provided herein. Products sold by Lattice have been subject to limited testing and it is the Buyer's responsibility to independently determine the suitability of any products and to test and verify the same. No Lattice products should be used in conjunction with mission- or safety-critical or any other application in which the failure of Lattice's product could create a situation where personal injury, death, severe property or environmental damage may occur. The information provided in this document is proprietary to Lattice Semiconductor, and Lattice reserves the right to make any changes to the information in this document or to any products at any time without notice.

Contents

Figures

Tables

Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
ADC	Analog to Digital Converter
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
AMBA	Advanced Microcontroller Bus Architecture
FPGA	Field Programmable Gate Array
LMMI	Lattice Memory Mapped Interface
PTAT	Proportional to Absolute Temperature)
SAR	Successive Approximation Register
SOC	Start-of-Conversion

1. Introduction

1.1. Quick Facts

Analog to Digital Converter (ADC) with Successive Approximation Register (SAR) architecture is one of the most common and widely used types of ADCs. It is commonly used in data-acquisition, industrial-control and instrumentation applications, where ultra-high speed is not necessary. ADCs with SAR architecture have good resolution and moderately high sampling rate.

The Lattice Semiconductor ADC Sequencer Module incorporates two 12-bit resolution and 1 MSPS conversion speed ADCs. Each IP is implemented with SAR architecture and supports both Continuous and Single-Pass conversion modes. The SAR ADC operates by using a binary search algorithm to converge on the input signal. The Lattice ADC IP includes a configurable Sequencer Module, which automates ADC data acquisition process. ADC IP also supports configurable over/under voltage and temperature alarming function. Both the Sequencer Module and alarm functions can be configured through the Lattice Memory Mapped Interface (when LMMI is enabled) and through the user interface.

The ADC IP can be targeted to the Lattice FPGA devices built on the Lattice Nexus™ platform and is implemented using the Lattice Radiant™ software Place and Route tool integrated with the either Synplify Pro® or Lattice LSE synthesis tool.

1.2. Features

The key features of the ADC Sequencer Module include:

- 12-bit or better resolution
- 1 MSPS sampling rate
- Selectable input signal source among 24 input channels, 12 for each ADC0 and ADC1 cores
- Uni-polar or bi-polar input conversion option
- SNDR – 68 dB with 50 kHz input signal at 1 MSPS conversion speed
- THD – 76 dB with 50 kHz input signal at 1 MSPS conversion speed
- INL < +/– 2LSB, DNL < +/– 1 LSB
- Option for internal 1.1 V to 1.3 V or external 1.0 V to 1.8 V reference voltage
- Input signal range 0 V to 1.8 V (1.2 V with internal reference case, 1.8 V with external ref)
- Vdd = 1.8 V for Analog, Vdd=1.0 V/0.9 V for Digital
- Power < 1 mW at maximum conversion speed
- Power Down Mode for sleep
- Sequential or simultaneous sampling option between two ADCs
- Internal junction temperature monitoring diode
- Five power supplies' voltage monitoring
- Three continuous-time comparators
- Configurable automated data acquisition process
- Configurable Over/Under Voltage alarm function
- AXI-4 based Interface along with the native output signals supports ADC IP output data flow
- LMMI based Interface for ADC IP output data flow support
- Up to 16 ADC GPIO differential pairs (11 – for LIFCL-17)

1.3. Conventions

1.3.1. Nomenclature

The nomenclature used in this document is based on Verilog HDL.

1.3.2. Signal Names

Signal names that end with:

- *_n* are active low
- *_i* are input signals
- *_o* are output signals

2. Functional Description

2.1. Overview

As shown in Figure 2.1, the ADC Sequencer Module consists of the following main design modules:

- ADC Analog Module:
  - Two independent 12-bit SAR ADC cores
  - Three continuous-time comparators
  - ADC core Auto Calibration Controllers per ADC core
  - Internal Reference Voltage Generation Block
- ADC Wrapper:
  - Sequencer Module
  - Alarm Module
  - AXI4-Stream Interface
  - LMMI Slave Module
  - Configuration Registers Block Module

A top-level block diagram of ADC Sequencer Module is shown in Figure 2.1.

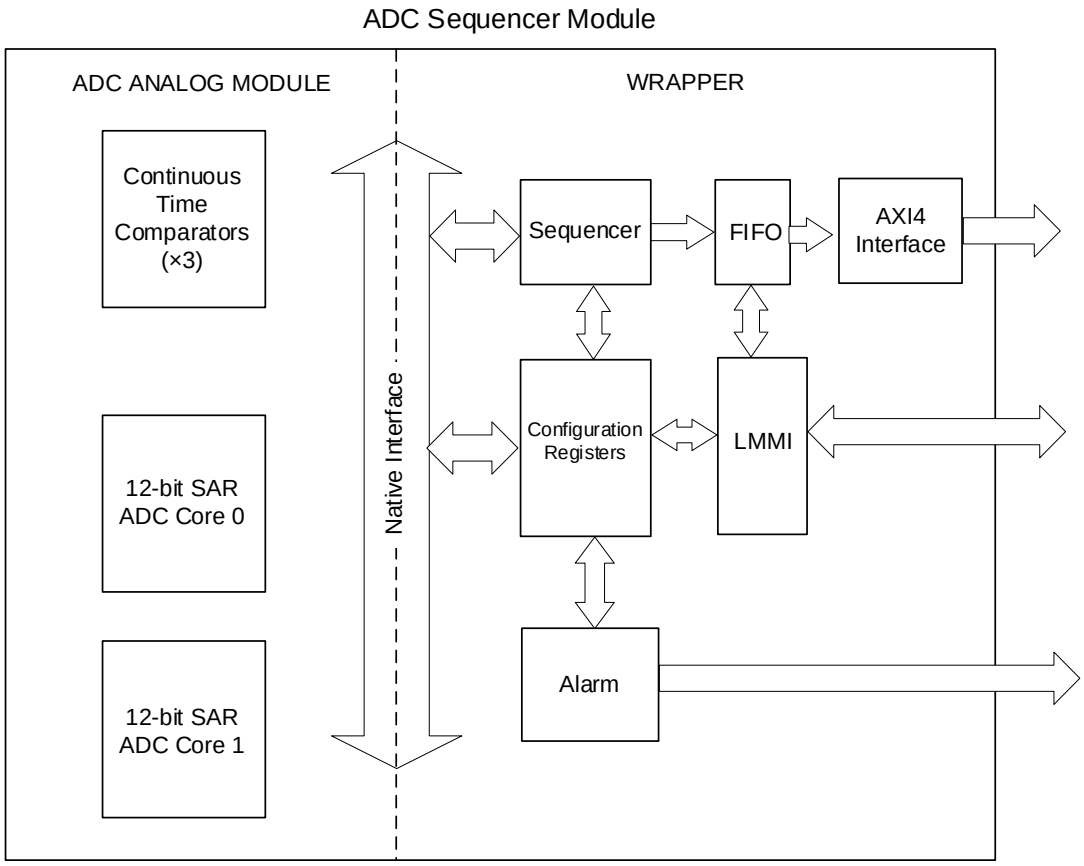

Figure 2.1. ADC Sequencer Module Top Level Block Diagram

The ADC Sequencer Module functional diagram is presented in Figure 2.2.

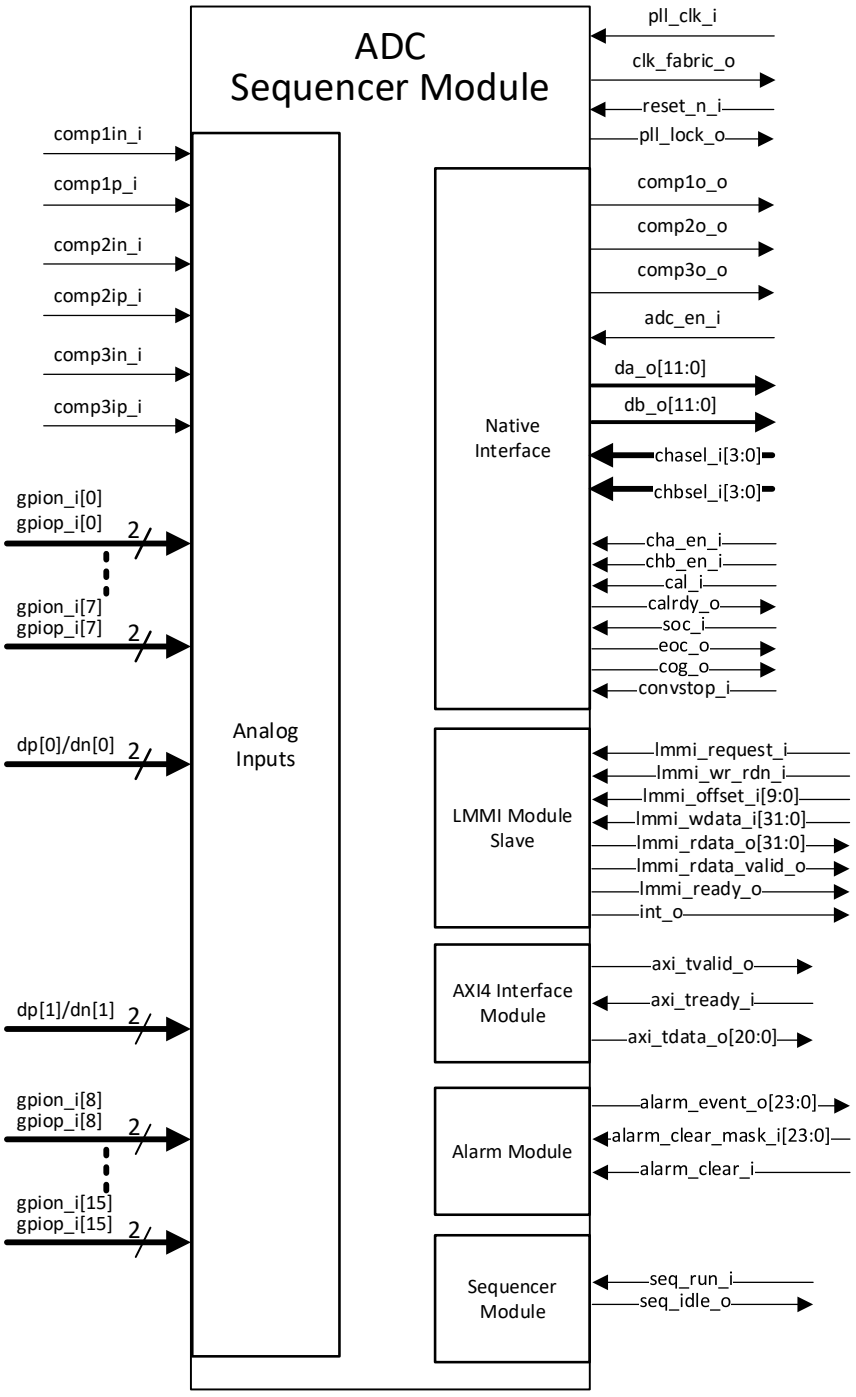

Figure 2.2. ADC Sequencer Module Functional Diagram

2.2. Signal Description

Table 2.1 lists the top-level input and output signals for ADC Sequencer Module.

Table 2.1. ADC Sequencer Module Ports

Port Name	Direction	Level	Description
Clocks and Reset			
pll_clk_i	In	Digital	PLL Clock input to ADC macro.
clk_fabric_o	Out	Digital	Clock output to fabric (clock conversion purpose).
reset_n_i	In	Digital	The ADC initialized with reset_n_i deassertion.
LMMI Interface			
lmmi_request_i	In	Digital	Start transaction.
lmmi_wr_rdn_i	In	Digital	Write = '1', Read = '0'
lmmi_offset_i[9:0]	In	Digital	Register offset, starting at offset 0
lmmi_wdata_i[31:0]	In	Digital	Output data bus.
lmmi_rdata_o[31:0]	Out	Digital	Input data bus.
lmmi_rdata_valid_o	Out	Digital	Read transaction is complete and lmmi_rdata_o[20:0] contains valid data.
lmmi_ready_o	Out	Digital	IP is ready to start a new transaction.
int_o	Out	Digital	Interrupt, active high, level sensitive. Stays high as long as any enabled interrupt is pending. This signal is optional when local interface used is either Native or APB.
Native Interface			
gpiop_io[NUM_PIN[1]-1:0]	In/Out	Analog	Positive input/output ports.
gpion_io[NUM_PIN[1]-1:0]	In/Out	Analog	Negative input/output ports.
dp_i[1:0]	In	Analog	Designated analog input positive ports.
dn_i[1:0]	In	Analog	Designated analog input negative ports.
adc_en_i	In	Digital	ADC enable.
adc_sel_i	In	Digital	ADC Core select. When set to 0, ADC0 is selected as output for axi_tdata_o; else ADC1 is selected. This signal is available only when Native interface is used and both ADC0 and ADC1 are enabled.
da_o[11:0]	Out	Digital	12-bit ADC channel A output.
db_o[11:0]	Out	Digital	12-bit ADC channel B output.
chasel_i[3:0]	In	Digital	Channel A ADC input selection.
chbsel_i[3:0]	In	Digital	Channel B ADC input selection.
cha_en_i	In	Digital	Ch. A enable.
chb_en_i	In	Digital	Ch. B enable.
soc_i	In	Digital	Start of conversion.
eoc_o	Out	Digital	End of conversion.
cog_o	Out	Digital	Conversion on-going signal.
convstop_i	In	Digital	Stop on-going conversion control.
cal_i	In	Digital	Calibration start.
calrdy_o	Out	Digital	End of calibration.
comp1ip_io	In/Out	Analog	1st comparator positive external bonding input/output.
comp1in_io	In/Out	Analog	1st comparator negative external bonding input/output.
comp2ip_io	In/Out	Analog	2nd comparator positive external bonding input/output.
comp2in_io	In/Out	Analog	2nd comparator negative external bonding input/output.
comp3ip_io	In/Out	Analog	3rd comparator positive external bonding input/output.
comp3in_io	In/Out	Analog	3rd comparator negative external bonding input/output.
comp1o_o	Out	Digital	1st comparator output.

Port Name	Direction	Level	Description
comp2o_o	Out	Digital	2nd comparator output.
comp3o_o	Out	Digital	3rd comparator output.
General			
pll_lock_o	Out	Digital	PLL lock output signal
AXI4 Stream Master			
axi_tvalid_o	Out	Digital	Flow control output. The signal goes high, when the transmitter is ready to send data.
axi_tready_i	In	Digital	Flow control input. The signal goes high, when the receive side of an AXI stream is ready.
axi_tdata_o[20:0]	Out	Digital	Output data flow, which concatenates 5-bits ADC input channel address, digitized 12-bit ADC output and extra 4-bits.
Sequencer			
seq_run_i	In	Digital	Runs the Sequencer for Single Pass mode.
seq_idle_o	Out	Digital	Indicates the idle state of the Sequencer
Alarm Function			
alarm_event_o[23:0]	Out	Digital	Over/Under Voltage/Temperature Alarm detection. This signal is optional when local interface used is either LMMI or APB.
alarm_clear_mask_i[23:0]	In	Digital	Mask of Detected Alarms to be cleared.
alarm_clear_i	In	Digital	Detected Alarm clear.
APB Interface			
apb_paddr_i[9:0]	In	Digital	Address of selected register
apb_penable_i	In	Digital	When set to 1, means the IP would go to the setup phase
apb_psel_i	In	Digital	When set to 1, the IP is currently selected
apb_pwdata_i[31:0]	In	Digital	Write data
apb_pwrite_i	In	Digital	When set to 1, a write transaction would be initiated, else a read.
apb_prdata_o[31:0]	Out	Digital	Read data
apb_pready_o	Out	Digital	When asserted, this means that the IP is ready
apb_pslverr_o	Out	Digital	When asserted with apb_pready_o, this means the IP has encountered an error.

Note:

1. Refer to attribute *Number of ADC pairs*. LIFCL-40 [access for 0-15], LIFCL-17 [access for 0,1,2,3,5,6,7,8,9,13,14 only].

2.3. Attribute Summary

Table 2.2 provides the list of user-configurable attributes for ADC Sequencer Module. The attributes are specified using ADC Sequencer Module Configuration user interface in Lattice Radiant.

Table 2.2. Attribute Table

User Interface Config. Tab	Sub-tab	Attribute	Selectable Values	Default	Dependency on other Attributes	Additional Requirements
General	Setup	Number of ADC pairs	(1 to 16/11 *<depending on device>)*	1	—	—
		ADC0 Enable	Checked, Unchecked	Unchecked	—	—
		ADC0 Reference Voltage Select	Internal, External	Internal	ADC0 Enable = “Checked”	—
		ADC0 External Reference Voltage	1.0 to 1.8, in 0.1 increments	1.8	ADC0 Enable = “Checked” and ADC0 Reference Voltage Select = “External”	—
		ADC0 Conversion Mode	Bi-Polar, Uni-Polar	Bi-Polar	ADC0 Enable = “Checked”	—
		ADC1 Enable	Checked, Unchecked	Unchecked		—
		ADC1 Reference Voltage Select	Internal, External	Internal	ADC1 Enable = “Checked”	—
		ADC1 External Reference Voltage	1.0 to 1.8, in 0.1 increments	1.8	ADC1 Enable = “Checked” and ADC1 Reference Voltage Select = “External”	—
		ADC1 Conversion Mode	Bi-Polar, Uni-Polar	Bi-Polar	ADC1 Enable = “Checked”	—
		Readout Data FIFO Depth	16, 32, 54, 128, 256, 512	16	ADC0 Enable = “Checked” || ADC1 Enable = “Checked”	—
		VCC Monitor Enable	Checked, Unchecked	Unchecked	—	—
		VCC Voltage	0.9, 1.0	1.0	—	—
		VCCAUX Monitor Enable	Checked, Unchecked	Unchecked	—	—
		Internal VCCM Monitor Enable	Checked, Unchecked	Unchecked	—	—
		VCCIO0 Monitor Enable	Checked, Unchecked	Unchecked	—	—
		VCCIO0 Voltage	1.8, 2.5, 3.3	2.5	—	—
		VCCIO1 Monitor Enable	Checked, Unchecked	Unchecked	—	—
		VCCIO1 Voltage	1.8, 2.5, 3.3	2.5	—	—
		DTR Monitor Enable	Checked, Unchecked	Unchecked	—	—
		COMP0 Enable	Checked, Unchecked	Unchecked	—	—

User Interface Config. Tab	Sub-tab	Attribute	Selectable Values	Default	Dependency on other Attributes	Additional Requirements
		COMP0 Input Source Select	COMP0 Input, GPIO0 Input	COMP0 Input	—	—
		COMP1 Enable	Checked, Unchecked	Unchecked	—	—
		COMP1 Input Source Select	COMP1 Input, GPIO1 Input	COMP1 Input	—	—
		COMP2 Enable	Checked, Unchecked	Unchecked	—	—
		COMP2 Input Source Select	COMP2 Input, GPIO2 Input	COMP2 Input	—	—
	Interface Configuration	Reference Clock Frequency	10–300 MHz	100 MHz	—	—
		ADC Converter Block Clock Frequency	20–40 MHz	25 MHz	—	—
		ADC Converter Block Clock Multiplier	x2, x4, x6, x8, x10, x12, x14, x16, x18, x20, x22, x24, x26, x28, x30, x32, x34, x36, x38, x40	x4	—	—
		ADC Logic Block Clock Frequency (MHz)	—	100 MHz	Value equals Block Clock Frequency multiplied by Block Clock Multiplier. This value is not editable, and is used for information only.	—
		Local User Interface	Native, LMMI, APB	Native	—	—
		Interrupt Enable	Checked, Unchecked	Unchecked	Hidden when Local User Interface = LMMI	—
		Alarm Event Enable	Checked, Unchecked	Unchecked	Hidden when Local User Interface = Native or no ADC Channel Alarms are enabled	—
ADC Channels	ADC0 GPIO<0-7>/DPIO0 Channel Configuration	Channel Enable	Checked, Unchecked	Unchecked	Channels associated with COMPx that is enabled is grayed out and shown Unchecked	—
		Minimum Sampling Time (cycles)	4–128	4	Channel Enable = “Checked”	—
		Number of Samples to Average on each Conversion	1–4	1	Channel Enable = “Checked”	—

User Interface Config. Tab	Sub-tab	Attribute	Selectable Values	Default	Dependency on other Attributes	Additional Requirements
		Number of Conversion to Average on Each Readout	1–4	1	Channel Enable = “Checked”	—
	ADC1 GPIO<8-15>/DPIO1 Channel Configuration	Channel Enable	Checked, Unchecked	Unchecked	Channels associated with COMPx that is enabled is grayed out and shown Unchecked	—
		Minimum Sampling Time (cycles)	4–128	4	Channel Enable = “Checked”	—
		Number of Samples to Average on each Conversion	1–4	1	Channel Enable = “Checked”	—
		Number of Conversion to Average on Each Readout	1–4	1	Channel Enable = “Checked”	—
Internal Channels	Internal VCC Channel Configuration	Channel Enable	Checked, Unchecked	Unchecked	—	—
		Minimum Sampling Time (cycles)	4–128	16	Channel Enable = “Checked”	—
		Number of Samples to Average on Each Conversion	1–4	2	Channel Enable = “Checked”	—
		Number of Conversion to Average on Each Readout Data	1– 4	4	Channel Enable = “Checked”	—
	Internal VCCAUX Channel Configuration	Channel Enable	Checked, Unchecked	Unchecked		—
		Minimum Sampling Time (cycles)	4–128	16	Channel Enable = “Checked”	—
		Number of Samples to Average on Each Conversion	1–4	2	Channel Enable = “Checked”	—
		Number of Conversion to Average on Each Readout Data	1–4	4	Channel Enable = “Checked”	—
	Internal VCCM Channel Configuration	Channel Enable	Checked, Unchecked	Unchecked	—	—
		Minimum Sampling Time (cycles)	4–128	16	Channel Enable = “Checked”	—
		Number of Samples to Average on Each Conversion	1–4	2	Channel Enable = “Checked”	—

User Interface Config. Tab	Sub-tab	Attribute	Selectable Values	Default	Dependency on other Attributes	Additional Requirements
		Number of Conversion to Average on Each Readout Data	1–4	4	Channel Enable = “Checked”	—
	Internal VCCIO0 Channel Configuration	Channel Enable	Checked, Unchecked	Unchecked	—	—
		Minimum Sampling Time (cycles)	4–128	16	Channel Enable = “Checked”	—
		Number of Samples to Average on Each Conversion	1–4	2	Channel Enable = “Checked”	—
	Internal VCCIO1 Channel Configuration	Channel Enable	Checked, Unchecked	Unchecked		—
		Minimum Sampling Time (cycles)	4–128	16	Channel Enable = “Checked”	—
		Number of Samples to Average on Each Conversion	1 –4	2	Channel Enable = “Checked”	—
		Number of Conversion to Average on Each Readout Data	1–4	4	Channel Enable = “Checked”	—
	Internal DTR Channel Configuration	Channel Enable	Checked, Unchecked	Unchecked	—	—
		Minimum Sampling Time (cycles)	4–128	16	Channel Enable = “Checked”	—
		Number of Samples to Average on Each Conversion	1–4	2	Channel Enable = “Checked”	—
		Number of Conversion to Average on Each Readout Data	1–4	4	Channel Enable = “Checked”	—
		Number of Conversion to Average on Each Readout Data	1–4	4	Channel Enable = “Checked”	—
Sequencer	Sequencer Configuration	Sequencer Enable	Checked, Unchecked	Unchecked	—	When Unchecked, all configuration in the tab would be greyed out
		Continuously Cycling on Configured Sequence	Continuous, Single Pass	Continuous	Sequencer Enable = “Checked”	—
		Configure Sequence Number	1–16	1	Sequencer Enable = “Checked”	—
	Sequence Conversion Step 1	ADC0 Channel Select	blank, GPIO<0-7>, DPIO0, VCC, VCCM, VCCAUX	blank	Sequencer Enable = “Checked”	Sets channel to be converted for Sequence Number n; n = “Configuring

User Interface Config. Tab	Sub-tab	Attribute	Selectable Values	Default	Dependency on other Attributes	Additional Requirements
						Sequence Number” blank = that ADC does not perform conversion blank in both ADCs signify the end of the sequence
		ADC1 Channel Select	blank, GPIO<8-15>, DPIO1, VCCIO0, VCCIO1, DTR	blank	Sequencer Enable = “Checked”	—
		Repeat Step Number of Times	1–128	1	Sequencer Enable = “Checked”	Repeat this specified number of times, before next conversion step
	Sequence Conversion Step 2	ADC0 Channel Select	blank, GPIO<0-7>, DPIO0, VCC, VCCM, VCCAUX	blank	Sequencer Enable = “Checked”	Sets channel to be converted for Sequence Number n; n = “Configuring Sequence Number” blank = that ADC does not perform conversion blank in both ADCs signify the end of the sequence
		ADC1 Channel Select	blank, GPIO<8-15>, DPIO1, VCCIO0, VCCIO1, DTR	blank	Sequencer Enable = “Checked”	—
		Repeat Step Number of Times	1–128	1	Sequencer Enable = “Checked”	Repeat this specified number of times, before next conversion step
	Sequence Conversion Step 3	ADC0 Channel Select	blank, GPIO<0-7>, DPIO0, VCC, VCCM, VCCAUX	blank	Sequencer Enable = “Checked”	Sets channel to be converted for Sequence Number n; n = “Configuring Sequence Number” blank = that ADC does not perform conversion

User Interface Config. Tab	Sub-tab	Attribute	Selectable Values	Default	Dependency on other Attributes	Additional Requirements
						blank in both ADCs signify the end of the sequence
		ADC1 Channel Select	blank, GPIO<8-15>, DPIO1, VCCIO0, VCCIO1, DTR	blank	Sequencer Enable = “Checked”	—
		Repeat Step Number of Times	1 to 128	1	Sequencer Enable = “Checked”	Repeat this specified number of times, before next conversion step
	Sequence Conversion Step 4	ADC0 Channel Select	blank, GPIO<0-7>, DPIO0, VCC, VCCM, VCCAUX	blank	Sequencer Enable = “Checked”	Sets channel to be converted for Sequence Number n; n = “Configuring Sequence Number” blank = that ADC does not perform conversion blank in both ADCs signify the end of the sequence
		ADC1 Channel Select	blank, GPIO<8-15>, DPIO1, VCCIO0, VCCIO1, DTR	blank	Sequencer Enable = “Checked”	—
		Repeat Step Number of Times	1–128	1	Sequencer Enable = “Checked”	Repeat this specified number of times, before next conversion step
	Sequence Conversion Step 5	ADC0 Channel Select	blank, GPIO<0-7>, DPIO0, VCC, VCCM, VCCAUX	blank	Sequencer Enable = “Checked”	Sets channel to be converted for Sequence Number n; n = “Configuring Sequence Number” blank = that ADC does not perform conversion blank in both ADCs signify the end of the sequence
		ADC1 Channel	blank, GPIO<8-	blank	Sequencer Enable =	—

User Interface Config. Tab	Sub-tab	Attribute	Selectable Values	Default	Dependency on other Attributes	Additional Requirements
		Select	15>, DPIO1, VCCIO0, VCCIO1, DTR		"Checked"	
		Repeat Step Number of Times	1–128	1	Sequencer Enable = "Checked"	Repeat this specified number of times, before next conversion step
	Sequence Conversion Step 6	ADC0 Channel Select	blank, GPIO<0-7>, DPIO0, VCC, VCCM, VCCAUX	blank	Sequencer Enable = "Checked"	Sets channel to be converted for Sequence Number n; n = "Configuring Sequence Number" blank = that ADC does not perform conversion blank in both ADCs signify the end of the sequence
		ADC1 Channel Select	blank, GPIO<8-15>, DPIO1, VCCIO0, VCCIO1, DTR	blank	Sequencer Enable = "Checked"	—
		Repeat Step Number of Times	1–128	1	Sequencer Enable = "Checked"	Repeat this specified number of times, before next conversion step
	Sequence Conversion Step 7	ADC0 Channel Select	blank, GPIO<0-7>, DPIO0, VCC, VCCM, VCCAUX	blank	Sequencer Enable = "Checked"	Sets channel to be converted for Sequence Number n; n = "Configuring Sequence Number" blank = that ADC does not perform conversion blank in both ADCs signify end of the sequence
		ADC1 Channel Select	blank, GPIO<8-15>, DPIO1, VCCIO0, VCCIO1, DTR	blank	Sequencer Enable = "Checked"	—

User Interface Config. Tab	Sub-tab	Attribute	Selectable Values	Default	Dependency on other Attributes	Additional Requirements
		Repeat Step Number of Times	1–128	1	Sequencer Enable = “Checked”	Repeat this specified number of times, before next conversion step
	Sequence Conversion Step 8	ADC0 Channel Select	blank, GPIO<0-7>, DPIO0, VCC, VCCM, VCCAUX	blank	Sequencer Enable = “Checked”	Sets channel to be converted for Sequence Number n; n = “Configuring Sequence Number” blank = that ADC does not perform conversion blank in both ADCs signify the end of the sequence
		ADC1 Channel Select	blank, GPIO<8-15>, DPIO1, VCCIO0, VCCIO1, DTR	blank	Sequencer Enable = “Checked”	—
		Repeat Step Number of Times	1–128	1	Sequencer Enable = “Checked”	Repeat this specified number of times, before next conversion step
	Sequence Conversion Step 9	ADC0 Channel Select	blank, GPIO<0-7>, DPIO0, VCC, VCCM, VCCAUX	blank	Sequencer Enable = “Checked”	Sets channel to be converted for Sequence Number n; n = “Configuring Sequence Number” blank = that ADC does not perform conversion blank in both ADCs signify the end of the sequence
		ADC1 Channel Select	blank, GPIO<8-15>, DPIO1, VCCIO0, VCCIO1, DTR	blank	Sequencer Enable = “Checked”	—
		Repeat Step Number of Times	1–128	1	Sequencer Enable = “Checked”	Repeat this specified number of times, before next conversion step

User Interface Config. Tab	Sub-tab	Attribute	Selectable Values	Default	Dependency on other Attributes	Additional Requirements
	Sequence Conversion Step 10	ADC0 Channel Select	blank, GPIO<0-7>, DPIO0, VCC, VCCM, VCCAUX	blank	Sequencer Enable = “Checked”	Sets channel to be converted for Sequence Number n; n = “Configuring Sequence Number” blank = that ADC does not perform conversion blank in both ADCs signify the end of the sequence
		ADC1 Channel Select	blank, GPIO<8-15>, DPIO1, VCCIO0, VCCIO1, DTR	blank	Sequencer Enable = “Checked”	—
		Repeat Step Number of Times	1–128	1	Sequencer Enable = “Checked”	Repeat this specified number of times, before next conversion step
	Sequence Conversion Step 11	ADC0 Channel Select	blank, GPIO<0-7>, DPIO0, VCC, VCCM, VCCAUX	blank	Sequencer Enable = “Checked”	Sets channel to be converted for Sequence Number n; n = “Configuring Sequence Number” blank = that ADC does not perform conversion blank in both ADCs signify the end of the sequence
		ADC1 Channel Select	blank, GPIO<8-15>, DPIO1, VCCIO0, VCCIO1, DTR	blank	Sequencer Enable = “Checked”	—
		Repeat Step Number of Times	1–128	1	Sequencer Enable = “Checked”	Repeat this specified number of times, before next conversion step
	Sequence Conversion Step 12	ADC0 Channel Select	blank, GPIO<0-7>, DPIO0, VCC, VCCM, VCCAUX	blank	Sequencer Enable = “Checked”	Sets channel to be converted for Sequence Number n; n = “Configuring

User Interface Config. Tab	Sub-tab	Attribute	Selectable Values	Default	Dependency on other Attributes	Additional Requirements
						Sequence Number" blank = that ADC does not perform conversion blank in both ADCs signify the end of the sequence Repeat this specified number of times, before next conversion step
		ADC1 Channel Select	blank, GPIO<8-15>, DPIO1, VCCIO0, VCCIO1, DTR	blank	Sequencer Enable = "Checked"	—
		Repeat Step Number of Times	1–128	1	Sequencer Enable = "Checked"	—
	Sequence Conversion Step 13	ADC0 Channel Select	blank, GPIO<0-7>, DPIO0, VCC, VCCM, VCCAUX	blank	Sequencer Enable = "Checked"	Sets channel to be converted for Sequence Number n; n = "Configuring Sequence Number" blank = that ADC does not perform conversion blank in both ADCs signify the end of the sequence
		ADC1 Channel Select	blank, GPIO<8-15>, DPIO1, VCCIO0, VCCIO1, DTR	blank	Sequencer Enable = "Checked"	—
		Repeat Step Number of Times	1–128	1	Sequencer Enable = "Checked"	Repeat this specified number of times, before next conversion step
	Sequence Conversion Step 14	ADC0 Channel Select	blank, GPIO<0-7>, DPIO0, VCC, VCCM, VCCAUX	blank	Sequencer Enable = "Checked"	Sets channel to be converted for Sequence Number n; n = "Configuring Sequence Number"

User Interface Config. Tab	Sub-tab	Attribute	Selectable Values	Default	Dependency on other Attributes	Additional Requirements
						blank = that ADC does not perform conversion blank in both ADCs signify the end of the sequence
		ADC1 Channel Select	blank, GPIO<8-15>, DPIO1, VCCIO0, VCCIO1, DTR	blank	Sequencer Enable = “Checked”	—
		Repeat Step Number of Times	1–128	1	Sequencer Enable = “Checked”	Repeat this specified number of times, before next conversion step
	Sequence Conversion Step 15	ADC0 Channel Select	blank, GPIO<0-7>, DPIO0, VCC, VCCM, VCCAUX	blank	Sequencer Enable = “Checked”	Sets channel to be converted for Sequence Number n; n = “Configuring Sequence Number” blank = that ADC does not perform conversion blank in both ADCs signify the end of the sequence
		ADC1 Channel Select	blank, GPIO<8-15>, DPIO1, VCCIO0, VCCIO1, DTR	blank	Sequencer Enable = “Checked”	—
		Repeat Step Number of Times	1–128	1	Sequencer Enable = “Checked”	Repeat this specified number of times, before next conversion step

User Interface Config. Tab	Sub-tab	Attribute	Selectable Values	Default	Dependency on other Attributes	Additional Requirements
	Sequence Conversion Step 16	ADC0 Channel Select	blank, GPIO<0-7>, DPIO0, VCC, VCCM, VCCAUX	blank	Sequencer Enable = “Checked”	Sets channel to be converted for Sequence Number n; n = “Configuring Sequence Number” blank = that ADC does not perform conversion blank in both ADCs signify the end of the sequence
		ADC1 Channel Select	blank, GPIO<8-15>, DPIO1, VCCIO0, VCCIO1, DTR	blank	Sequencer Enable = “Checked”	—
		Repeat Step Number of Times	1–128	1	Sequencer Enable = “Checked”	Repeat this specified number of times, before next conversion step
	Nesting Sequence Step 1	Sequence Number Select	blank, 1 to 16	blank	Sequence Enable = “Checked”	Blank signify end of the nesting sequence
		Repeat Sequence Number of Times	1–16	1	Sequence Enable = “Checked”	Repeat this specified sequence number of times, before next sequence step
	Nesting Sequence Step 2	Sequence Number Select	blank, 1–16	blank	Sequence Enable = “Checked”	Blank signify end of the nesting sequence
		Repeat Sequence Number of Times	1–16	1	Sequence Enable = “Checked”	Repeat this specified sequence number of times, before next sequence step
	Nesting Sequence Step 3	Sequence Number Select	blank, 1–16	blank	Sequence Enable = “Checked”	Blank signify end of the nesting sequence
		Repeat Sequence Number of Times	1–16	1	Sequence Enable = “Checked”	Repeat this specified sequence number of times, before next sequence step
	Nesting Sequence Step 4	Sequence Number Select	blank, 1–16	blank	Sequence Enable = “Checked”	Blank signify end of the nesting sequence

User Interface Config. Tab	Sub-tab	Attribute	Selectable Values	Default	Dependency on other Attributes	Additional Requirements
		Repeat Sequence Number of Times	1–16	1	Sequence Enable = “Checked”	Repeat this specified sequence number of times, before next sequence step
	Nesting Sequence Step 5	Sequence Number Select	blank, 1–16	blank	Sequence Enable = “Checked”	Blank signify end of the nesting sequence
		Repeat Sequence Number of Times	1–16	1	Sequence Enable = “Checked”	Repeat this specified sequence number of times, before next sequence step
	Nesting Sequence Step 6	Sequence Number Select	blank, 1–16	blank	Sequence Enable = “Checked”	Blank signify end of the nesting sequence
		Repeat Sequence Number of Times	1–16	1	Sequence Enable = “Checked”	Repeat this specified sequence number of times, before next sequence step
ADC Channel Alarms	ADC0 GPIO<0-7>/DPIO0 Alarms Configuration	Over Voltage Alarm Enable	Checked, Unchecked	Unchecked		—
		Over Voltage Alarm Limit (V)	0 to Vref, in 0.1 increments	Vref	Over Voltage Alarm Enable = “Checked”	—
		Number of Consecutive Over Voltage Limit Events to Set Alarm	1–4	1	Over Voltage Alarm Enable = “Checked”	—
		Set Over Voltage Alarm Output Sticky	Yes, No	No	Over Voltage Alarm Enable = “Checked”	—
		Under Voltage Alarm Enable	Checked, Unchecked	Unchecked		—
		Under Voltage Alarm Limit (V)	0 to Vref, in 0.1 increments	0	Under Voltage Alarm Enable = “Checked”	—
		Number of Consecutive Under Voltage Limit Events to Set Alarm	1–4	1	Under Voltage Alarm Enable = “Checked”	—
		Set Under Voltage Alarm Output Sticky	Yes, No	No	Under Voltage Alarm Enable = “Checked”	—
	ADC1 GPIO<8-15>/DPIO1 Alarms Configuration	Over Voltage Alarm Enable	Checked, Unchecked	Unchecked	—	—
		Over Voltage Alarm Limit	0 to Vref, in 0.1 increments	Vref	Over Voltage Alarm Enable = “Checked”	—
		Number of Consecutive Over Voltage Limit Events to Set Alarm	1–4	1	Over Voltage Alarm Enable = “Checked”	—

User Interface Config. Tab	Sub-tab	Attribute	Selectable Values	Default	Dependency on other Attributes	Additional Requirements
		Set Over Voltage Alarm Output Sticky	Yes, No	No	Over Voltage Alarm Enable = “Checked”	—
		Under Voltage Alarm Enable	Checked, Unchecked	Unchecked		—
		Under Voltage Alarm Limit	0 to Vref, in 0.1 increments	0	Under Voltage Alarm Enable = “Checked”	—
		Number of Consecutive Under Voltage Limit Events to Set Alarm	1–4	1	Under Voltage Alarm Enable = “Checked”	—
		Set Under Voltage Alarm Output Sticky	Yes, No	No	Under Voltage Alarm Enable = “Checked”	—
Internal Channel Alarms	Internal VCC Channel Alarm Configuration	Over Voltage Alarm Enable	Checked, Unchecked	Unchecked		—
		Over Voltage Alarm Limit (%)	+4 to +10	+10	Over Voltage Alarm Enable = “Checked”	—
		Number of Consecutive Over Voltage Limit Events to Set Alarm	1–4	1	Over Voltage Alarm Enable = “Checked”	—
		Set Over Voltage Alarm Output Sticky	Yes, No	No	Over Voltage Alarm Enable = “Checked”	—
		Under Voltage Alarm Enable	Checked, Unchecked	Unchecked		—
		Under Voltage Alarm Limit (%)	-4 to -10	-10	Under Voltage Alarm Enable = “Checked”	—
		Number of Consecutive Under Voltage Limit Events to Set Alarm	1– 4	1	Under Voltage Alarm Enable = “Checked”	—
		Set Under Voltage Alarm Output Sticky	Yes, No	No	Under Voltage Alarm Enable = “Checked”	—
	Internal VCCAUX Channel Alarm Configuration	Over Voltage Alarm Enable	Checked, Unchecked	Unchecked		—
		Over Voltage Alarm Limit	+4% to +10%	+10%	Over Voltage Alarm Enable = “Checked”	—
		Number of Consecutive Over Voltage Limit Events to Set Alarm	1–4	1	Over Voltage Alarm Enable = “Checked”	—
		Set Over Voltage Alarm Output Sticky	Yes, No	No	Over Voltage Alarm Enable = “Checked”	—

User Interface Config. Tab	Sub-tab	Attribute	Selectable Values	Default	Dependency on other Attributes	Additional Requirements
		Under Voltage Alarm Enable	Checked, Unchecked	Unchecked		—
		Under Voltage Alarm Limit	-4% to -10%	-10%	Under Voltage Alarm Enable = “Checked”	—
		Number of Consecutive Under Voltage Limit Events to Set Alarm	1–4	1	Under Voltage Alarm Enable = “Checked”	—
		Set Under Voltage Alarm Output Sticky	Yes, No	No	Under Voltage Alarm Enable = “Checked”	—
	Internal VCCIO0 Channel Alarm Configuration	Over Voltage Alarm Enable	Checked, Unchecked	Unchecked	—	—
		Over Voltage Alarm Limit	+4% to +10%	+10%	Over Voltage Alarm Enable = “Checked”	—
		Number of Consecutive Over Voltage Limit Events to Set Alarm	1–4	1	Over Voltage Alarm Enable = “Checked”	—
		Set Under Voltage Alarm Output Sticky	Yes, No	No	Over Voltage Alarm Enable = “Checked”	—
		Under Voltage Alarm Enable	Checked, Unchecked	Unchecked		—
		Under Voltage Alarm Limit	-4% to -10%	-10%	Under Voltage Alarm Enable = “Checked”	—
		Number of Consecutive Under Voltage Limit Events to Set Alarm	1–4	1	Under Voltage Alarm Enable = “Checked”	—
		Set Under Voltage Alarm Output Sticky	Yes, No	No	Under Voltage Alarm Enable = “Checked”	—
	Internal VCCIO1 Channel Alarm Configuration	Over Voltage Alarm Enable	Checked, Unchecked	Unchecked		—
		Over Voltage Alarm Limit	+4% to +10%	+10%	Over Voltage Alarm Enable = “Checked”	—
		Number of Consecutive Over Voltage Limit Events to Set Alarm	1–4	1	Over Voltage Alarm Enable = “Checked”	—
		Set Over Voltage Alarm Output Sticky	Yes, No	No	Over Voltage Alarm Enable = “Checked”	—
		Under Voltage Alarm Enable	Checked, Unchecked	Unchecked		—
		Under Voltage Alarm Limit	-4% to -10%	-10%	Under Voltage Alarm Enable = “Checked”	—

User Interface Config. Tab	Sub-tab	Attribute	Selectable Values	Default	Dependency on other Attributes	Additional Requirements
		Number of Consecutive Under Voltage Limit Events to Set Alarm	1–4	1	Under Voltage Alarm Enable = “Checked”	—
		Set Under Voltage Alarm Output Sticky	Yes, No	No	Under Voltage Alarm Enable = “Checked”	—
	Internal DTR Channel Alarm Configuration	Over Temperature Alarm Enable	Checked, Unchecked	Unchecked		—
		Over Temperature Alarm Limit	-40 to 125	100	Over Temperature Alarm Enable = “Checked”	—
		Number of Consecutive Over Temperature Limit Events to Set Alarm	1–4	1	Over Temperature Alarm Enable = “Checked”	—
		Set Over Voltage Temp Output Sticky	Yes, No	No	Over Temperature Alarm Enable = “Checked”	—
		Over Temperature Alarm Enable	Checked, Unchecked	Unchecked		—
		Under Temperature Alarm Limit	-40°C–125°C	-10°C–100°C	Under Temperature Alarm Enable = “Checked”	—
		Number of Consecutive Under Temperature Limit Events to Set Alarm	1–4	1	Under Temperature Alarm Enable = “Checked”	—
		Set Under Temp Alarm Output Sticky	Yes, No	No	Under Temperature Alarm Enable = “Checked”	—

2.3.1. Notes to Attributes Settings

2.3.1.1. ADC0 Enable/ADC1 Enable

When in the user interface the ADC0 Enable/ADC1 Enable attribute is “Checked” it enables Channel A/Channel B input. If the ADC0 Enable/ADC1 Enable is not enabled, then the corresponding ADC0/ADC1 cannot be used in Sequencer Module settings.

2.3.1.2. ADC0 Reference Voltage Select/ADC1 Reference Voltage Select

ADC0 Reference Voltage Select/ADC1 Reference Voltage Select attribute in the user interface defines the External/Internal reference voltage block selection. Internal reference is not precise and is mainly used for wafer level functional testing. The Internal reference is not recommended for customer design. An accurate External reference should be used for all customer ADC applications. If the Internal voltage reference is used, then VCCIO0, VCCIO1, and VCCAUX need to operate at 2.5 V or less.

The ADC's reference voltage must be higher than or equal to any voltage applied to any of the channel inputs. This includes the divided-down power supply monitoring channels. If the reference voltage is as little as 0.1 V lower than an applied input, then the ADC result from all channels becomes unreliable.

2.3.1.3. ADC0 External Reference Voltage/ADC1 External Reference Voltage

ADC0 External Reference Voltage/ADC1 External Reference Voltage is used for alarm generation. When in the user interface. ADC0 Enable/ADC1 Enable is *Checked* and the ADC0 Reference Voltage Select/ADC1 Reference Voltage Select is selected *External* then ADC0 External Reference Voltage/ADC1 External Reference Voltage accepts values from 1.0 V to 1.8 V, in 0.1 increments. The ADC can convert max 1.8 V input signal with 1.8 V reference voltage and input signal can be converted in unipolar mode or bi-polar mode. In case of unipolar mode, positive input signal needs to be higher than negative input.

2.3.1.4. VCC Monitor Enable, VCCAUX Monitor Enable, Internal VCCM Monitor Enable, VCCIO0 Monitor Enable, VCCIO1 Monitor Enable

Enabling the attributes in the user interface sets chasel_i[3:0] and chbsel_i[3:0] in order to provide monitoring of power supply voltages that connected to the respective VMEAS inputs by hard connection. These attributes are used only for alarm generation.

2.3.1.5. VCC Voltage, VCCIO0 Voltage, VCCIO1 Voltage, VCCAUX, VCCM, Temp

The values are set within Internal Channel Select attribute field of Configuration Tab user interface.

The selected value is used in ADC IP alarming function.

2.3.1.6. Reference Clock Frequency, ADC Logic Block Clock Frequency, ADC Logic Block Clock Multiplier, ADC Converter Block Clock Frequency

The PLL setting is set based on the input and output frequency of the PLL. Reference Clock Frequency defines the reference frequency to PLL. ADC Logic Block Clock (clk_dclk_i) Frequency defines the frequency of the PLL output, which is the input clock to ADC IP and calculated as:

DCLK Frequency=ADC Converter Block Core Frequency × ADC Converter Block Core Multiplier

ADC Converter Block Clock Frequency defines the frequency to ADC Converter Core Block. The ADC's sampling period can be programmable to minimize input resistance effect and the ADC macro has a power down feature with minimal leakage for sleep mode.

2.3.1.7. Sequence Configuration

When sequential conversion is selected, input ports' sequence is controlled by Module sequencer. Each ADC input signal is selected among eight GPIO input pairs, one designated analog input pair, and three internal voltage rails as unipolar or bi-polar mode (one of the inputs is assigned for internal junction temperature sensing diode).

2.3.1.8. Alarm Mode

For details on the user interface Configuration Tabs attributes for Alarm Setting Configuration, see Table 2.2.

2.3.1.9. Calibration Mode

Conversion rate for the ADC is varied by varying the input clock rate. The relation between clock rate and conversion rate is defined as:

Conversion Rate = Sampling Rate × (number of required clocks to finish conversion).

The CLK in the following timing diagram equals to clk_fabric for the conversion mode and the other signals show the timing relationship to the fabric (DCLK and clk_fabric are provided by the same PLL). The ADC initialized with reset_n_i deassertion and initial calibration. CALRDY is low after RESETN deassertion and remains low until a first calibration is run. The calibration starts with CAL going high (at least eight clocks after RESETN deassertion). After calibration time, CALRDY goes high indication that the ADC is calibrated. The timing diagram also includes a first conversion starting just after the calibration conclusion.

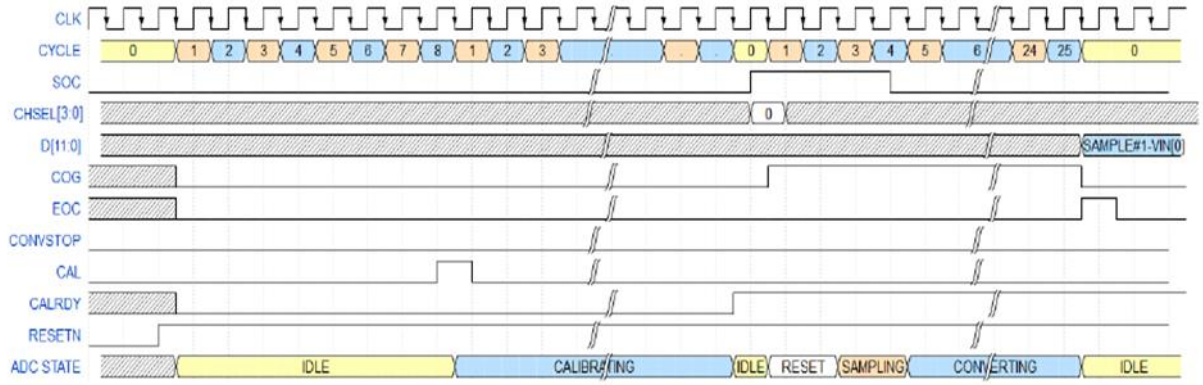

Figure 2.3. Calibration Timing Diagram

2.3.1.10. Conversion Modes

The ADC supports two conversion modes: Continuous conversion mode and Single-Pass conversion mode. In both cases, the SOC (Start-of-Conversion) signal is acquired on CLK falling edge. Then the analog signal tracking is started for minimum two clock cycles after SOC rising edge acquisition. The analog input signal tracking time is controlled by the SOC pulse width, which can have from minimum four clock cycle to unlimited clock cycle. The tracking of analog input signal stops on the CLK falling edge after SOC de-asserted. One ADC conversion takes at least 25 clock cycles corresponding to two clock cycles tracking time and the ADC output data becomes available on CLK falling edge as indicated by the EOC (End of Conversion) signal going high. EOC may go high with some delay after COG (Conversion On-Going) going low. The COG is synchronized to Fabric clock domain and asserted about 5 clock cycle after the SOC assertion. The data remains available until the end of the next conversion and the output data should be sampled on the CLK rising edge when EOC is high.

Two ADCs can sample the input as sequentially or simultaneously and its sampling period is programmable by changing SOC signal period.

Continuous Conversion Mode

Continuous conversion mode is used for continuous signal conversion.

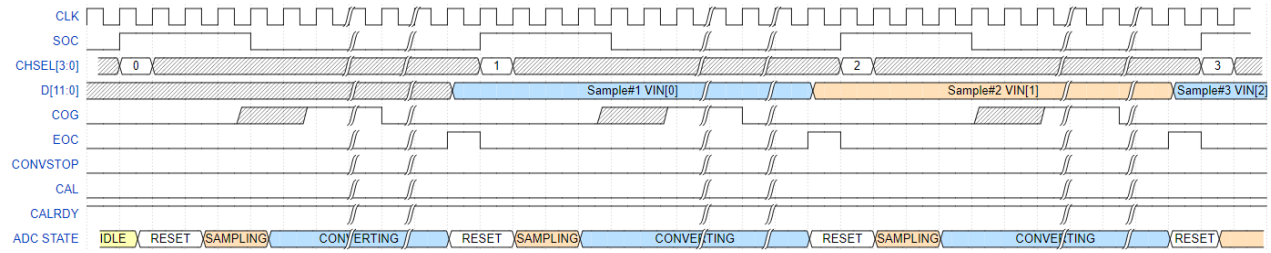

Figure 2.4. Continuous Sampling Mode Timing Diagram

Single-Pass Conversion Mode

Single-Pass conversion mode can be used for individual samples conversion or to reduce the sample rate while keeping the same clock frequency and sampling time. When conversion ends and no SOC pulse is applied, the ADC is put into idle mode with no static current consumption and reduced dynamic current consumption. Clock gating is performed in wrapper side to minimize any dynamic current consumption in idle mode.

Timing diagram in Figure 2.5 shows Single-Pass conversion operation mode considering SOC=1 during four clock cycles (minimum time).

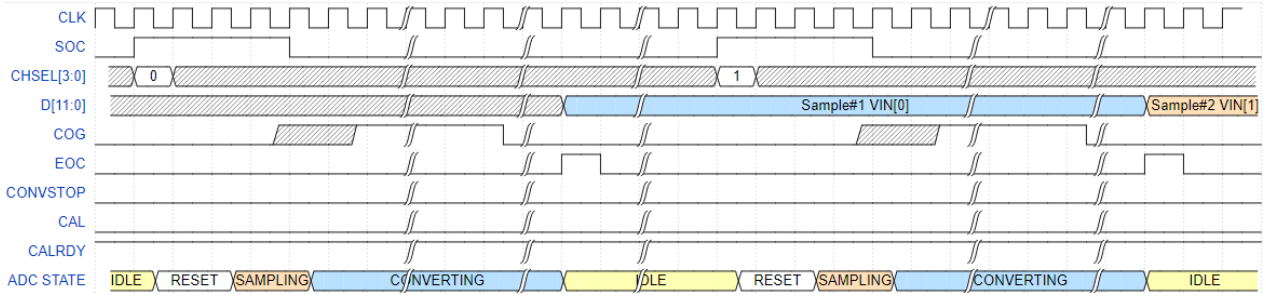

Figure 2.5. Single-Pass Conversion Mode Timing Diagram

2.3.1.11. Conversion Stop Signal

In order to abort an on-going conversion, CONVSTOP (conversion stop) signal can be used as shown in Figure 2.6.

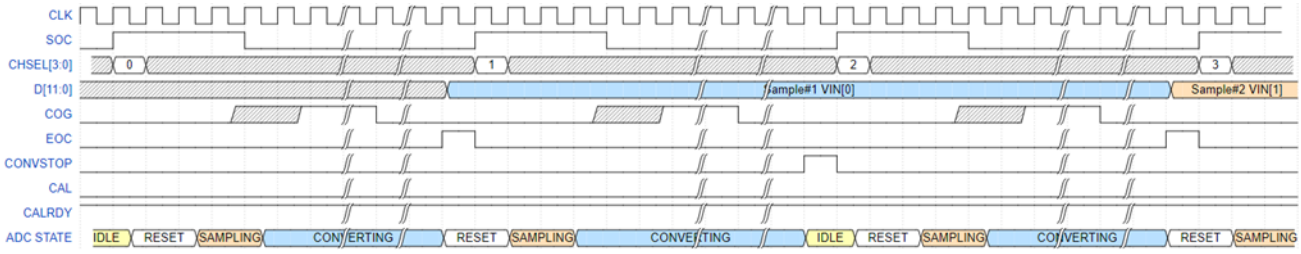

Figure 2.6. CONVSTOP Signal Used to Abort an Ongoing Conversion

2.3.1.12. Programmable Input Signal Sampling Time

ADC's sampling duration can be controlled by changing SOC pulse width. The first conversion has n clock cycles sampling period and the second conversion has the minimum four clock cycles sampling period.

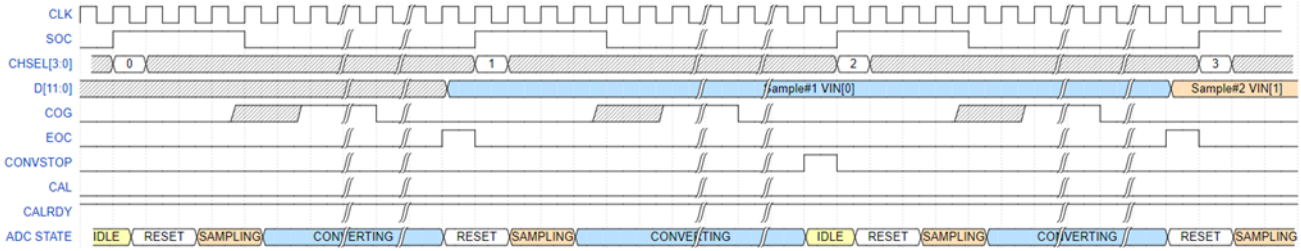

Figure 2.7. Programmable Input Signal Sampling

2.3.1.13. Analog Input Signal and Output Code

Analog input signal conversion to a digital code in bi-polar mode is shown in Figure 2.8.

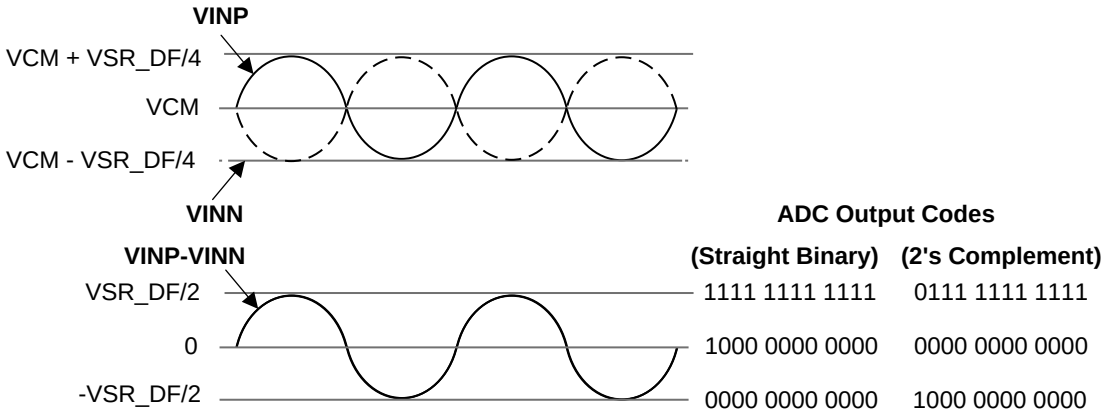

Figure 2.8. Bi-Polar Input Signal and Output Code Example

Analog input signal conversion to a digital code in unipolar mode is shown in Figure 2.9.

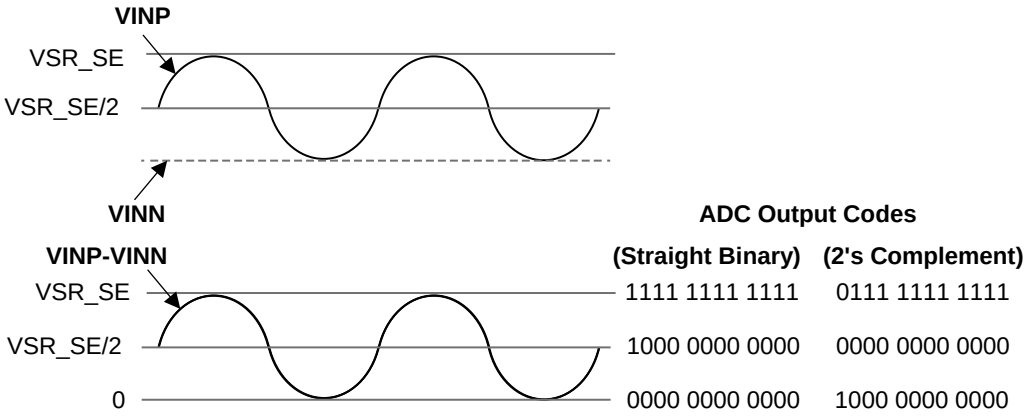

Figure 2.9. Uni-Polar Input Signal and Output Code Example

2.3.1.14. Power Supply Sensor

There are five on-chip power supply sensors that can monitor the FPGA power supply voltages. The sensors can measure VCCIO, VCCAUX, VCC and VCCM on the package power supply balls.

ADC conversion code is given in the following equation:

$$Voltage = \frac{ADC\ output\ code}{4096} \times 3.0V$$

The conversion graph is shown in Figure 2.10.

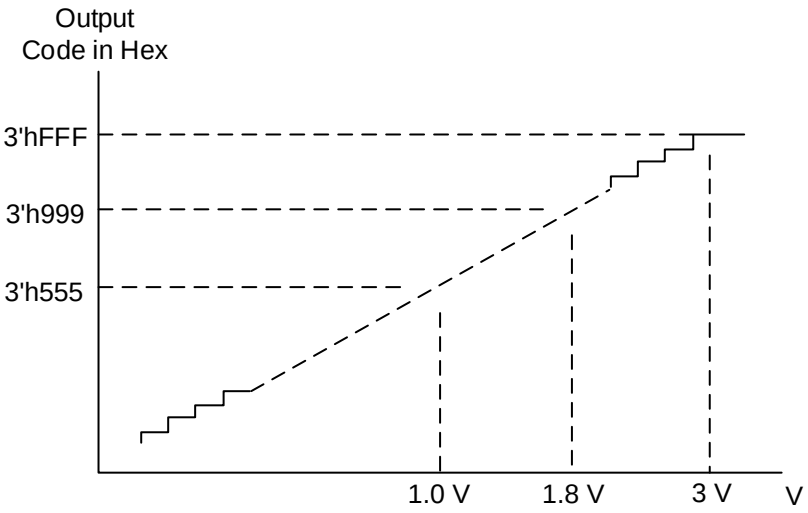

Figure 2.10. Power Supply Voltage Conversion Graph

2.3.1.15. DTR (Digital Temperature Readout)

On-die junction temperature can be monitored using internal PTAT (Proportional to Absolute Temperature) characteristic BJT diode voltage, see Figure 2.11.

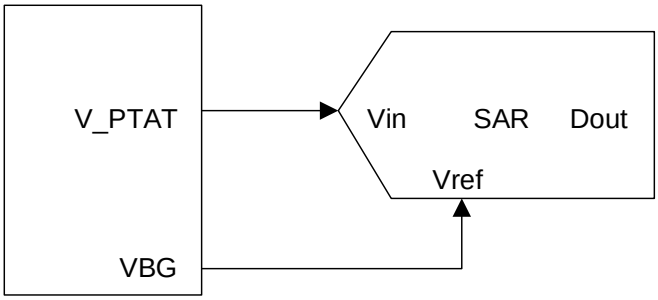

Figure 2.11. Digital Temperature Readout

DTR output is inversely proportional to the following equation:

$$\boldsymbol{Dout} = \frac{\boldsymbol{Vin}}{\boldsymbol{Vref}} \times (\mathbf{2^n - 1})$$

2.4. Register Description

2.4.1. Register Address Map

Table 2.3. Register Address Map

Offset	Register Name	Width	Access	Description
0x001	SETUP_ADC0_EN	1	R/W	When set “1” it enables ADC0.
0x002	SETUP_ADC1_EN	1	R/W	When set “1” it enables ADC1.
0x003	ADC0_CHANNEL_EN	12	R/W	Enables ADC0 channels configuration options. Each bit enables corresponding channel.
0x004	ADC1_CHANNEL_EN	12	R/W	Enables ADC1 channels configuration options. Each bit enables corresponding channel.
0x005	ADC0_CH0_MIN_SMPL_TIME	8	R/W	Defines the minimum sampling time for ADC0 Chanel0. Defines how many clock cycles “SOC” signal is asserted.
0x006	ADC0_CH1_MIN_SMPL_TIME	8	R/W	Defines the minimum sampling time for ADC0 Chanel1. Defines how many clock cycles “SOC” signal is asserted
0x007	ADC0_CH2_MIN_SMPL_TIME	8	R/W	Defines the minimum sampling time for ADC0 Chanel2. Defines how many clock cycles “SOC” signal is asserted.
0x008	ADC0_CH3_MIN_SMPL_TIME	8	R/W	Defines the minimum sampling time for ADC0 Chanel3. Defines how many clock cycles “SOC” signal is asserted.
0x009	ADC0_CH4_MIN_SMPL_TIME	8	R/W	Defines the minimum sampling time for ADC0 Chanel4. Defines how many clock cycles “SOC” signal is asserted.
0x00A	ADC0_CH5_MIN_SMPL_TIME	8	R/W	Defines the minimum sampling time for ADC0 Chanel5. Defines how many clock cycles “SOC” signal is asserted.
0x00B	ADC0_CH6_MIN_SMPL_TIME	8	R/W	Defines the minimum sampling time for ADC0 Chanel6. Defines how many clock cycles “SOC” signal is asserted.
0x00C	ADC0_CH7_MIN_SMPL_TIME	8	R/W	Defines the minimum sampling time for ADC0 Chanel7. Defines how many clock cycles “SOC” signal is asserted.
0x00D	ADC0_CH8_MIN_SMPL_TIME	8	R/W	Defines the minimum sampling time for ADC0 Chanel8. Defines how many clock cycles “SOC” signal is asserted.
0x00E	ADC0_CH9_MIN_SMPL_TIME	8	R/W	Defines the minimum sampling time for ADC0 Chanel9. Defines how many clock cycles “SOC” signal is asserted.
0x00F	ADC0_CH10_MIN_SMPL_TIME	8	R/W	Defines the minimum sampling time for ADC0 Chanel10. Defines how many clock cycles “SOC” signal is asserted.
0x010	ADC0_CH11_MIN_SMPL_TIME	8	R/W	Defines the minimum sampling time for ADC0 Chanel11. Defines how many clock cycles “SOC” signal is asserted.
0x011	ADC1_CH0_MIN_SMPL_TIME	8	R/W	Defines the minimum sampling time for ADC1 Chanel0. Defines how many clock cycles “SOC” signal is asserted.
0x012	ADC1_CH1_MIN_SMPL_TIME	8	R/W	Defines the minimum sampling time for ADC1 Chanel1. Defines how many clock cycles “SOC” signal is asserted.
0x013	ADC1_CH2_MIN_SMPL_TIME	8	R/W	Defines the minimum sampling time for ADC1 Chanel2. Defines how many clock cycles “SOC” signal is asserted.
0x014	ADC1_CH3_MIN_SMPL_TIME	8	R/W	Defines the minimum sampling time for ADC1 Chanel3. Defines how many clock cycles “SOC” signal is asserted.
0x015	ADC1_CH4_MIN_SMPL_TIME	8	R/W	Defines the minimum sampling time for ADC1 Chanel4. Defines how many clock cycles “SOC” signal is asserted.
0x016	ADC1_CH5_MIN_SMPL_TIME	8	R/W	Defines the minimum sampling time for ADC1 Chanel5. Defines how many clock cycles “SOC” signal is asserted.
0x017	ADC1_CH6_MIN_SMPL_TIME	8	R/W	Defines the minimum sampling time for ADC1 Chanel6. Defines how many clock cycles “SOC” signal is asserted.
0x018	ADC1_CH7_MIN_SMPL_TIME	8	R/W	Defines the minimum sampling time for ADC1 Chanel7. Defines how many clock cycles “SOC” signal is asserted.

Offset	Register Name	Width	Access	Description
0x019	ADC1_CH8_MIN_SMPL_TIME	8	R/W	Defines the minimum sampling time for ADC1 Chanel8. Defines how many clock cycles “SOC” signal is asserted.
0x01A	ADC1_CH9_MIN_SMPL_TIME	8	R/W	Defines the minimum sampling time for ADC1 Chanel9. Defines how many clock cycles “SOC” signal is asserted.
0x01B	ADC1_CH10_MIN_SMPL_TIME	8	R/W	Defines the minimum sampling time for ADC1 Chanel10. Defines how many clock cycles “SOC” signal is asserted.
0x01C	ADC1_CH11_MIN_SMPL_TIME	8	R/W	Defines the minimum sampling time for ADC1 Chanel11. Defines how many clock cycles “SOC” signal is asserted.
0x01D	ADC0_CH0_SAMPLES_NUM	3	R/W	Defines the number of samples within one conversion to be averaged for ADC0 Chanel0.
0x01E	ADC0_CH1_SAMPLES_NUM	3	R/W	Defines the number of samples within one conversion to be averaged for ADC0 Chanel1.
0x01F	ADC0_CH2_SAMPLES_NUM	3	R/W	Defines the number of samples within one conversion to be averaged for ADC0 Chanel2.
0x020	ADC0_CH3_SAMPLES_NUM	3	R/W	Defines the number of samples within one conversion to be averaged for ADC0 Chanel3.
0x021	ADC0_CH4_SAMPLES_NUM	3	R/W	Defines the number of samples within one conversion to be averaged for ADC0 Chanel4.
0x022	ADC0_CH5_SAMPLES_NUM	3	R/W	Defines the number of samples within one conversion to be averaged for ADC0 Chanel5.
0x023	ADC0_CH6_SAMPLES_NUM	3	R/W	Defines the number of samples within one conversion to be averaged for ADC0 Chanel6.
0x024	ADC_0_CH_7_SAMPLES_NUM	3	R/W	Defines the number of samples within one conversion to be averaged for ADC0 Chanel7.
0x025	ADC0_CH8_SAMPLES_NUM	3	R/W	Defines the number of samples within one conversion to be averaged for ADC0 Chanel8.
0x026	ADC0_CH9_SAMPLES_NUM	3	R/W	Defines the number of samples within one conversion to be averaged for ADC0 Chanel9.
0x027	ADC0_CH10_SAMPLES_NUM	3	R/W	Defines the number of samples within one conversion to be averaged for ADC0 Chanel10.
0x028	ADC0_CH11_SAMPLES_NUM	3	R/W	Defines the number of samples within one conversion to be averaged for ADC0 Chanel11.
0x029	ADC1_CH0_SAMPLES_NUM	3	R/W	Defines the number of samples within one conversion to be averaged for ADC1 Chanel0.
0x02A	ADC1_CH1_SAMPLES_NUM	3	R/W	Defines the number of samples within one conversion to be averaged for ADC1 Chanel10.
0x02B	ADC1_CH2_SAMPLES_NUM	3	R/W	Defines the number of samples within one conversion to be averaged for ADC1 Chanel2.
0x02C	ADC1_CH3_SAMPLES_NUM	3	R/W	Defines the number of samples within one conversion to be averaged for ADC1 Chanel3.
0x02D	ADC1_CH4_SAMPLES_NUM	3	R/W	Defines the number of samples within one conversion to be averaged for ADC1 Chanel4.
0x02E	ADC1_CH5_SAMPLES_NUM	3	R/W	Defines the number of samples within one conversion to be averaged for ADC1 Chanel5.
0x02F	ADC1_CH6_SAMPLES_NUM	3	R/W	Defines the number of samples within one conversion to be averaged for ADC1 Chanel6.
0x030	ADC1_CH7_SAMPLES_NUM	3	R/W	Defines the number of samples within one conversion to be averaged for ADC1 Chanel7.
0x031	ADC1_CH8_SAMPLES_NUM	3	R/W	Defines the number of samples within one conversion to be averaged for ADC1 Chanel8.

Offset	Register Name	Width	Access	Description
0x032	ADC1_CH9_SAMPLES_NUM	3	R/W	Defines the number of samples within one conversion to be averaged for ADC1 Chanel9.
0x033	ADC1_CH10_SAMPLES_NUM	3	R/W	Defines the number of samples within one conversion to be averaged for ADC1 Chanel10.
0x034	ADC1_CH11_SAMPLES_NUM	3	R/W	Defines the number of samples within one conversion to be averaged for ADC1 Chanel11.
0x035	ADC0_CH0_CONV_NUM	3	R/W	Defines the number of values followed each conversion and which are to be averaged for ADC0 Channel0.
0x036	ADC0_CH1_CONV_NUM	3	R/W	Defines the number of values followed each conversion and which are to be averaged for ADC0 Channel1.
0x037	ADC0_CH2_CONV_NUM	3	R/W	Defines the number of values followed each conversion and which are to be averaged for ADC0 Channel2.
0x038	ADC0_CH3_CONV_NUM	3	R/W	Defines the number of values followed each conversion and which are to be averaged for ADC0 Channel3.
0x039	ADC0_CH4_CONV_NUM	3	R/W	Defines the number of values followed each conversion and which are to be averaged for ADC0 Channel4.
0x03A	ADC0_CH5_CONV_NUM	3	R/W	Defines the number of values followed each conversion and which are to be averaged for ADC0 Channel5.
0x03B	ADC0_CH6_CONV_NUM	3	R/W	Defines the number of values followed each conversion and which are to be averaged for ADC0 Channel6.
0x03C	ADC0_CH7_CONV_NUM	3	R/W	Defines the number of values followed each conversion and which are to be averaged for ADC0 Channel7.
0x03D	ADC0_CH8_CONV_NUM	3	R/W	Defines the number of values followed each conversion and which are to be averaged for ADC0 Channel8.
0x03E	ADC0_CH9_CONV_NUM	3	R/W	Defines the number of values followed each conversion and which are to be averaged for ADC0 Channel9.
0x03F	ADC0_CH10_CONV_NUM	3	R/W	Defines the number of values followed each conversion and which are to be averaged for ADC0 Channel10.
0x040	ADC0_CH11_CONV_NUM	3	R/W	Defines the number of values followed each conversion and which are to be averaged for ADC0 Channel11.
0x041	ADC1_CH0_CONV_NUM	3	R/W	Defines the number of values followed each conversion and which are to be averaged for ADC1 Channel0.
0x042	ADC1_CH1_CONV_NUM	3	R/W	Defines the number of values followed each conversion and which are to be averaged for ADC1 Channel1.
0x043	ADC1_CH2_CONV_NUM	3	R/W	Defines the number of values followed each conversion and which are to be averaged for ADC1 Channel2.
0x044	ADC1_CH3_CONV_NUM	3	R/W	Defines the number of values followed each conversion and which are to be averaged for ADC1 Channel3.
0x045	ADC1_CH4_CONV_NUM	3	R/W	Defines the number of values followed each conversion and which are to be averaged for ADC1 Channel4.
0x046	ADC1_CH5_CONV_NUM	3	R/W	Defines the number of values followed each conversion and which are to be averaged for ADC1 Channel5.
0x047	ADC1_CH6_CONV_NUM	3	R/W	Defines the number of values followed each conversion and which are to be averaged for ADC1 Channel6.
0x048	ADC1_CH7_CONV_NUM	3	R/W	Defines the number of values followed each conversion and which are to be averaged for ADC1 Channel7.
0x049	ADC1_CH8_CONV_NUM	3	R/W	Defines the number of values followed each conversion and which are to be averaged for ADC1 Channel8.
0x04A	ADC1_CH9_CONV_NUM	3	R/W	Defines the number of values followed each conversion and which are to be averaged for ADC1 Channel9.
0x04B	ADC1_CH10_CONV_NUM	3	R/W	Defines the number of values followed each conversion and which are to be averaged for ADC1 Channel10.

Offset	Register Name	Width	Access	Description
0x04C	ADC1_CH11_CONV_NUM	3	R/W	Defines the number of values followed each conversion and which are to be averaged for ADC1 Channel11.
0x04D	SEQ_EN	1	R/W	Enables the Sequencer.
0x04E	SEQ_CFG_CONT_CYC	1	R/W	Defines Sequencer Continuous/Single Pass modes. When “1” Continuous mode, when “0” Single Pass mode.
0x04F	SEQ_CFG_SEQ_NUM	5	R/W	Defines Sequence Conversion Steps number.
0x050	SEQ_RUN	1	R/W	When “1” it runs the Sequencer when Sequencer is set in Single Pass mode.
0x051	SEQ_0_CFG_ADC0_CH_SEL	4	R/W	Defines the appropriate Channel of ADC0 for sequence conversion step1.
0x052	SEQ_1_CFG_ADC0_CH_SEL	4	R/W	Defines the appropriate Channel of ADC0 for sequence conversion step2.
0x053	SEQ_2_CFG_ADC0_CH_SEL	4	R/W	Defines the appropriate Channel of ADC0 for sequence conversion step3.
0x054	SEQ_3_CFG_ADC0_CH_SEL	4	R/W	Defines the appropriate Channel of ADC0 for sequence conversion step4.
0x055	SEQ_4_CFG_ADC0_CH_SEL	4	R/W	Defines the appropriate Channel of ADC0 for sequence conversion step5.
0x056	SEQ_5_CFG_ADC0_CH_SEL	4	R/W	Defines the appropriate Channel of ADC0 for sequence conversion step6.
0x057	SEQ_6_CFG_ADC0_CH_SEL	4	R/W	Defines the appropriate Channel of ADC0 for sequence conversion step7.
0x058	SEQ_7_CFG_ADC0_CH_SEL	4	R/W	Defines the appropriate Channel of ADC0 for sequence conversion step8.
0x059	SEQ_8_CFG_ADC0_CH_SEL	4	R/W	Defines the appropriate Channel of ADC0 for sequence conversion step9.
0x05A	SEQ_9_CFG_ADC0_CH_SEL	4	R/W	Defines the appropriate Channel of ADC0 for sequence conversion step10.
0x05B	SEQ_10_CFG_ADC0_CH_SEL	4	R/W	Defines the appropriate Channel of ADC0 for sequence conversion step11.
0x05C	SEQ_11_CFG_ADC0_CH_SEL	4	R/W	Defines the appropriate Channel of ADC0 for sequence conversion step12.
0x05D	SEQ_12_CFG_ADC0_CH_SEL	4	R/W	Defines the appropriate Channel of ADC0 for sequence conversion step13.
0x05E	SEQ_13_CFG_ADC0_CH_SEL	4	R/W	Defines the appropriate Channel of ADC0 for sequence conversion step14.
0x05F	SEQ_14_CFG_ADC0_CH_SEL	4	R/W	Defines the appropriate Channel of ADC0 for sequence conversion step15.
0x060	SEQ_15_CFG_ADC0_CH_SEL	4	R/W	Defines the appropriate Channel of ADC0 for sequence conversion step16.
0x061	SEQ_0_CFG_ADC1_CH_SEL	4	R/W	Defines the appropriate Channel of ADC1 for sequence conversion step1.
0x062	SEQ_1_CFG_ADC1_CH_SEL	4	R/W	Defines the appropriate Channel of ADC1 for sequence conversion step2.
0x063	SEQ_2_CFG_ADC1_CH_SEL	4	R/W	Defines the appropriate Channel of ADC1 for sequence conversion step3.
0x064	SEQ_3_CFG_ADC1_CH_SEL	4	R/W	Defines the appropriate Channel of ADC1 for sequence conversion step4.
0x065	SEQ_4_CFG_ADC1_CH_SEL	4	R/W	Defines the appropriate Channel of ADC1 for sequence conversion step5.
0x066	SEQ_5_CFG_ADC1_CH_SEL	4	R/W	Defines the appropriate Channel of ADC1 for sequence conversion step6.

Offset	Register Name	Width	Access	Description
0x067	SEQ_6_CFG_ADC1_CH_SEL	4	R/W	Defines the appropriate Channel of ADC1 for sequence conversion step7.
0x068	SEQ_7_CFG_ADC_1_CH_SEL	4	R/W	Defines the appropriate Channel of ADC1 for sequence conversion step8.
0x069	SEQ_8_CFG_ADC1_CH_SEL	4	R/W	Defines the appropriate Channel of ADC1 for sequence conversion step9.
0x06A	SEQ_9_CFG_ADC1_CH_SEL	4	R/W	Defines the appropriate Channel of ADC1 for sequence conversion step10.
0x06B	SEQ_10_CFG_ADC1_CH_SEL	4	R/W	Defines the appropriate Channel of ADC1 for sequence conversion step11.
0x06C	SEQ_11_CFG_ADC1_CH_SEL	4	R/W	Defines the appropriate Channel of ADC1 for sequence conversion step12.
0x06D	SEQ_12_CFG_ADC1_CH_SEL	4	R/W	Defines the appropriate Channel of ADC1 for sequence conversion step13.
0x06E	SEQ_13_CFG_ADC1_CH_SEL	4	R/W	Defines the appropriate Channel of ADC1 for sequence conversion step14.
0x06F	SEQ_14_CFG_ADC1_CH_SEL	4	R/W	Defines the appropriate Channel of ADC1 for sequence conversion step15.
0x070	SEQ_15_CFG_ADC1_CH_SEL	4	R/W	Defines the appropriate Channel of ADC1 for sequence conversion step16.
0x071	SEQ_0_CFG_STEP_RPT_NUM	8	R/W	Sets the number of cycles the Sequence Conversion Step1 should be repeated.
0x072	SEQ_1_CFG_STEP_RPT_NUM	8	R/W	Sets the number of cycles the Sequence Conversion Step2 should be repeated.
0x073	SEQ_2_CFG_STEP_RPT_NUM	8	R/W	Sets the number of cycles the Sequence Conversion Step3 should be repeated.
0x074	SEQ_3_CFG_STEP_RPT_NUM	8	R/W	Sets the number of cycles the Sequence Conversion Step4 should be repeated.
0x075	SEQ_4_CFG_STEP_RPT_NUM	8	R/W	Sets the number of cycles the Sequence Conversion Step5 should be repeated.
0x076	SEQ_5_CFG_STEP_RPT_NUM	8	R/W	Sets the number of cycles the Sequence Conversion Step6 should be repeated.
0x077	SEQ_6_CFG_STEP_RPT_NUM	8	R/W	Sets the number of cycles the Sequence Conversion Step7 should be repeated.
0x078	SEQ_7_CFG_STEP_RPT_NUM	8	R/W	Sets the number of cycles the Sequence Conversion Step8 should be repeated.
0x079	SEQ_8_CFG_STEP_RPT_NUM	8	R/W	Sets the number of cycles the Sequence Conversion Step9 should be repeated.
0x07A	SEQ_9_CFG_STEP_RPT_NUM	8	R/W	Sets the number of cycles the Sequence Conversion Step10 should be repeated.
0x07B	SEQ_10_CFG_STEP_RPT_NUM	8	R/W	Sets the number of cycles the Sequence Conversion Step11 should be repeated.
0x07C	SEQ_11_CFG_STEP_RPT_NUM	8	R/W	Sets the number of cycles the Sequence Conversion Step12 should be repeated.
0x07D	SEQ_12_CFG_STEP_RPT_NUM	8	R/W	Sets the number of cycles the Sequence Conversion Step13 should be repeated.
0x07E	SEQ_13_CFG_STEP_RPT_NUM	8	R/W	Sets the number of cycles the Sequence Conversion Step14 should be repeated.
0x07F	SEQ_14_CFG_STEP_RPT_NUM	8	R/W	Sets the number of cycles the Sequence Conversion Step15 should be repeated.
0x080	SEQ_15_CFG_STEP_RPT_NUM	8	R/W	Sets the number of cycles the Sequence Conversion Step16 should be repeated.

Offset	Register Name	Width	Access	Description
0x081	ADC0_CH0_OVER_VOLT_EN	12	R/W	Enables the Over Voltage Alarm feature of ADC0 Channel 0.
0x082	ADC0_CH1_OVER_VOLT_EN	12	R/W	Enables the Over Voltage Alarm feature of ADC0 Channel 1.
0x083	ADC0_CH2_OVER_VOLT_EN	12	R/W	Enables the Over Voltage Alarm feature of ADC0 Channel 2.
0x084	ADC0_CH3_OVER_VOLT_EN	12	R/W	Enables the Over Voltage Alarm feature of ADC0 Channel 3.
0x085	ADC_0_CH4_OVER_VOLT_EN	12	R/W	Enables the Over Voltage Alarm feature of ADC0 Channel 4.
0x086	ADC0_CH5_OVER_VOLT_EN	12	R/W	Enables the Over Voltage Alarm feature of ADC0 Channel 5.
0x087	ADC0_CH6_OVER_VOLT_EN	12	R/W	Enables the Over Voltage Alarm feature of ADC0 Channel 6.
0x088	AL_ADC0_CH7_OVER_VOLT_EN	12	R/W	Enables the Over Voltage Alarm feature of ADC0 Channel 7.
0x089	ADC0_CH8_OVER_VOLT_EN	12	R/W	Enables the Over Voltage Alarm feature of ADC0 VCCM.
0x08A	ADC0_CH9_OVER_VOLT_EN	12	R/W	Enables the Over Voltage Alarm feature of ADC0 VCC.
0x08B	ADC0_CH10_OVER_VOLT_EN	12	R/W	Enables the Over Voltage Alarm feature of ADC0 VCCAUX.
0x08C	ADC0_CH11_OVER_VOLT_EN	12	R/W	Enables the Over Voltage Alarm feature of ADC0 Dp/Dn.
0x08D	ADC1_CH0_OVER_VOLT_EN	12	R/W	Enables the Over Voltage Alarm feature of ADC1 Channel 0.
0x08E	ADC1_CH1_OVER_VOLT_EN	12	R/W	Enables the Over Voltage Alarm feature of ADC1 Channel 1.
0x08F	ADC1_CH2_OVER_VOLT_EN	12	R/W	Enables the Over Voltage Alarm feature of ADC1 Channel 2.
0x090	ADC1_CH3_OVER_VOLT_EN	12	R/W	Enables the Over Voltage Alarm feature of ADC1 Channel 3.
0x091	ADC1_CH4_OVER_VOLT_EN	12	R/W	Enables the Over Voltage Alarm feature of ADC1 Channel 4.
0x092	ADC1_CH5_OVER_VOLT_EN	12	R/W	Enables the Over Voltage Alarm feature of ADC1 Channel 5.
0x093	ADC1_CH6_OVER_VOLT_EN	12	R/W	Enables the Over Voltage Alarm feature of ADC1 Channel 6.
0x094	ADC1_CH7_OVER_VOLT_EN	12	R/W	Enables the Over Voltage Alarm feature of ADC1 Channel 7.
0x095	ADC1_CH8_OVER_VOLT_EN	12	R/W	Enables the Over Voltage Alarm feature of ADC1 VCCIO1.
0x096	ADC1_CH9_OVER_VOLT_EN	12	R/W	Enables the Over Voltage Alarm feature of ADC1 VCCIO0.
0x097	ADC1_CH10_OVER_VOLT_EN	12	R/W	Enables the Over Voltage Alarm feature of ADC1 DTR.
0x098	ADC1_CH11_OVER_VOLT_EN	12	R/W	Enables the Over Voltage Alarm feature of ADC1 Dp/Dn.
0x099	ADC0_CH0_OVER_VOLT_AL_LIMIT	12	R/W	Sets over voltage alarm limit value for ADC0 Channel 0. Allowable values range 0 - 4095.
0x09A	ADC0_CH1_OVER_VOLT_AL_LIMIT	12	R/W	Sets over voltage alarm limit value for ADC0 Channel 1. Allowable values range 0 - 4095.
0x09B	ADC0_CH2_OVER_VOLT_AL_LIMIT	12	R/W	Sets over voltage alarm limit value for ADC0 Channel 2. Allowable values range 0 - 4095.

Offset	Register Name	Width	Access	Description
0x09C	ADC0_CH3_OVER_VOLT_AL_LIMIT	12	R/W	Sets over voltage alarm limit value for ADC0 Channel 3. Allowable values range 0 - 4095.
0x09D	ADC0_CH4_OVER_VOLT_AL_LIMIT	12	R/W	Sets over voltage alarm limit value for ADC0 Channel 4. Allowable values range 0 - 4095.
0x09E	ADC0_CH5_OVER_VOLT_AL_LIMIT	12	R/W	Sets over voltage alarm limit value for ADC0 Channel 5. Allowable values range 0 - 4095.
0x09F	ADC0_CH6_OVER_VOLT_AL_LIMIT	12	R/W	Sets over voltage alarm limit value for ADC0 Channel 6. Allowable values range 0 - 4095.
0x0A0	ADC0_CH7_OVER_VOLT_AL_LIMIT	12	R/W	Sets over voltage alarm limit value for ADC0 Channel 7. Allowable values range 0 - 4095.
0x0A1	ADC0_CH8_OVER_VOLT_AL_LIMIT	12	R/W	Sets over voltage alarm limit value for ADC0 VCCM. Allowable values range 0 - 4095.
0x0A2	ADC0_CH9_OVER_VOLT_AL_LIMIT	12	R/W	Sets over voltage alarm limit value for ADC0 VCC. Allowable values range 0 - 4095.
0x0A3	ADC0_CH10_OVER_VOLT_AL_LIMIT	12	R/W	Sets over voltage alarm limit value for ADC0 VCCAUX. Allowable values range 0 - 4095.
0x0A4	ADC0_CH11_OVER_VOLT_AL_LIMIT	12	R/W	Sets over voltage alarm limit value for ADC0 Channel Dp/Dn. Allowable values range 0 - 4095.
0x0A5	ADC1_CH0_OVER_VOLT_AL_LIMIT	12	R/W	Sets over voltage alarm limit value for ADC1 Channel 0. Allowable values range 0 - 4095.
0x0A6	ADC1_CH1_OVER_VOLT_AL_LIMIT	12	R/W	Sets over voltage alarm limit value for ADC1 Channel 1. Allowable values range 0 - 4095.
0x0A7	ADC1_CH2_OVER_VOLT_AL_LIMIT	12	R/W	Sets over voltage alarm limit value for ADC1 Channel 2. Allowable values range 0 - 4095.
0x0A8	ADC1_CH3_OVER_VOLT_AL_LIMIT	12	R/W	Sets over voltage alarm limit value for ADC1 Channel 3. Allowable values range 0 - 4095.
0x0A9	ADC1_CH4_OVER_VOLT_AL_LIMIT	12	R/W	Sets over voltage alarm limit value for ADC1 Channel 4. Allowable values range 0 - 4095.
0x0AA	ADC1_CH5_OVER_VOLT_AL_LIMIT	12	R/W	Sets over voltage alarm limit value for ADC1 Channel 5. Allowable values range 0 - 4095.
0x0AB	ADC1_CH6_OVER_VOLT_AL_LIMIT	12	R/W	Sets over voltage alarm limit value for ADC1 Channel 6. Allowable values range 0 - 4095.
0x0AC	ADC1_CH7_OVER_VOLT_AL_LIMIT	12	R/W	Sets over voltage alarm limit value for ADC1 Channel 7. Allowable values range 0 - 4095.
0x0AD	ADC1_CH8_OVER_VOLT_AL_LIMIT	12	R/W	Sets over voltage alarm limit value for ADC1 VCCIO1. Allowable values range 0 - 4095.
0x0AE	ADC1_CH9_OVER_VOLT_AL_LIMIT	12	R/W	Sets over voltage alarm limit value for ADC1 VCCIO0. Allowable values range 0 - 4095.
0x0AF	ADC1_CH10_OVER_VOLT_AL_LIMIT	12	R/W	Sets over voltage alarm limit value for ADC1 DTR. Allowable values range 0 - 4095.
0X0B0	ADC1_CH11_OVER_VOLT_AL_LIMIT	12	R/W	Sets over voltage alarm limit value for ADC1 Channel Dp/Dn. Allowable values range 0 - 4095.
0X0B1	ADC0_CH0_OVER_EVENT_NUM	3	R/W	Sets the number of consecutive over voltage limit events to set alarm for ADC0 Channel 0. Max. number is 4.
0X0B2	ADC0_CH1_OVER_EVENT_NUM	3	R/W	Sets the number of consecutive over voltage limit events to set alarm for ADC0 Channel 1. Max. number is 4.
0X0B3	ADC0_CH2_OVER_EVENT_NUM	3	R/W	Sets the number of consecutive over voltage limit events to set alarm for ADC0 Channel 2. Max. number is 4.

Offset	Register Name	Width	Access	Description
0X0B4	ADC0_CH3_OVER_EVENT_NUM	3	R/W	Sets the number of consecutive over voltage limit events to set alarm for ADC0 Channel 3. Max. number is 4.
0X0B5	ADC0_CH4_OVER_EVENT_NUM	3	R/W	Sets the number of consecutive over voltage limit events to set alarm for ADC0 Channel 4. Max. number is 4.
0X0B6	ADC0_CH5_OVER_EVENT_NUM	3	R/W	Sets the number of consecutive over voltage limit events to set alarm for ADC0 Channel 5. Max. number is 4.
0X0B7	ADC0_CH6_OVER_EVENT_NUM	3	R/W	Sets the number of consecutive over voltage limit events to set alarm for ADC0 Channel 6. Max. number is 4.
0X0B8	ADC0_CH7_OVER_EVENT_NUM	3	R/W	Sets the number of consecutive over voltage limit events to set alarm for ADC0 Channel 7. Max. number is 4.
0X0B9	ADC0_CH8_OVER_EVENT_NUM	3	R/W	Sets the number of consecutive over voltage limit events to set alarm for ADC0 VCCM. Max. number is 4.
0X0BA	ADC0_CH9_OVER_EVENT_NUM	3	R/W	Sets the number of consecutive over voltage limit events to set alarm for ADC0 VCC. Max. number is 4.
0X0BB	ADC0_CH10_OVER_EVENT_NUM	3	R/W	Sets the number of consecutive over voltage limit events to set alarm for ADC0 VCCAUX. Max. number is 4.
0X0BC	ADC0_CH11_OVER_EVENT_NUM	3	R/W	Sets the number of consecutive over voltage limit events to set alarm for ADC0 Channel Dp[0]/Dn[0]. Max. number is 4.
0X0BD	ADC1_CH0_OVER_EVENT_NUM	3	R/W	Sets the number of consecutive over voltage limit events to set alarm for ADC1 Channel 0. Max. number is 4.
0X0BE	ADC1_CH1_OVER_EVENT_NUM	3	R/W	Sets the number of consecutive over voltage limit events to set alarm for ADC1 Channel 1. Max. number is 4.
0X0BF	ADC1_CH2_OVER_EVENT_NUM	3	R/W	Sets the number of consecutive over voltage limit events to set alarm for ADC1 Channel 2. Max. number is 4.
0X0C0	ADC1_CH3_OVER_EVENT_NUM	3	R/W	Sets the number of consecutive over voltage limit events to set alarm for ADC1 Channel 3. Max. number is 4.
0X0C1	ADC1_CH4_OVER_EVENT_NUM	3	R/W	Sets the number of consecutive over voltage limit events to set alarm for ADC1 Channel 4. Max. number is 4.
0X0C2	ADC1_CH5_OVER_EVENT_NUM	3	R/W	Sets the number of consecutive over voltage limit events to set alarm for ADC1 Channel 5. Max. number is 4.
0X0C3	ADC1_CH_6_OVER_EVENT_NUM	3	R/W	Sets the number of consecutive over voltage limit events to set alarm for ADC1 Channel 6. Max. number is 4.
0X0C4	ADC1_CH_7_OVER_EVENT_NUM	3	R/W	Sets the number of consecutive over voltage limit events to set alarm for ADC1 Channel 7. Max. number is 4.
0X0C5	ADC1_CH8_OVER_EVENT_NUM	3	R/W	Sets the number of consecutive over voltage limit events to set alarm for ADC1 VCCIO1. Max. number is 4.
0X0C6	ADC1_CH9_OVER_EVENT_NUM	3	R/W	Sets the number of consecutive over voltage limit events to set alarm for ADC1 VCCIO0. Max. number is 4.

Offset	Register Name	Width	Access	Description
0X0C7	ADC1_CH10_OVER_EVENT_NUM	3	R/W	Sets the number of consecutive over voltage limit events to set alarm for ADC1 DTR. Max. number is 4.
0X0C8	ADC1_CH11_OVER_EVENT_NUM	3	R/W	Sets the number of consecutive over voltage limit events to set alarm for ADC1 Dp/Dn. Max. number is 4.
0X0C9	ADC0_CH0_OVER_STICKY_OUT	12	R/W	Sets over voltage alarm output sticky mode for ADC0 Channel0.
0X0CA	ADC0_CH1_OVER_STICKY_OUT	12	R/W	Sets over voltage alarm output sticky mode for ADC0 Channel1.
0X0CB	ADC0_CH2_OVER_STICKY_OUT	12	R/W	Sets over voltage alarm output sticky mode for ADC0 Channel2.
0X0CC	ADC0_CH3_OVER_STICKY_OUT	12	R/W	Sets over voltage alarm output sticky mode for ADC0 Channel3.
0X0CD	ADC0_CH4_OVER_STICKY_OUT	12	R/W	Sets over voltage alarm output sticky mode for ADC0 Channel4.
0X0CE	ADC0_CH5_OVER_STICKY_OUT	12	R/W	Sets over voltage alarm output sticky mode for ADC0 Channel5.
0X0CF	ADC0_CH6_OVER_STICKY_OUT	12	R/W	Sets over voltage alarm output sticky mode for ADC0 Channel6.
0X0D0	ADC0_CH7_OVER_STICKY_OUT	12	R/W	Sets over voltage alarm output sticky mode for ADC0 Channel7.
0X0D1	ADC0_CH8_OVER_STICKY_OUT	12	R/W	Sets over voltage alarm output sticky mode for ADC0 VCCM.
0X0D2	ADC0_CH9_OVER_STICKY_OUT	12	R/W	Sets over voltage alarm output sticky mode for ADC0 VCC.
0X0D3	ADC0_CH10_OVER_STICKY_OUT	12	R/W	Sets over voltage alarm output sticky mode for ADC0 VCCAUX.
0X0D4	ADC0_CH11_OVER_STICKY_OUT	12	R/W	Sets over voltage alarm output sticky mode for ADC0 Channel Dp/Dn.
0X0D5	ADC1_CH0_OVER_STICKY_OUT	12	R/W	Sets over voltage alarm output sticky mode for ADC1 Channel0.
0X0D6	ADC1_CH1_OVER_STICKY_OUT	12	R/W	Sets over voltage alarm output sticky mode for ADC1 Channel1.
0X0D7	ADC1_CH2_OVER_STICKY_OUT	12	R/W	Sets over voltage alarm output sticky mode for ADC1 Channel2.
0X0D8	ADC1_CH3_OVER_STICKY_OUT	12	R/W	Sets over voltage alarm output sticky mode for ADC1 Channel3.
0X0D9	ADC1_CH4_OVER_STICKY_OUT	12	R/W	Sets over voltage alarm output sticky mode for ADC1 Channel4.
0X0DA	ADC1_CH5_OVER_STICKY_OUT	12	R/W	Sets over voltage alarm output sticky mode for ADC1 Channel5.
0X0DB	ADC1_CH6_OVER_STICKY_OUT	12	R/W	Sets over voltage alarm output sticky mode for ADC1 Channel6.
0X0DC	ADC1_CH7_OVER_STICKY_OUT	12	R/W	Sets over voltage alarm output sticky mode for ADC1 Channel7.
0X0DD	ADC1_CH8_OVER_STICKY_OUT	12	R/W	Sets over voltage alarm output sticky mode for ADC1 VCCIO1.
0X0DE	ADC1_CH9_OVER_STICKY_OUT	12	R/W	Sets over voltage alarm output sticky mode for ADC1 VCCIO0.
0X0DF	ADC1_CH10_OVER_STICKY_OUT	12	R/W	Sets over voltage alarm output sticky mode for ADC1 DTR.
0X0E0	ADC1_CH11_OVER_STICKY_OUT	12	R/W	Sets over voltage alarm output sticky mode for ADC1 Dp/Dn.

Offset	Register Name	Width	Access	Description
0X0E1	ADC0_CH0_UNDER_VOLT_EN	12	R/W	Enables the Under-Voltage Alarm feature of ADC0 Channel 0.
0X0E2	ADC0_CH1_UNDER_VOLT_EN	12	R/W	Enables the Under-Voltage Alarm feature of ADC0 Channel 1.
0X0E3	ADC0_CH2_UNDER_VOLT_EN	12	R/W	Enables the Under-Voltage Alarm feature of ADC0 Channel 2.
0X0E4	ADC0_CH3_UNDER_VOLT_EN	12	R/W	Enables the Under-Voltage Alarm feature of ADC0 Channel 3.
0X0E5	ADC0_CH4_UNDER_VOLT_EN	12	R/W	Enables the Under-Voltage Alarm feature of ADC0 Channel 4.
0X0E6	ADC0_CH5_UNDER_VOLT_EN	12	R/W	Enables the Under-Voltage Alarm feature of ADC0 Channel 5.
0X0E7	ADC0_CH6_UNDER_VOLT_EN	12	R/W	Enables the Under-Voltage Alarm feature of ADC0 Channel 6.
0X0E8	ADC0_CH7_UNDER_VOLT_EN	12	R/W	Enables the Under-Voltage Alarm feature of ADC0 Channel 7.
0X0E9	ADC0_CH8_UNDER_VOLT_EN	12	R/W	Enables the Under-Voltage Alarm feature of ADC0 VCCM.
0X0EA	ADC0_CH9_UNDER_VOLT_EN	12	R/W	Enables the Under-Voltage Alarm feature of ADC0 VCC.
0X0EB	ADC0_CH10_UNDER_VOLT_EN	12	R/W	Enables the Under-Voltage Alarm feature of ADC0 VCCAUX.
0X0EC	ADC0_CH11_UNDER_VOLT_EN	12	R/W	Enables the Under-Voltage Alarm feature of ADC0 Dp/Dn.
0X0ED	ADC1_CH0_UNDER_VOLT_EN	12	R/W	Enables the Under-Voltage Alarm feature of ADC1 Channel 0.
0X0EE	ADC1_CH1_UNDER_VOLT_EN	12	R/W	Enables the Under-Voltage Alarm feature of ADC1 Channel 1.
0X0EF	ADC1_CH2_UNDER_VOLT_EN	12	R/W	Enables the Under-Voltage Alarm feature of ADC1 Channel 2.
0x0F0	ADC1_CH3_UNDER_VOLT_EN	12	R/W	Enables the Under-Voltage Alarm feature of ADC1 Channel 3.
0x0F1	ADC1_CH4_UNDER_VOLT_EN	12	R/W	Enables the Under-Voltage Alarm feature of ADC1 Channel 4.
0x0F2	ADC1_CH5_UNDER_VOLT_EN	12	R/W	Enables the Under-Voltage Alarm feature of ADC1 Channel 5.
0x0F3	ADC1_CH6_UNDER_VOLT_EN	12	R/W	Enables the Under-Voltage Alarm feature of ADC1 Channel 6.
0x0F4	ADC1_CH7_UNDER_VOLT_EN	12	R/W	Enables the Under-Voltage Alarm feature of ADC1 Channel 7.
0x0F5	ADC1_CH8_UNDER_VOLT_EN	12	R/W	Enables the Under-Voltage Alarm feature of ADC1 VCCIO1.
0x0F6	ADC1_CH9_UNDER_VOLT_EN	12	R/W	Enables the Under-Voltage Alarm feature of ADC1 VCCIO0.
0x0F7	ADC1_CH10_UNDER_VOLT_EN	12	R/W	Enables the Under-Voltage Alarm feature of ADC1 DTR.
0x0F8	ADC1_CH11_UNDER_VOLT_EN	12	R/W	Enables the Under-Voltage Alarm feature of ADC1 Dp/Dn.
0x0F9	ADC0_CH0_UNDER_VOLT_AL_LIMIT	12	R/W	Sets Under Voltage Alarm limit value for ADC0 Channel 0. Allowable values range 0 - 4095.
0x0FA	ADC0_CH1_UNDER_VOLT_AL_LIMIT	12	R/W	Sets Under Voltage Alarm limit value for ADC0 Channel 1. Allowable values range 0 - 4095.
0x0FB	ADC0_CH2_UNDER_VOLT_AL_LIMIT	12	R/W	Sets Under Voltage Alarm limit value for ADC0 Channel 2. Allowable values range 0 - 4095.

Offset	Register Name	Width	Access	Description
0x0FC	ADC0_CH3_UNDER_VOLT_AL_LIMIT	12	R/W	Sets Under Voltage Alarm limit value for ADC0 Channel 3. Allowable values range 0 - 4095.
0x0FD	ADC0_CH4_UNDER_VOLT_AL_LIMIT	12	R/W	Sets Under Voltage Alarm limit value for ADC0 Channel 4. Allowable values range 0 - 4095.
0x0FE	ADC0_CH5_UNDER_VOLT_AL_LIMIT	12	R/W	Sets Under Voltage Alarm limit value for ADC0 Channel 5. Allowable values range 0 - 4095.
0x0FF	ADC0_CH6_UNDER_VOLT_AL_LIMIT	12	R/W	Sets Under Voltage Alarm limit value for ADC0 Channel 6. Allowable values range 0 - 4095.
0x100	ADC0_CH7_UNDER_VOLT_AL_LIMIT	12	R/W	Sets Under Voltage Alarm limit value for ADC0 Channel 7. Allowable values range 0 - 4095.
0x101	ADC0_CH8_UNDER_VOLT_AL_LIMIT	12	R/W	Sets Under Voltage Alarm limit value for ADC0 VCCM. Allowable values range 0 - 4095.
0x102	ADC0_CH9_UNDER_VOLT_AL_LIMIT	12	R/W	Sets Under Voltage Alarm limit value for ADC0 VCC. Allowable values range 0 - 4095.
0x103	ADC0_CH10_UNDER_VOLT_AL_LIMIT	12	R/W	Sets Under Voltage Alarm limit value for ADC0 VCCAUX. Allowable values range 0 - 4095.
0x104	ADC0_CH11_UNDER_VOLT_AL_LIMIT	12	R/W	Sets Under Voltage Alarm limit value for ADC0 Channel Dp/Dn. Allowable values range 0 - 4095.
0x105	ADC1_CH0_UNDER_VOLT_AL_LIMIT	12	R/W	Sets Under Voltage Alarm limit value for ADC1 Channel 0. Allowable values range 0 - 4095.
0x106	ADC1_CH1_UNDER_VOLT_AL_LIMIT	12	R/W	Sets Under Voltage Alarm limit value for ADC1 Channel 1. Allowable values range 0 - 4095.
0x107	ADC1_CH2_UNDER_VOLT_AL_LIMIT	12	R/W	Sets Under Voltage Alarm limit value for ADC1 Channel 2. Allowable values range 0 - 4095.
0x108	ADC1_CH3_UNDER_VOLT_AL_LIMIT	12	R/W	Sets Under Voltage Alarm limit value for ADC1 Channel 3. Allowable values range 0 - 4095.
0x109	ADC1_CH4_UNDER_VOLT_AL_LIMIT	12	R/W	Sets Under Voltage Alarm limit value for ADC1 Channel 4. Allowable values range 0 - 4095.
0x10A	ADC1_CH5_UNDER_VOLT_AL_LIMIT	12	R/W	Sets Under Voltage Alarm limit value for ADC1 Channel 5. Allowable values range 0 - 4095.
0x10B	ADC1_CH6_UNDER_VOLT_AL_LIMIT	12	R/W	Sets Under Voltage Alarm limit value for ADC1 Channel 6. Allowable values range 0 - 4095.
0x10C	ADC1_CH7_UNDER_VOLT_AL_LIMIT	12	R/W	Sets Under Voltage Alarm limit value for ADC1 Channel 7. Allowable values range 0 - 4095.
0x10D	ADC1_CH8_UNDER_VOLT_AL_LIMIT	12	R/W	Sets Under voltage alarm limit value for ADC1 VCCIO1. Allowable values range 0 - 4095.
0x10E	ADC1_CH9_UNDER_VOLT_AL_LIMIT	12	R/W	Sets Under Voltage Alarm limit value for ADC1 VCCIO0. Allowable values range 0 - 4095.
0x10F	ADC1_CH10_UNDER_VOLT_AL_LIMIT	12	R/W	Sets Under Voltage Alarm limit value for ADC1 DTR. Allowable values range 0 - 4095.
0x110	ADC1_CH11_UNDER_VOLT_AL_LIMIT	12	R/W	Sets Under Voltage Alarm limit value for ADC1 Channel Dp/Dn. Allowable values range 0 - 4095.
0x111	ADC0_CH0_UNDER_EVENT_NUM	3	R/W	Sets the number of consecutive Under Voltage limit events to set alarm for ADC0 Channel 0. Max. number is 4.
0x112	ADC0_CH1_UNDER_EVENT_NUM	3	R/W	Sets the number of consecutive Under Voltage limit events to set alarm for ADC0 Channel 1. Max. number is 4.
0x113	ADC0_CH2_UNDER_EVENT_NUM	3	R/W	Sets the number of consecutive Under Voltage limit events to set alarm for ADC0 Channel 2. Max. number is 4.

Offset	Register Name	Width	Access	Description
0x114	ADC0_CH3_UNDER_EVENT_NUM	3	R/W	Sets the number of consecutive Under Voltage limit events to set alarm for ADC0 Channel 3. Max. number is 4.
0x115	ADC0_CH4_UNDER_EVENT_NUM	3	R/W	Sets the number of consecutive Under Voltage limit events to set alarm for ADC0 Channel 4. Max. number is 4.
0x116	ADC0_CH5_UNDER_EVENT_NUM	3	R/W	Sets the number of consecutive Under Voltage limit events to set alarm for ADC0 Channel 5. Max. number is 4.
0x117	ADC0_CH6_UNDER_EVENT_NUM	3	R/W	Sets the number of consecutive Under Voltage limit events to set alarm for ADC0 Channel 6. Max. number is 4.
0x118	ADC0_CH7_UNDER_EVENT_NUM	3	R/W	Sets the number of consecutive Under Voltage limit events to set alarm for ADC0 Channel 7. Max. number is 4.
0x119	ADC0_CH8_UNDER_EVENT_NUM	3	R/W	Sets the number of consecutive Under Voltage limit events to set alarm for ADC0 VCCM. Max. number is 4.
0x11A	ADC0_CH9_UNDER_EVENT_NUM	3	R/W	Sets the number of consecutive Under Voltage limit events to set alarm for ADC0 VCC. Max. number is 4.
0x11B	ADC0_CH10_UNDER_EVENT_NUM	3	R/W	Sets the number of consecutive Under Voltage limit events to set alarm for ADC0 VCCAUX. Max. number is 4.
0x11C	ADC0_CH11_UNDER_EVENT_NUM	3	R/W	Sets the number of consecutive Under Voltage limit events to set alarm for ADC0 Channel Dp/Dn. Max. number is 4.
0x11D	ADC1_CH0_UNDER_EVENT_NUM	3	R/W	Sets the number of consecutive Under Voltage limit events to set alarm for ADC1 Channel 0. Max. number is 4.
0x11E	ADC1_CH1_UNDER_EVENT_NUM	3	R/W	Sets the number of consecutive Under Voltage limit events to set alarm for ADC1 Channel 1. Max. number is 4.
0x11F	ADC1_CH2_UNDER_EVENT_NUM	3	R/W	Sets the number of consecutive Under Voltage limit events to set alarm for ADC1 Channel 2. Max. number is 4.
0x120	ADC1_CH3_UNDER_EVENT_NUM	3	R/W	Sets the number of consecutive Under Voltage limit events to set alarm for ADC1 Channel 3. Max. number is 4.
0x121	ADC1_CH4_UNDER_EVENT_NUM	3	R/W	Sets the number of consecutive Under Voltage limit events to set alarm for ADC1 Channel 4. Max. number is 4.
0x122	ADC1_CH5_UNDER_EVENT_NUM	3	R/W	Sets the number of consecutive Under Voltage limit events to set alarm for ADC1 Channel 5. Max. number is 4.
0x123	ADC1_CH6_UNDER_EVENT_NUM	3	R/W	Sets the number of consecutive Under Voltage limit events to set alarm for ADC1 Channel 6. Max. number is 4.
0x124	ADC1_CH7_UNDER_EVENT_NUM	3	R/W	Sets the number of consecutive Under Voltage limit events to set alarm for ADC1 Channel 7. Max. number is 4.
0x125	ADC1_CH8_UNDER_EVENT_NUM	3	R/W	Sets the number of consecutive Under Voltage limit events to set alarm for ADC1 VCCIO1. Max. number is 4.

Offset	Register Name	Width	Access	Description
0x126	ADC1_CH9_UNDER_EVENT_NUM	3	R/W	Sets the number of consecutive Under Voltage limit events to set alarm for ADC1 VCCIO0. Max. number is 4.
0x127	ADC1_CH10_UNDER_EVENT_NUM	3	R/W	Sets the number of consecutive Under Voltage limit events to set alarm for ADC1 DTR. Max. number is 4.
0x128	ADC1_CH11_UNDER_EVENT_NUM	3	R/W	Sets the number of consecutive Under Voltage limit events to set alarm for ADC1 Dp/Dn. Max. number is 4.
0x129	ADC0_CH0_UNDER_STICKY_OUT	12	R/W	Sets Under Voltage alarm output sticky mode for ADC0 Channel0.
0x12A	ADC0_CH1_UNDER_STICKY_OUT	12	R/W	Sets Under Voltage alarm output sticky mode for ADC0 Channel1.
0x12B	ADC0_CH2_UNDER_STICKY_OUT	12	R/W	Sets Under Voltage alarm output sticky mode for ADC0 Channel2.
0x12C	ADC0_CH3_UNDER_STICKY_OUT	12	R/W	Sets Under Voltage alarm output sticky mode for ADC0 Channel3.
0x12D	ADC0_CH4_UNDER_STICKY_OUT	12	R/W	Sets Under Voltage alarm output sticky mode for ADC0 Channel4.
0x12E	ADC0_CH5_UNDER_STICKY_OUT	12	R/W	Sets Under Voltage alarm output sticky mode for ADC0 Channel5.
0x12F	ADC0_CH6_UNDER_STICKY_OUT	12	R/W	Sets Under Voltage alarm output sticky mode for ADC0 Channel6.
0x130	ADC0_CH7_UNDER_STICKY_OUT	12	R/W	Sets Under Voltage alarm output sticky mode for ADC0 Channel7.
0x131	ADC0_CH8_UNDER_STICKY_OUT	12	R/W	Sets Under voltage alarm output sticky mode for ADC0 VCCM.
0x132	ADC0_CH9_UNDER_STICKY_OUT	12	R/W	Sets Under Voltage alarm output sticky mode for ADC0 VCC.
0x133	ADC0_CH10_UNDER_STICKY_OUT	12	R/W	Sets Under Voltage alarm output sticky mode for ADC0 VCCAUX.
0x134	ADC0_CH11_UNDER_STICKY_OUT	12	R/W	Sets Under Voltage alarm output sticky mode for ADC0 Channel Dp/Dn.
0x135	ADC1_CH0_UNDER_STICKY_OUT	12	R/W	Sets Under Voltage alarm output sticky mode for ADC1 Channel0.
0x136	ADC1_CH1_UNDER_STICKY_OUT	12	R/W	Sets Under Voltage alarm output sticky mode for ADC1 Channel1.
0x137	ADC1_CH2_UNDER_STICKY_OUT	12	R/W	Sets Under Voltage alarm output sticky mode for ADC1 Channel2.
0x138	ADC1_CH3_UNDER_STICKY_OUT	12	R/W	Sets Under voltage alarm output sticky mode for ADC1 Channel3.
0x139	ADC1_CH4_UNDER_STICKY_OUT	12	R/W	Sets Under Voltage alarm output sticky mode for ADC1 Channel4.
0x13A	ADC1_CH5_UNDER_STICKY_OUT	12	R/W	Sets Under Voltage alarm output sticky mode for ADC1 Channel5.
0x13B	ADC1_CH6_UNDER_STICKY_OUT	12	R/W	Sets Under Voltage alarm output sticky mode for ADC1 Channel6.
0x13C	ADC1_CH7_UNDER_STICKY_OUT	12	R/W	Sets Under Voltage alarm output sticky mode for ADC1 Channel7.
0x13D	ADC1_CH8_UNDER_STICKY_OUT	12	R/W	Sets Under Voltage alarm output sticky mode for ADC1 VCCIO1.
0x13E	ADC1_CH9_UNDER_STICKY_OUT	12	R/W	Sets Under Voltage alarm output sticky mode for ADC1 VCCIO0.
0x13F	ADC1_CH10_UNDER_STICKY_OUT	12	R/W	Sets Under Voltage alarm output sticky mode for ADC1 DTR.

Offset	Register Name	Width	Access	Description
0x140	ADC1_CH11_UNDER_STICKY_OUT	12	R/W	Sets Under Voltage alarm output sticky mode for ADC1 Dp/Dn.
0x141	LMMI_ADC_EN	1	R/W	Enables ADC output data transmission through LMMI.
0x142	LMMI_ADC_0_CH_SEL	4	R/W	Selects the appropriate input channel of ADC0.
0x143	LMMI_ADC_0_EN	1	R/W	Enables ADC0.
0x144	LMMI_ADC_1_CH_SEL	4	R/W	Selects the appropriate input channel of ADC1.
0x145	LMMI_ADC_1_EN	1	R/W	Enables ADC1.
0x146	LMMI_ADC_SOC	1	R/W	When set to “1” it enables SOC signal.
0x147	LMMI_ADC_CAL	1	R/W	Initiates calibration.
0x148	LMMI_ADC_CONVSTOP	1	R/W	When set “1” it initiates the conversion stop signal (CONVSTOP).
0x149	LMMI_INT_SET_REG	24	R/W	Clear Interrupt register.
0x14A	LMMI_INT_EN_REG	24	R/W	Enables Over/Under voltage alarm event function individually for all ADC inputs.
0x14B	LMMI_INT_STATUS_REG	32	R	Read interrupt status.
0x14C	ADDR_RD_FIFO_DATA_REG	32	R	Read FIFO data.
0x14D	ADDR_COMP_RESULTS	3	R	Read Comparator outputs.
0x14E	ADDR_COMP_LATCHED_RESULTS	3	R	Read Comparator latched outputs.
0x14F	ADDR_RD_DATA_REG	25	R	Read converted data.
0x150	ADDR_LMMI_ADC_EOC	1	R	Indicates end of conversion.
0x151	ADDR_LMMI_ADC_CALRDY	1	R	Indicates end of calibration.
0x152	ADDR_SEQ_CFG_SEQ_STATE	2	R	Indicates the current state of the Sequencer
0x153	ADC_CORE_SEL	1	W	When set to 1, ADC1 is selected for axi_tdata_o and lmmi_rdata_o value when accessing ADDR_RD_FIFO_DATA_REG register; else ADC0 is selected.

2.4.2. Register Reference Values

Table 2.4. ADC0_CHANNEL_EN and ADC1_CHANNEL_EN Register Details

Register Name	Bit Value	Channel
(0x003) ADC0_CHANNEL_EN[11:0]		
[0]	1 – enable; 0 – disable	ADC0 Ch0
[1]	1 – enable; 0 – disable	ADC0 Ch1
[2]	1 – enable; 0 – disable	ADC0 Ch2
[3]	1 – enable; 0 – disable	ADC0 Ch3
[4]	1 – enable; 0 – disable	ADC0 Ch4
[5]	1 – enable; 0 – disable	ADC0 Ch5
[6]	1 – enable; 0 – disable	ADC0 Ch6
[7]	1 – enable; 0 – disable	ADC0 Ch7
[8]	1 – enable; 0 – disable	ADC0 VCCM
[9]	1 – enable; 0 – disable	ADC0 VCC
[10]	1 – enable; 0 – disable	ADC0 VCCAUX
[11]	1 – enable; 0 – disable	ADC0 Dp/Dn

Register Name	Bit Value	Channel
(0x004) ADC1_CHANNEL_EN[11:0]		
[0]	1 – enable; 0 – disable	ADC1 Ch0
[1]	1 – enable; 0 – disable	ADC1 Ch1
[2]	1 – enable; 0 – disable	ADC1 Ch2
[3]	1 – enable; 0 – disable	ADC1 Ch3
[4]	1 – enable; 0 – disable	ADC1 Ch4
[5]	1 – enable; 0 – disable	ADC1 Ch5
[6]	1 – enable; 0 – disable	ADC1 Ch6
[7]	1 – enable; 0 – disable	ADC1 Ch7
[8]	1 – enable; 0 – disable	ADC1 VCCIO1
[9]	1 – enable; 0 – disable	ADC1 VCCIO0
[10]	1 – enable; 0 – disable	ADC1 DTR
[11]	1 – enable; 0 – disable	ADC1 Dp/Dn

Table 2.5. ADCX_CHY_MIN_SMPL_TIME Register Details

Register Name	Accepted Values	Default Value
(0x005) ADC0_CH0_MIN_SMPL_TIME[7:0]	4–128	4
(0x006) ADC0_CH1_MIN_SMPL_TIME[7:0]	4–128	4
(0x007) ADC0_CH2_MIN_SMPL_TIME[7:0]	4–128	4
(0x008) ADC0_CH3_MIN_SMPL_TIME[7:0]	4–128	4
(0x009) ADC0_CH4_MIN_SMPL_TIME[7:0]	4–128	4
(0x00A) ADC0_CH5_MIN_SMPL_TIME[7:0]	4–128	4
(0x00B) ADC0_CH6_MIN_SMPL_TIME[7:0]	4–128	4
(0x00C) ADC0_CH7_MIN_SMPL_TIME[7:0]	4–128	4
(0x00D) ADC0_CH8_MIN_SMPL_TIME[7:0]	4–128	16
(0x00E) ADC0_CH9_MIN_SMPL_TIME[7:0]	4–128	16
(0x00F) ADC0_CH10_MIN_SMPL_TIME[7:0]	4–128	16
(0x010) ADC0_CH11_MIN_SMPL_TIME[7:0]	4–128	4
(0x011) ADC1_CH0_MIN_SMPL_TIME[7:0]	4–128	4
(0x012) ADC1_CH1_MIN_SMPL_TIME[7:0]	4–128	4
(0x013) ADC1_CH2_MIN_SMPL_TIME[7:0]	4–128	4
(0x014) ADC1_CH3_MIN_SMPL_TIME[7:0]	4–128	4
(0x015) ADC1_CH4_MIN_SMPL_TIME[7:0]	4–128	4
(0x016) ADC1_CH5_MIN_SMPL_TIME[7:0]	4–128	4
(0x017) ADC1_CH6_MIN_SMPL_TIME[7:0]	4–128	4
(0x018) ADC1_CH7_MIN_SMPL_TIME[7:0]	4–128	4
(0x019) ADC1_CH8_MIN_SMPL_TIME[7:0]	4–128	16
(0x01A) ADC1_CH9_MIN_SMPL_TIME[7:0]	4–128	16
(0x01B) ADC1_CH10_MIN_SMPL_TIME[7:0]	4–128	16
(0x01C) ADC1_CH11_MIN_SMPL_TIME[7:0]	4–128	4

Table 2.6. ADCX_CHY_SAMPLES_NUM Register Details

Register Name	Accepted Values	Default Value
(0x01D) ADC0_CH0_SAMPLES_NUM[2:0]	1–4	1
(0x01E) ADC0_CH1_SAMPLES_NUM[2:0]	1–4	1
(0x01F) ADC0_CH2_SAMPLES_NUM[2:0]	1–4	1
(0x020) ADC0_CH3_SAMPLES_NUM[2:0]	1–4	1
(0x021) ADC0_CH4_SAMPLES_NUM[2:0]	1–4	1
(0x022) ADC0_CH5_SAMPLES_NUM[2:0]	1–4	1
(0x023) ADC0_CH6_SAMPLES_NUM[2:0]	1–4	1
(0x024) ADC0_CH7_SAMPLES_NUM[2:0]	1–4	1
(0x025) ADC0_CH8_SAMPLES_NUM[2:0]	1–4	2
(0x026) ADC0_CH9_SAMPLES_NUM[2:0]	1–4	2
(0x027) ADC0_CH10_SAMPLES_NUM[2:0]	1–4	2
(0x028) ADC0_CH11_SAMPLES_NUM[2:0]	1–4	1
(0x029) ADC1_CH0_SAMPLES_NUM[2:0]	1–4	1
(0x02A) ADC1_CH1_SAMPLES_NUM[2:0]	1–4	1
(0x02B) ADC1_CH2_SAMPLES_NUM[2:0]	1–4	1
(0x02C) ADC1_CH3_SAMPLES_NUM[2:0]	1–4	1
(0x02D) ADC1_CH4_SAMPLES_NUM[2:0]	1–4	1
(0x02E) ADC1_CH5_SAMPLES_NUM[2:0]	1–4	1
(0x02F) ADC1_CH6_SAMPLES_NUM[2:0]	1–4	1
(0x030) ADC1_CH7_SAMPLES_NUM[2:0]	1–4	1
(0x031) ADC1_CH8_SAMPLES_NUM[2:0]	1–4	2
(0x032) ADC1_CH9_SAMPLES_NUM[2:0]]	1–4	2
(0x033) ADC1_CH10_SAMPLES_NUM[2:0]	1–4	2
(0x034) ADC1_CH11_SAMPLES_NUM[2:0]	1–4	1

Table 2.7. ADCX_CHY_CONV_NUM Register Details

Register Name	Accepted Values	Default Value
(0x035) ADC0_CH0_CONV_NUM[2:0]	1–4	1
(0x036) ADC0_CH1_CONV_NUM[2:0]	1–4	1
(0x037) ADC0_CH2_CONV_NUM[2:0]	1–4	1
(0x038) ADC0_CH3_CONV_NUM[2:0]	1–4	1
(0x039) ADC0_CH4_CONV_NUM[2:0]	1–4	1
(0x03A) ADC0_CH5_CONV_NUM[2:0]	1–4	1
(0x03B) ADC0_CH6_CONV_NUM[2:0]	1–4	1
(0x03C) ADC0_CH7_CONV_NUM[2:0]	1–4	1
(0x03D) ADC0_CH8_CONV_NUM[2:0]	1–4	4
(0x03E) ADC0_CH9_CONV_NUM[2:0]	1–4	4
(0x03F) ADC0_CH10_CONV_NUM[2:0]	1–4	4
(0x040) ADC0_CH11_CONV_NUM[2:0]	1–4	1
(0x041) ADC1_CH0_CONV_NUM[2:0]	1–4	1
(0x042) ADC1_CH1_CONV_NUM[2:0]	1–4	1
(0x043) ADC1_CH2_CONV_NUM[2:0]	1–4	1
(0x044) ADC1_CH3_CONV_NUM[2:0]	1–4	1
(0x045) ADC1_CH4_CONV_NUM[2:0]	1–4	1
(0x046) ADC1_CH5_CONV_NUM[2:0]	1–4	1
(0x047) ADC1_CH6_CONV_NUM[2:0]	1–4	1

Register Name	Accepted Values	Default Value
(0x048) ADC1_CH7_CONV_NUM[2:0]	1–4	1
(0x049) ADC1_CH8_CONV_NUM[2:0]	1–4	4
(0x04A) ADC1_CH9_CONV_NUM[2:0]]	1–4	4
(0x04B) ADC1_CH10_CONV_NUM[2:0]	1–4	4
(0x04C) ADC1_CH11_CONV_NUM[2:0]	1–4	1

Table 2.8. SEQ_CFG_SEQ_NUM Register Details

Register Name	Accepted Values	Default Value
(0x04F) SEQ_CFG_SEQ_NUM[4:0]	1–16	1

Table 2.9. SEQ_CONVSTEPX_ADC0_CH_SEL Register Details

Register Name	Accepted Values	Default Value
(0x051) SEQ_CONVSTEP0_ADC0_CH_SEL[3:0]	0–11	15
(0x052) SEQ_CONVSTEP1_ADC0_CH_SEL[3:0]	0–11	15
(0x053) SEQ_CONVSTEP2_ADC0_CH_SEL[3:0]	0–11	15
(0x054) SEQ_CONVSTEP3_ADC0_CH_SEL[3:0]	0–11	15
(0x055) SEQ_CONVSTEP4_ADC0_CH_SEL[3:0]	0–11	15
(0x056) SEQ_CONVSTEP5_ADC0_CH_SEL[3:0]	0–11	15
(0x057) SEQ_CONVSTEP6_ADC0_CH_SEL[3:0]	0–11	15
(0x058) SEQ_CONVSTEP7_ADC0_CH_SEL[3:0]	0–11	15
(0x059) SEQ_CONVSTEP8_ADC0_CH_SEL[3:0]	0–11	15
(0x05A) SEQ_CONVSTEP9_ADC0_CH_SEL[3:0]	0–11	15
(0x05B) SEQ_CONVSTEP10_ADC0_CH_SEL[3:0]	0–11	15
(0x05C) SEQ_CONVSTEP11_ADC0_CH_SEL[3:0]	0–11	15
(0x05D) SEQ_CONVSTEP12_ADC0_CH_SEL[3:0]	0–11	15
(0x05E) SEQ_CONVSTEP13_ADC0_CH_SEL[3:0]	0–11	15
(0x05F) SEQ_CONVSTEP14_ADC0_CH_SEL[3:0]	0–11	15
(0x060) SEQ_CONVSTEP15_ADC0_CH_SEL[3:0]	0–11	15

Register Name	Accepted Values	Default Value
SEQ_CONVSTEPX_ADC0_CH_SEL[3:0]	1111	No Channel selected
	0000	CH0
	0001	CH1
	0010	CH2
	0011	CH3
	0100	CH4
	0101	CH5
	0110	CH6
	0111	CH7
	1011	CH8
	1000	VCCM
	1001	VCC
	1010	VCCAUX

Table 2.10. SEQ_CONVSTEPX_ADC1_CH_SEL Register Details

Register Name	Accepted Values	Default Value
(0x061) SEQ_CONVSTEP0_ADC1_CH_SEL[3:0]	0–11	15
(0x062) SEQ_CONVSTEP1_ADC1_CH_SEL[3:0]	0–11	15
(0x063) SEQ_CONVSTEP2_ADC1_CH_SEL[3:0]	0–11	15
(0x064) SEQ_CONVSTEP3_ADC1_CH_SEL[3:0]	0–11	15
(0x065) SEQ_CONVSTEP4_ADC1_CH_SEL[3:0]	0–11	15
(0x066) SEQ_CONVSTEP5_ADC1_CH_SEL[3:0]	0–11	15
(0x067) SEQ_CONVSTEP6_ADC1_CH_SEL[3:0]	0–11	15
(0x068) SEQ_CONVSTEP7_ADC1_CH_SEL[3:0]	0–11	15
(0x069) SEQ_CONVSTEP8_ADC1_CH_SEL[3:0]	0–11	15
(0x06A) SEQ_CONVSTEP9_ADC1_CH_SEL[3:0]	0–11	15
(0x06B) SEQ_CONVSTEP10_ADC1_CH_SEL[3:0]	0–11	15
(0x06C) SEQ_CONVSTEP11_ADC1_CH_SEL[3:0]	0–11	15
(0x06D) SEQ_CONVSTEP12_ADC1_CH_SEL[3:0]	0–11	15
(0x06E) SEQ_CONVSTEP13_ADC1_CH_SEL[3:0]	0–11	15
(0x06F) SEQ_CONVSTEP14_ADC1_CH_SEL[3:0]	0–11	15
(0x070) SEQ_CONVSTEP15_ADC1_CH_SEL[3:0]	0–11	15

Register Name	Accepted Values	Default Value
SEQ_CONVSTEPX_ADC1_CH_SEL[3:0]	1111	No Channel selected
	0000	CH0
	0001	CH1
	0010	CH2
	0011	CH3
	0100	CH4
	0101	CH5
	0110	CH6
	0111	CH7
	1011	CH8
	1000	VCCIO1
	1001	VCCIO0
	1010	DTR

Table 2.11. SEQ_CONVSTEPX_RPT_NUM Register Details

Register Name	Accepted Values (Repeat Number)	Default Value
(0x071) SEQ_CONVSTEP0_RPT_NUM[7:0]	1–128	1
(0x072) SEQ_CONVSTEP1_RPT_NUM[7:0]	1–128	1
(0x073) SEQ_CONVSTEP2_RPT_NUM[7:0]	1–128	1
(0x074) SEQ_CONVSTEP3_RPT_NUM[7:0]	1–128	1
(0x075) SEQ_CONVSTEP4_RPT_NUM[7:0]	1–128	1
(0x076) SEQ_CONVSTEP5_RPT_NUM[7:0]	1–128	1
(0x077) SEQ_CONVSTEP6_RPT_NUM[7:0]	1–128	1
(0x078) SEQ_CONVSTEP7_RPT_NUM[7:0]	1–128	1
(0x079) SEQ_CONVSTEP8_RPT_NUM[7:0]	1–128	1
(0x07A) SEQ_CONVSTEP9_RPT_NUM[7:0]	1–128	1
(0x07B) SEQ_CONVSTEP10_RPT_NUM[7:0]	1–128	1
(0x07C) SEQ_CONVSTEP11_RPT_NUM[7:0]	1–128	1
(0x07D) SEQ_CONVSTEP12_RPT_NUM[7:0]	1–128	1
(0x07E) SEQ_CONVSTEP13_RPT_NUM[7:0]	1–128	1
(0x07F) SEQ_CONVSTEP14_RPT_NUM[7:0]	1–128	1
(0x080) SEQ_CONVSTEP15_RPT_NUM[7:0]	1–128	1

Table 2.12. ADCX_CHY_OVER_VOLT_EN Register Details

Register Name	Bit Value	Channel
(0x081) ADC0_CH0_OVER_VOLT_EN[0]	1 – enable; 0 – disable	ADC0 Ch0
(0x082) ADC0_CH1_OVER_VOLT_EN[1]	1 – enable; 0 – disable	ADC0 Ch1
(0x083) ADC0_CH2_OVER_VOLT_EN[2]	1 – enable; 0 – disable	ADC0 Ch2
(0x084) ADC0_CH3_OVER_VOLT_EN[3]	1 – enable; 0 – disable	ADC0 Ch3
(0x085) ADC0_CH4_OVER_VOLT_EN[4]	1 – enable; 0 – disable	ADC0 Ch4
(0x086) ADC0_CH5_OVER_VOLT_EN[5]	1 – enable; 0 – disable	ADC0 Ch5
(0x087) ADC0_CH6_OVER_VOLT_EN[6]	1 – enable; 0 – disable	ADC0 Ch6
(0x088) ADC0_CH7_OVER_VOLT_EN[7]	1 – enable; 0 – disable	ADC0 Ch7
(0x089) ADC0_CH8_OVER_VOLT_EN[8]	1 – enable; 0 – disable	ADC0 VCCM
(0x08A) ADC0_CH9_OVER_VOLT_EN[9]	1 – enable; 0 – disable	ADC0 VCC
(0x08B) ADC0_CH10_OVER_VOLT_EN[10]	1 – enable; 0 – disable	ADC0 VCCAUX
(0x08C) ADC0_CH11_OVER_VOLT_EN[11]	1 – enable; 0 – disable	ADC0 Dp/Dn
(0x08D) ADC1_CH0_OVER_VOLT_EN[0]	1 – enable; 0 – disable	ADC1 Ch0
(0x08E) ADC1_CH1_OVER_VOLT_EN[1]	1 – enable; 0 – disable	ADC1 Ch1
(0x08F) ADC1_CH2_OVER_VOLT_EN[2]	1 – enable; 0 – disable	ADC1 Ch2
(0x090) ADC1_CH3_OVER_VOLT_EN[3]	1 – enable; 0 – disable	ADC1 Ch3
(0x091) ADC1_CH4_OVER_VOLT_EN[4]	1 – enable; 0 – disable	ADC1 Ch4
(0x092) ADC1_CH5_OVER_VOLT_EN[5]	1 – enable; 0 – disable	ADC1 Ch5
(0x093) ADC1_CH6_OVER_VOLT_EN[6]	1 – enable; 0 – disable	ADC1 Ch6
(0x094) ADC1_CH7_OVER_VOLT_EN[7]	1 – enable; 0 – disable	ADC1 Ch7
(0x095) ADC1_CH8_OVER_VOLT_EN[8]	1 – enable; 0 – disable	ADC1 VCCIO1
(0x096) ADC1_CH9_OVER_VOLT_EN[9]	1 – enable; 0 – disable	ADC1 VCCIO0
(0x097) ADC1_CH10_OVER_VOLT_EN[10]	1 – enable; 0 – disable	ADC1 DTR
(0x098) ADC1_CH11_OVER_VOLT_EN[11]	1 – enable; 0 – disable	ADC1 Dp/Dn

Table 2.13. ADCX_CHY_OVER_VOLT_AL_LIMIT Register Details

Register Name	Allowable Values	Default Value
(0x099) ADC0_CH0_OVER_VOLT_AL_LIMIT[11:0]	0–4095	1
(0x09A) ADC0_CH1_OVER_VOLT_AL_LIMIT[11:0]	0–4095	1
(0x09B) ADC0_CH2_OVER_VOLT_AL_LIMIT[11:0]	0–4095	1
(0x09C) ADC0_CH3_OVER_VOLT_AL_LIMIT[11:0]	0–4095	1
(0x09D) ADC0_CH4_OVER_VOLT_AL_LIMIT[11:0]	0–4095	1
(0x09E) ADC0_CH5_OVER_VOLT_AL_LIMIT[11:0]	0–4095	1
(0x09F) ADC0_CH6_OVER_VOLT_AL_LIMIT[11:0]	0–4095	1
(0x0A0) ADC0_CH7_OVER_VOLT_AL_LIMIT[11:0]	0–4095	1
(0x0A1) ADC0_CH8_OVER_VOLT_AL_LIMIT[11:0]	0–4095	1
(0x0A2) ADC0_CH9_OVER_VOLT_AL_LIMIT[11:0]	0–4095	1
(0x0A3) ADC0_CH10_OVER_VOLT_AL_LIMIT[11:0]	0–4095	1
(0x0A4) ADC0_CH11_OVER_VOLT_AL_LIMIT[11:0]	0–4095	1
(0x0A5) ADC1_CH0_OVER_VOLT_AL_LIMIT[11:0]	0–4095	1
(0x0A6) ADC1_CH1_OVER_VOLT_AL_LIMIT[11:0]	0–4095	1
(0x0A7) ADC1_CH2_OVER_VOLT_AL_LIMIT[11:0]	0–4095	1
(0x0A8) ADC1_CH3_OVER_VOLT_AL_LIMIT[11:0]	0–4095	1
(0x0A9) ADC1_CH4_OVER_VOLT_AL_LIMIT[11:0]	0–4095	1
(0x0AA) ADC1_CH5_OVER_VOLT_AL_LIMIT[11:0]	0–4095	1
(0x0AB) ADC1_CH6_OVER_VOLT_AL_LIMIT[11:0]	0–4095	1
(0x0AC) ADC1_CH7_OVER_VOLT_AL_LIMIT[11:0]	0–4095	1
(0x0AD) ADC1_CH8_OVER_VOLT_AL_LIMIT[11:0]	0–4095	1
(0x0AE) ADC1_CH9_OVER_VOLT_AL_LIMIT[11:0]	0–4095	1
(0x0AF) ADC1_CH10_OVER_VOLT_AL_LIMIT[11:0]	0–4095	1
(0x0B0) ADC1_CH11_OVER_VOLT_AL_LIMIT[11:0]	0–4095	1

Table 2.14. ADCX_CHY_OVER_EVENT_NUM Register Details

Register Name	Allowable Values	Default Value
(0x0B1) ADC0_CH0_OVER_EVENT_NUM[2:0]	1–4	1
(0x0B2) ADC0_CH1_OVER_EVENT_NUM[2:0]	1–4	1
(0x0B3) ADC0_CH2_OVER_EVENT_NUM[2:0]	1–4	1
(0x0B4) ADC0_CH3_OVER_EVENT_NUM[2:0]	1–4	1
(0x0B5) ADC0_CH4_OVER_EVENT_NUM[2:0]	1–4	1
(0x0B6) ADC0_CH5_OVER_EVENT_NUM[2:0]	1–4	1
(0x0B7) ADC0_CH6_OVER_EVENT_NUM[2:0]	1–4	1
(0x0B8) ADC0_CH7_OVER_EVENT_NUM[2:0]	1–4	1
(0x0B9) ADC0_CH8_OVER_EVENT_NUM[2:0]	1–4	1
(0x0BA) ADC0_CH9_OVER_EVENT_NUM[2:0]	1–4	1
(0x0BB) ADC0_CH10_OVER_EVENT_NUM[2:0]	1–4	1
(0x0BC) ADC0_CH11_OVER_EVENT_NUM[2:0]	1–4	1
(0x0BD) ADC1_CH0_OVER_EVENT_NUM[2:0]	1–4	1
(0x0BE) ADC1_CH1_OVER_EVENT_NUM[2:0]	1–4	1
(0x0BF) ADC1_CH2_OVER_EVENT_NUM[2:0]	1–4	1
(0x0C0) ADC1_CH3_OVER_EVENT_NUM[2:0]	1–4	1
(0x0C1) ADC1_CH4_OVER_EVENT_NUM[2:0]	1–4	1
(0x0C2) ADC1_CH5_OVER_EVENT_NUM[2:0]	1–4	1
(0x0C3) ADC1_CH6_OVER_EVENT_NUM[2:0]	1–4	1

Register Name	Allowable Values	Default Value
(0x0C4) ADC1_CH7_OVER_EVENT_NUM[2:0]	1–4	1
(0x0C5) ADC1_CH8_OVER_EVENT_NUM[2:0]	1–4	1
(0x0C6) ADC1_CH9_OVER_EVENT_NUM[2:0]	1–4	1
(0x0C7) ADC1_CH10_OVER_EVENT_NUM[2:0]	1–4	1
(0x0C8) ADC1_CH11_OVER_EVENT_NUM[2:0]	1–4	1

Table 2.15. ADCX_CHY_OVER_STICKY_OUT Register Details

Register Name	Bit Value	Channel
(0x0C9) ADC0_CH0_OVER_STICKY_OUT[0]	1 – enable; 0 – disable	ADC0 Ch0
(0x0CA) ADC0_CH1_OVER_STICKY_OUT[1]	1 – enable; 0 – disable	ADC0 Ch1
(0x0CB) ADC0_CH2_OVER_STICKY_OUT[2]	1 – enable; 0 – disable	ADC0 Ch2
(0x0CC) ADC0_CH3_OVER_STICKY_OUT[3]	1 – enable; 0 – disable	ADC0 Ch3
(0x0CD) ADC0_CH4_OVER_STICKY_OUT[4]	1 – enable; 0 – disable	ADC0 Ch4
(0x0CE) ADC0_CH5_OVER_STICKY_OUT[5]	1 – enable; 0 – disable	ADC0 Ch5
(0x0CF) ADC0_CH6_OVER_STICKY_OUT[6]	1 – enable; 0 – disable	ADC0 Ch6
(0x0D0) ADC0_CH7_OVER_STICKY_OUT[7]	1 – enable; 0 – disable	ADC0 Ch7
(0x0D1) ADC0_CH8_OVER_STICKY_OUT[8]	1 – enable; 0 – disable	ADC0 VCCM
(0x0D2) ADC0_CH9_OVER_STICKY_OUT[9]	1 – enable; 0 – disable	ADC0 VCC
(0x0D3) ADC0_CH10_OVER_STICKY_OUT[10]	1 – enable; 0 – disable	ADC0 VCCAUX
(0x0D4) ADC0_CH11_OVER_STICKY_OUT[11]	1 – enable; 0 – disable	ADC0 Dp/Dn
(0x0D5) ADC1_CH0_OVER_STICKY_OUT[0]	1 – enable; 0 – disable	ADC1 Ch0
(0x0D6) ADC1_CH1_OVER_STICKY_OUT[1]	1 – enable; 0 – disable	ADC1 Ch1
(0x0D7) ADC1_CH2_OVER_STICKY_OUT[2]	1 – enable; 0 – disable	ADC1 Ch2
(0x0D8) ADC1_CH3_OVER_STICKY_OUT[3]	1 – enable; 0 – disable	ADC1 Ch3
(0x0D9) ADC1_CH4_OVER_STICKY_OUT[4]	1 – enable; 0 – disable	ADC1 Ch4
(0x0DA) ADC1_CH5_OVER_STICKY_OUT[5]	1 – enable; 0 – disable	ADC1 Ch5
(0x0DB) ADC1_CH6_OVER_STICKY_OUT[6]	1 – enable; 0 – disable	ADC1 Ch6
(0x0DC) ADC1_CH7_OVER_STICKY_OUT[7]	1 – enable; 0 – disable	ADC1 Ch7
(0x0DD) ADC1_CH8_OVER_STICKY_OUT[8]	1 – enable; 0 – disable	ADC1 VCCIO1
(0x0DE) ADC1_CH9_OVER_STICKY_OUT[9]	1 – enable; 0 – disable	ADC1 VCCIO0
(0x0DF) ADC1_CH10_OVER_STICKY_OUT[10]	1 – enable; 0 – disable	ADC1 DTR
(0x0E0) ADC1_CH11_OVER_STICKY_OUT[11]	1 – enable; 0 – disable	ADC1 Dp/Dn

Table 2.16. ADCX_CHY_UNDER_VOLT_EN Register Details

Register Name	Bit Value	Channel
(0x0E1) ADC0_CH0_UNDER_VOLT_EN[0]	1 – enable; 0 – disable	ADC0 Ch0
(0x0E2) ADC0_CH1_UNDER_VOLT_EN[1]	1 – enable; 0 – disable	ADC0 Ch1
(0x0E3) ADC0_CH2_UNDER_VOLT_EN[2]	1 – enable; 0 – disable	ADC0 Ch2
(0x0E4) ADC0_CH3_UNDER_VOLT_EN[3]	1 – enable; 0 – disable	ADC0 Ch3
(0x0E5) ADC0_CH4_UNDER_VOLT_EN[4]	1 – enable; 0 – disable	ADC0 Ch4
(0x0E6) ADC0_CH5_UNDER_VOLT_EN[5]	1 – enable; 0 – disable	ADC0 Ch5
(0x0E7) ADC0_CH6_UNDER_VOLT_EN[6]	1 – enable; 0 – disable	ADC0 Ch6
(0x0E8) ADC0_CH7_UNDER_VOLT_EN[7]	1 – enable; 0 – disable	ADC0 Ch7
(0x0E9) ADC0_CH8_UNDER_VOLT_EN[8]	1 – enable; 0 – disable	ADC0 VCCM
(0x0EA) ADC0_CH9_UNDER_VOLT_EN[9]	1 – enable; 0 – disable	ADC0 VCC
(0x0EB) ADC0_CH10_UNDER_VOLT_EN[10]	1 – enable; 0 – disable	ADC0 VCCAUX
(0x0EC) ADC0_CH11_UNDER_VOLT_EN[11]	1 – enable; 0 – disable	ADC0 Dp/Dn
(0x0ED) ADC1_CH0_UNDER_VOLT_EN[0]	1 – enable; 0 – disable	ADC1 Ch0
(0x0EE) ADC1_CH1_UNDER_VOLT_EN[1]	1 – enable; 0 – disable	ADC1 Ch1
(0x0EF) ADC1_CH2_UNDER_VOLT_EN[2]	1 – enable; 0 – disable	ADC1 Ch2
(0x0F0) ADC1_CH3_UNDER_VOLT_EN[3]	1 – enable; 0 – disable	ADC1 Ch3
(0x0F1) ADC1_CH4_UNDER_VOLT_EN[4]	1 – enable; 0 – disable	ADC1 Ch4
(0x0F2) ADC1_CH5_UNDER_VOLT_EN[5]	1 – enable; 0 – disable	ADC1 Ch5
(0x0F3) ADC1_CH6_UNDER_VOLT_EN[6]	1 – enable; 0 – disable	ADC1 Ch6
(0x0F4) ADC1_CH7_UNDER_VOLT_EN[7]	1 – enable; 0 – disable	ADC1 Ch7
(0x0F5) ADC1_CH8_UNDER_VOLT_EN[8]	1 – enable; 0 – disable	ADC1 VCCIO1
(0x0F6) ADC1_CH9_UNDER_VOLT_EN[9]	1 – enable; 0 – disable	ADC1 VCCIO0
(0x0F7) ADC1_CH10_UNDER_VOLT_EN[10]	1 – enable; 0 – disable	ADC1 DTR
(0x0F8) ADC1_CH11_UNDER_VOLT_EN[11]	1 – enable; 0 – disable	ADC1 Dp/Dn

Table 2.17. ADCX_CHY_UNDER_VOLT_AL_LIMIT Register Details

Register Name	Allowable Values	Default Value
(0x0F9) ADC0_CH0_UNDER_VOLT_AL_LIMIT[11:0]	0–4095	1
(0x0FA) ADC0_CH1_UNDER_VOLT_AL_LIMIT[11:0]	0–4095	1
(0x0FB) ADC0_CH2_UNDER_VOLT_AL_LIMIT[11:0]	0–4095	1
(0x0FC) ADC0_CH3_UNDER_VOLT_AL_LIMIT[11:0]	0–4095	1
(0x0FD) ADC0_CH4_UNDER_VOLT_AL_LIMIT[11:0]	0–4095	1
(0x0FE) ADC0_CH5_UNDER_VOLT_AL_LIMIT[11:0]	0–4095	1
(0x0FF) ADC0_CH6_UNDER_VOLT_AL_LIMIT[11:0]	0–4095	1
(0x100) ADC0_CH7_UNDER_VOLT_AL_LIMIT[11:0]	0–4095	1
(0x101) ADC0_CH8_UNDER_VOLT_AL_LIMIT[11:0]	0–4095	1
(0x102) ADC0_CH9_UNDER_VOLT_AL_LIMIT[11:0]	0–4095	1
(0x103) ADC0_CH10_UNDER_VOLT_AL_LIMIT[11:0]	0–4095	1
(0x104) ADC0_CH11_UNDER_VOLT_AL_LIMIT[11:0]	0–4095	1
(0x105) ADC1_CH0_UNDER_VOLT_AL_LIMIT[11:0]	0–4095	1
(0x106) ADC1_CH1_UNDER_VOLT_AL_LIMIT[11:0]	0–4095	1
(0x107) ADC1_CH2_UNDER_VOLT_AL_LIMIT[11:0]	0–4095	1
(0x108) ADC1_CH3_UNDER_VOLT_AL_LIMIT[11:0]	0–4095	1
(0x109) ADC1_CH4_UNDER_VOLT_AL_LIMIT[11:0]	0–4095	1
(0x10A) ADC1_CH5_UNDER_VOLT_AL_LIMIT[11:0]	0–4095	1
(0x10B) ADC1_CH6_UNDER_VOLT_AL_LIMIT[11:0]	0–4095	1

Register Name	Allowable Values	Default Value
(0x10C) ADC1_CH7_UNDER_VOLT_AL_LIMIT[11:0]	0–4095	1
(0x10D) ADC1_CH8_UNDER_VOLT_AL_LIMIT[11:0]	0–4095	1
(0x10E) ADC1_CH9_UNDER_VOLT_AL_LIMIT[11:0]	0–4095	1
(0x10F) ADC1_CH10_UNDER_VOLT_AL_LIMIT[11:0]	0–4095	1
(0x110) ADC1_CH11_UNDER_VOLT_AL_LIMIT[11:0]	0–4095	1

Table 2.18. ADCX_CHY_UNDER_EVENT_NUM Register Details

Register Name	Allowable Value	Default Value
(0x111) ADC0_CH0_UNDER_EVENT_NUM[2:0]	1–4	1
(0x112) ADC0_CH1_UNDER_EVENT_NUM[2:0]	1–4	1
(0x113) ADC0_CH2_UNDER_EVENT_NUM[2:0]	1–4	1
(0x114) ADC0_CH3_UNDER_EVENT_NUM[2:0]	1–4	1
(0x115) ADC0_CH4_UNDER_EVENT_NUM[2:0]	1–4	1
(0x116) ADC0_CH5_UNDER_EVENT_NUM[2:0]	1–4	1
(0x117) ADC0_CH6_UNDER_EVENT_NUM[2:0]	1–4	1
(0x118) ADC0_CH7_UNDER_EVENT_NUM[2:0]	1–4	1
(0x119) ADC0_CH8_UNDER_EVENT_NUM[2:0]	1–4	1
(0x11A) ADC0_CH9_UNDER_EVENT_NUM[2:0]	1–4	1
(0x11B) ADC0_CH10_UNDER_EVENT_NUM[2:0]	1–4	1
(0x11C) ADC0_CH11_UNDER_EVENT_NUM[2:0]	1–4	1
(0x11D) ADC1_CH0_UNDER_EVENT_NUM[2:0]	1–4	1
(0x11E) ADC1_CH1_UNDER_EVENT_NUM[2:0]	1–4	1
(0x11F) ADC1_CH2_UNDER_EVENT_NUM[2:0]	1–4	1
(0x120) ADC1_CH3_UNDER_EVENT_NUM[2:0]	1–4	1
(0x121) ADC1_CH4_UNDER_EVENT_NUM[2:0]	1–4	1
(0x122) ADC1_CH5_UNDER_EVENT_NUM[2:0]	1–4	1
(0x123) ADC1_CH6_UNDER_EVENT_NUM[2:0]	1–4	1
(0x124) ADC1_CH7_UNDER_EVENT_NUM[2:0]	1–4	1
(0x125) ADC1_CH8_UNDER_EVENT_NUM[2:0]	1–4	1
(0x126) ADC1_CH9_UNDER_EVENT_NUM[2:0]	1–4	1
(0x127) ADC1_CH10_UNDER_EVENT_NUM[2:0]	1–4	1
(0x128) ADC1_CH11_UNDER_EVENT_NUM[2:0]	1–4	1

Table 2.19. ADCX_CHY_UNDER_STICKY_OUT Register Details

Register Name	Bit Value	Channel
(0x129) ADC0_CH0_UNDER_STICKY_OUT[0]	1 – enable; 0 – disable	ADC0 Ch0
(0x12A) ADC0_CH1_UNDER_STICKY_OUT[1]	1 – enable; 0 – disable	ADC0 Ch1
(0x12B) ADC0_CH2_UNDER_STICKY_OUT[2]	1 – enable; 0 – disable	ADC0 Ch2
(0x12C) ADC0_CH3_UNDER_STICKY_OUT[3]	1 – enable; 0 – disable	ADC0 Ch3
(0x12D) ADC0_CH4_UNDER_STICKY_OUT[4]	1 – enable; 0 – disable	ADC0 Ch4
(0x12E) ADC0_CH5_UNDER_STICKY_OUT[5]	1 – enable; 0 – disable	ADC0 Ch5
(0x12F) ADC0_CH6_UNDER_STICKY_OUT[6]	1 – enable; 0 – disable	ADC0 Ch6
(0x130) ADC0_CH7_UNDER_STICKY_OUT[7]	1 – enable; 0 – disable	ADC0 Ch7
(0x131) ADC0_CH8_UNDER_STICKY_OUT[8]	1 – enable; 0 – disable	ADC0 VCCM
(0x132) ADC0_CH9_UNDER_STICKY_OUT[9]	1 – enable; 0 – disable	ADC0 VCC
(0x133) ADC0_CH10_UNDER_STICKY_OUT[10]	1 – enable; 0 – disable	ADC0 VCCAUX
(0x134) ADC0_CH11_UNDER_STICKY_OUT[11]	1 – enable; 0 – disable	ADC0 Dp/Dn
(0x135) ADC1_CH0_UNDER_STICKY_OUT[0]	1 – enable; 0 – disable	ADC1 Ch0
(0x136) ADC1_CH1_UNDER_STICKY_OUT[1]	1 – enable; 0 – disable	ADC1 Ch1
(0x137) ADC1_CH2_UNDER_STICKY_OUT[2]	1 – enable; 0 – disable	ADC1 Ch2
(0x138) ADC1_CH3_UNDER_STICKY_OUT[3]	1 – enable; 0 – disable	ADC1 Ch3
(0x139) ADC1_CH4_UNDER_STICKY_OUT[4]	1 – enable; 0 – disable	ADC1 Ch4
(0x13A) ADC1_CH5_UNDER_STICKY_OUT[5]	1 – enable; 0 – disable	ADC1 Ch5
(0x13B) ADC1_CH6_UNDER_STICKY_OUT[6]	1 – enable; 0 – disable	ADC1 Ch6
(0x13C) ADC1_CH7_UNDER_STICKY_OUT[7]	1 – enable; 0 – disable	ADC1 Ch7
(0x13D) ADC1_CH8_UNDER_STICKY_OUT[8]	1 – enable; 0 – disable	ADC1 VCCIO1
(0x13E) ADC1_CH9_UNDER_STICKY_OUT[9]	1 – enable; 0 – disable	ADC1 VCCIO0
(0x13F) ADC1_CH10_UNDER_STICKY_OUT[10]	1 – enable; 0 – disable	ADC1 DTR
(0x140) ADC1_CH11_UNDER_STICKY_OUT[11]	1 – enable; 0 – disable	ADC1 Dp/Dn

Table 2.20. LMMI_ADC0_CH_SEL and LMMI_ADC1_CH_SEL Register Details

LMMI_ADC0_CH_SEL	
Value	**Selected Input Channel**
0000	ADC0 Ch0
0001	ADC0 Ch1
0010	ADC0 Ch2
0011	ADC0 Ch3
0100	ADC0 Ch4
0101	ADC0 Ch5
0110	ADC0 Ch6
0111	ADC0 Ch7
1000	ADC0 VCC
1001	ADC0 VCCM
1010	ADC0 VCCAUX
1011	ADC0 Dp/Dn

LMMI_ADC1_CH_SEL	
Value	**Selected Input Channel**
0000	ADC1 Ch0
0001	ADC1 Ch1
0010	ADC1 Ch2
0011	ADC1 Ch3
0100	ADC1 Ch4
0101	ADC1 Ch5
0110	ADC1 Ch6
0111	ADC1 Ch7
1000	ADC1 VCCIO0
1001	ADC1 VCCIO1
1010	ADC1 DTR
1011	ADC1 Dp/Dn

Table 2.21. LMMI_INT_STATUS_REG Register Details

Bit	Bit Value	Channel
0	0 – No interrupt; 1 – Interrupt pending	ADC0 Ch0
1	0 – No interrupt; 1 – Interrupt pending	ADC0 Ch1
2	0 – No interrupt; 1 – Interrupt pending	ADC0 Ch2
3	0 – No interrupt; 1 – Interrupt pending	ADC0 Ch3
4	0 – No interrupt; 1 – Interrupt pending	ADC0 Ch4
5	0 – No interrupt; 1 – Interrupt pending	ADC0 Ch5
6	0 – No interrupt; 1 – Interrupt pending	ADC0 Ch6
7	0 – No interrupt; 1 – Interrupt pending	ADC0 Ch7
8	0 – No interrupt; 1 – Interrupt pending	ADC0 VCCM
9	0 – No interrupt; 1 – Interrupt pending	ADC0 VCC
10	0 – No interrupt; 1 – Interrupt pending	ADC0 VCCAUX
11	0 – No interrupt; 1 – Interrupt pending	ADC0 Dp/Dn
12	0 – No interrupt; 1 – Interrupt pending	ADC1 Ch0
13	0 – No interrupt; 1 – Interrupt pending	ADC1 Ch1
14	0 – No interrupt; 1 – Interrupt pending	ADC1 Ch2
15	0 – No interrupt; 1 – Interrupt pending	ADC1 Ch3
16	0 – No interrupt; 1 – Interrupt pending	ADC1 Ch4
17	0 – No interrupt; 1 – Interrupt pending	ADC1 Ch5
18	0 – No interrupt; 1 – Interrupt pending	ADC1 Ch6
19	0 – No interrupt; 1 – Interrupt pending	ADC1 Ch7
20	0 – No interrupt; 1 – Interrupt pending	ADC1 VCCIO1
21	0 – No interrupt; 1 – Interrupt pending	ADC1 VCCIO0
22	0 – No interrupt; 1 – Interrupt pending	ADC1 DTR
23	0 – No interrupt; 1 – Interrupt pending	ADC1 Dp/Dn
24 - 31	**Reserved**	

Table 2.22. LMMI_INT_EN_REG Register Details

Bit	Bit Value	Channel
0	0 – No interrupt; 1 – Interrupt pending	ADC0 Ch0
1	0 – No interrupt; 1 – Interrupt pending	ADC0 Ch1
2	0 – No interrupt; 1 – Interrupt pending	ADC0 Ch2
3	0 – No interrupt; 1 – Interrupt pending	ADC0 Ch3
4	0 – No interrupt; 1 – Interrupt pending	ADC0 Ch4
5	0 – No interrupt; 1 – Interrupt pending	ADC0 Ch5
6	0 – No interrupt; 1 – Interrupt pending	ADC0 Ch6
7	0 – No interrupt; 1 – Interrupt pending	ADC0 Ch7
8	0 – No interrupt; 1 – Interrupt pending	ADC0 VCCM
9	0 – No interrupt; 1 – Interrupt pending	ADC0 VCC
10	0 – No interrupt; 1 – Interrupt pending	ADC0 VCCAUX
11	0 – No interrupt; 1 – Interrupt pending	ADC0 Dp/Dn
12	0 – No interrupt; 1 – Interrupt pending	ADC1 Ch0
13	0 – No interrupt; 1 – Interrupt pending	ADC1 Ch1
14	0 – No interrupt; 1 – Interrupt pending	ADC1 Ch2
15	0 – No interrupt; 1 – Interrupt pending	ADC1 Ch3
16	0 – No interrupt; 1 – Interrupt pending	ADC1 Ch4
17	0 – No interrupt; 1 – Interrupt pending	ADC1 Ch5

Bit	Bit Value	Channel
18	0 – No interrupt; 1 – Interrupt pending	ADC1 Ch6
19	0 – No interrupt; 1 – Interrupt pending	ADC1 Ch7
20	0 – No interrupt; 1 – Interrupt pending	ADC1 VCCIO1
21	0 – No interrupt; 1 – Interrupt pending	ADC1 VCCIO0
22	0 – No interrupt; 1 – Interrupt pending	ADC1 DTR
23	0 – No interrupt; 1 – Interrupt pending	ADC1 Dp/Dn

Table 2.23. LMMI_INT_SET_REG Register Details

Bit	Bit Value	Channel
0	0 – No interrupt; 1 – Interrupt pending	ADC0 Ch0
1	0 – No interrupt; 1 – Interrupt pending	ADC0 Ch1
2	0 – No interrupt; 1 – Interrupt pending	ADC0 Ch2
3	0 – No interrupt; 1 – Interrupt pending	ADC0 Ch3
4	0 – No interrupt; 1 – Interrupt pending	ADC0 Ch4
5	0 – No interrupt; 1 – Interrupt pending	ADC0 Ch5
6	0 – No interrupt; 1 – Interrupt pending	ADC0 Ch6
7	0 – No interrupt; 1 – Interrupt pending	ADC0 Ch7
8	0 – No interrupt; 1 – Interrupt pending	ADC0 VCCM
9	0 – No interrupt; 1 – Interrupt pending	ADC0 VCC
10	0 – No interrupt; 1 – Interrupt pending	ADC0 VCCAUX
11	0 – No interrupt; 1 – Interrupt pending	ADC0 Dp/Dn
12	0 – No interrupt; 1 – Interrupt pending	ADC1 Ch0
13	0 – No interrupt; 1 – Interrupt pending	ADC1 Ch1
14	0 – No interrupt; 1 – Interrupt pending	ADC1 Ch2
15	0 – No interrupt; 1 – Interrupt pending	ADC1 Ch3
16	0 – No interrupt; 1 – Interrupt pending	ADC1 Ch4
17	0 – No interrupt; 1 – Interrupt pending	ADC1 Ch5
18	0 – No interrupt; 1 – Interrupt pending	ADC1 Ch6
19	0 – No interrupt; 1 – Interrupt pending	ADC1 Ch7
20	0 – No interrupt; 1 – Interrupt pending	ADC1 VCCIO1
21	0 – No interrupt; 1 – Interrupt pending	ADC1 VCCIO0
22	0 – No interrupt; 1 – Interrupt pending	ADC1 DTR
23	0 – No interrupt; 1 – Interrupt pending	ADC1 Dp/Dn

2.5. Modules Description

2.5.1. ADC Cores

Two ADC Cores are implemented with SAR (Successive Approximation Register) architecture. Each of the ADC core converts unipolar or bi-polar input signal into 12-bit resolution data with maximum 1 MSPS (Mega Samples Per Second) conversion speed sequentially or simultaneously.

2.5.2. Continuous-time Comparators

Three continuous-time comparators are used to compare three pre-selected GPIO (General Purpose I/O) *gpion_io[0]/gpiop_io[0], gpion_io[1]/gpiop_io[1], gpion_io[2]/gpiop_io[2]* signals or externally bonded *comp1in_io/comp1ip_io, comp2in_io/comp2ip_io*, *comp3in_io/comp3ip_io* signals continuously.

Continuous-time comparators are enabled by checking the *COMP0 Enable*, *COMP1 Enable*, *COMP2 Enable* attributes in the user interface.

2.5.3. ADC Core Auto Calibration Controllers

The ADC's auto-calibration function can calibrate gain and offset errors on start-up. The ADC needs to be offset and gain error calibrated before conversion and calibration is initiated by ADC hardware reset by *reset_n_i* and is signaled complete by *calrdy_o*. The ADC's reference voltage that affects overall ADC performance can be provided by internal reference generation block using current from bandgap or external reference block that has better accuracy than internal reference block. When internal reference is selected, reference voltage is provided from bandgap and has voltage calibration function. When external reference is selected, it has to have at least ± 0.2% accuracy.

2.5.4. Internal Reference Generation Block

Each ADC has selectable reference option between internal reference generator and external reference block. The ADC can convert max 1.8 V input signal with 1.8 V reference voltage and input signal can be converted in unipolar mode or bi-polar mode. In case of unipolar mode, positive input signal needs to be higher than negative input.

The reference voltage of the ADC must be higher than or equal to any voltage applied to any of the channel inputs. This includes the divided-down power supply monitoring channels. If the reference voltage is as little as 0.1 V lower than an applied input, then the ADC result from all channels becomes unreliable.

2.5.5. Sequencer Module

Sequencer Module controls ADC data acquisition process and performs the logic of programmed sequence of tasks which are displayed as *Sequence Conversion Steps* attributes in the user interface. For example, in *Sequence Conversion Step 1* field, two input channels corresponding to ADC0 and ADC1 channels respectively can be selected. There is also an attribute *Repeat Step Number of Times* which defines the number of cycles the *Sequence Conversion Step 1* task should be repeated. There are up to 16 tasks can be enabled in the same way, such as *Sequence Conversion Step 2*, *Sequence Conversion Step 3* and so on. Eventually, all defined sequences of tasks are performed with a single run.

There are also the *Nesting Sequence Steps* attributes affiliated with the *Sequence Conversion Steps* attributes. The *Nesting Sequence Steps* attributes can be attached to the already enabled *Sequence Conversion Step* tasks forcing even more cycles for the *Sequence Conversion Step* tasks. For example, if the user set *Sequence Number Select* to 2 and *Repeat Sequence Number of Times* to 3, then the Sequence Step 2 is repeated three times per each Run.

Figure 2.12 shows the sequence module programming flow chart.

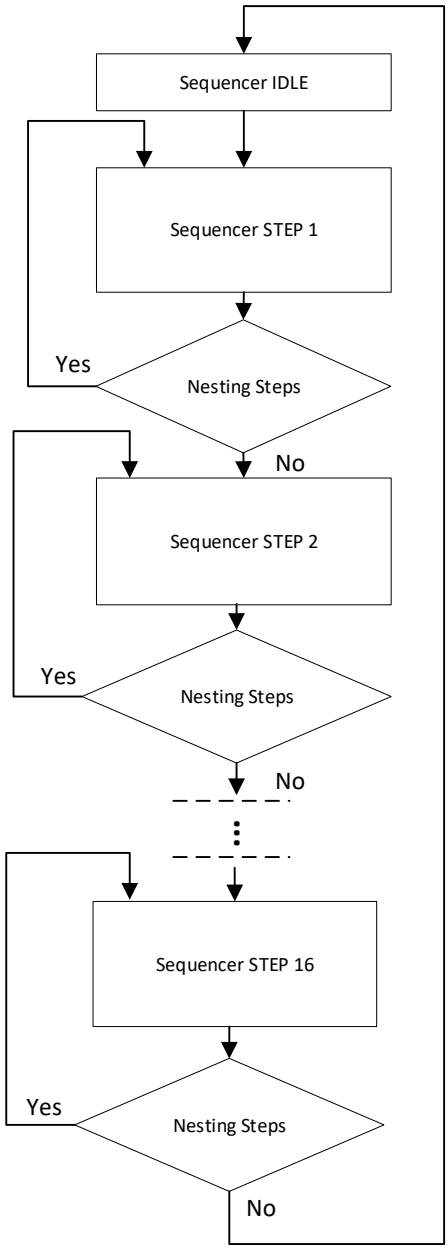

Figure 2.12. Sequencer Module Flow Chart

The *ADCx Channely Configuration* field's attributes, *Channel Enable*, *Minimum Sampling Time*, *Number of Samples to Average on Each Conversion*, *Number of Conversions to Average on Each Readout* are used by Sequencer Module to process ADC output signals. All settings described above are used in conjunction with the *ADCx Channely Configuration* field's attributes set.

For the specific selected ADC Channel, the *Minimum Sampling Time* attribute value defines one conversion time during which the ADC0/ADC1 input signal is tracked.

The *Number of Samples to Average on Each Conversion* attribute defines the number of samples within one conversion to be averaged.

The *Number of Conversions to Average on Each Readout* attribute defines the number of averaged values followed each conversion and which are to be averaged.

The Sequencer Module sequentially repeats the averaging operations within defined sequences.

The Sequencer Module is enabled by checking the *Sequencer Enable* attribute in *Sequence Configuration* field of the user interface and two modes of operation can be set for the Sequencer Module - *Continuous* mode and *Single Pass* mode.

The input *seq_run_i* and output *seq_idle_o* signals are associated with Sequencer Module operation modes.

When Sequencer Module is in continues mode, after the wrapper logic is reset by *rst_n_i* signal the Sequencer Module is pushed into running mode and drives *seq_idle_o* low indicating that the Sequencer Module is in running mode. In this mode the *seq_run_i* input is not applicable.

When the Sequencer Module is in single pass mode, then the *seq_run_i* input becomes valid and applying the positive pulse drives the Sequencer Module into running mode.

After finishing the conversion, the signal *seq_idle_o* goes high indicating that the Sequencer Module is in idle mode.

2.5.6. Alarm Module

Alarm Module supports configurable Over/Under voltage alarm function. Over/Voltage Under/Voltage Alarming function can be activated for each ADC input separately with individual alarm set points. Alarming function also allows enabling temperature alarm feature.

The signal *alarm_event_o[23:0]* indicates all the over/under voltage alarm events detected separately on each ADC channel. The signal *alarm_clear_i* clears detected alarm event indications according to the alarm clear mask applied to the *alarm_clear_mask_i[23:0]* signal where the upper 12-bits matches ADC1[11:0] alarms and the lower 12-bits matches ADC0[11:0] alarms. When the LMMI is enabled then the signal *alarm_clear_i* is not available. Instead, the user can clear alarm function by writing Clear Alarm Register through LMMI.

2.5.7. AXI4-Stream Interface Module

The transmission of ADC channel A/B digitized signals is also supported by AXI4-Stream Interface Module through *axi_tdata_o[20:0]* output signal. The 1-bit *adc_sel* displays the ADC core selected. The 4-bit *ch_addr* signal displays the channel of the selected ADC core where the digitized result is read from. The 16-bit width *dout* signal contains the 12-bit of digitized value of the analog input signal and plus extra 4-bits. This is illustrated in Figure 2.13.

Bit 0	Bit1 – Bit4 (4 bits)	Bit5 – Bit8 (4 bits)	Bit9 – Bit 20 (12 bits)

Figure 2.13. *dout* Signal Bits

Notes on Figure 2.13*:*

	Description
Bit20	ADC Core Select
Bit19 – Bit16	Sequencer Channel Select
Bit15 – Bit12	Sequencer Step Select
Bit11 – Bit0	Digitized Value of Analog Input

The AXI4-Stream Interface is enabled either by enabling the Sequencer Module or by enabling LMMI interface. In case if the LMMI is enabled, but the Sequencer is not, the user can still reconfigure ADC Sequencer Module through LMMI and enable the Sequencer.

2.5.8. LMMI Module

LMMI device module implements memory mapped registers. This interface is suited for IP blocks which use dynamically programmable configuration/control bits and read/write transactions. LMMI is a memory-mapped address/data interface which supports both single and burst transactions with a maximum throughput of one transaction per clock cycle.

A number of registers are initialized via the LMMI interface to ensure that ADC Sequencer Module functions as intended. LMMI defines a standard set of interface signals for register/memory access. The basic requirement is that any additional interface signals must not duplicate functionality described in this spec, that is there should be only one interface (LMMI) for register/memory access.

In ADC Sequencer Module, the LMMI interface is used for controlling dynamically programmable configuration registers, for configuring the Sequencer Module and Alarming Function. The LMMI Module can also provide the output transmission of ADC channel A/B digitized signal through signal *lmmi_rdata_o[31:0]* of LMMI bus.

Setting of the *Local User Interface* attribute in the user interface to “LMMI” mode enables the LMMI interface and at the same time disables ADC Native Interface.

For more information on LMMI, refer to Lattice Memory Mapped Interface and Lattice Interrupt Interface User Guide (FPGA-UG-02039).

2.5.9. APB Module

APB device module implements memory mapped registers. This interface is suited for IP, blocks which needs to be interfaced with an APB Master/Interconnect or thru a high-speed bus (AHB-Lite) via bridge.

In ADC Sequencer Module, the APB interface is used for controlling dynamically programmable configuration registers, for configuring the Sequencer Module and Alarming Function. The LMMI Module can also provide the output transmission of ADC channel A/B digitized signal through signal *apb_prdata_o[31:0]* of the APB bus.

The APB Module is compliant with the APB specification. For more information, refer to AMBA 3 Advance Peripheral Bus Protocol.

3. IP Generation and Evaluation

This chapter provides information on how to generate and synthesize ADC Sequencer Module using Lattice Radiant Software, as well as how to run the simulation. For more information on Lattice Radiant Software, refer to the *Lattice Radiant Software User Guide* and relevant Lattice tutorials.

3.1. Licensing the IP

No license is required for this IP module.

3.2. Generating and Synthesizing the IP

Lattice Radiant Software allows the user to generate and customize modules and IPs and integrate them into the device architecture.

To generate ADC Sequencer Module in Lattice Radiant software:

1. In the Module/IP Block Wizard create a new Lattice Radiant Software project for ADC Sequencer Module.
2. In the dialog box of the Module/IP Block Wizard window, configure ADC Sequencer Module according to custom specifications using drop-down menus and check boxes. As a sample configuration, see Figure 3.1. For configuration options, see Table 2.2.

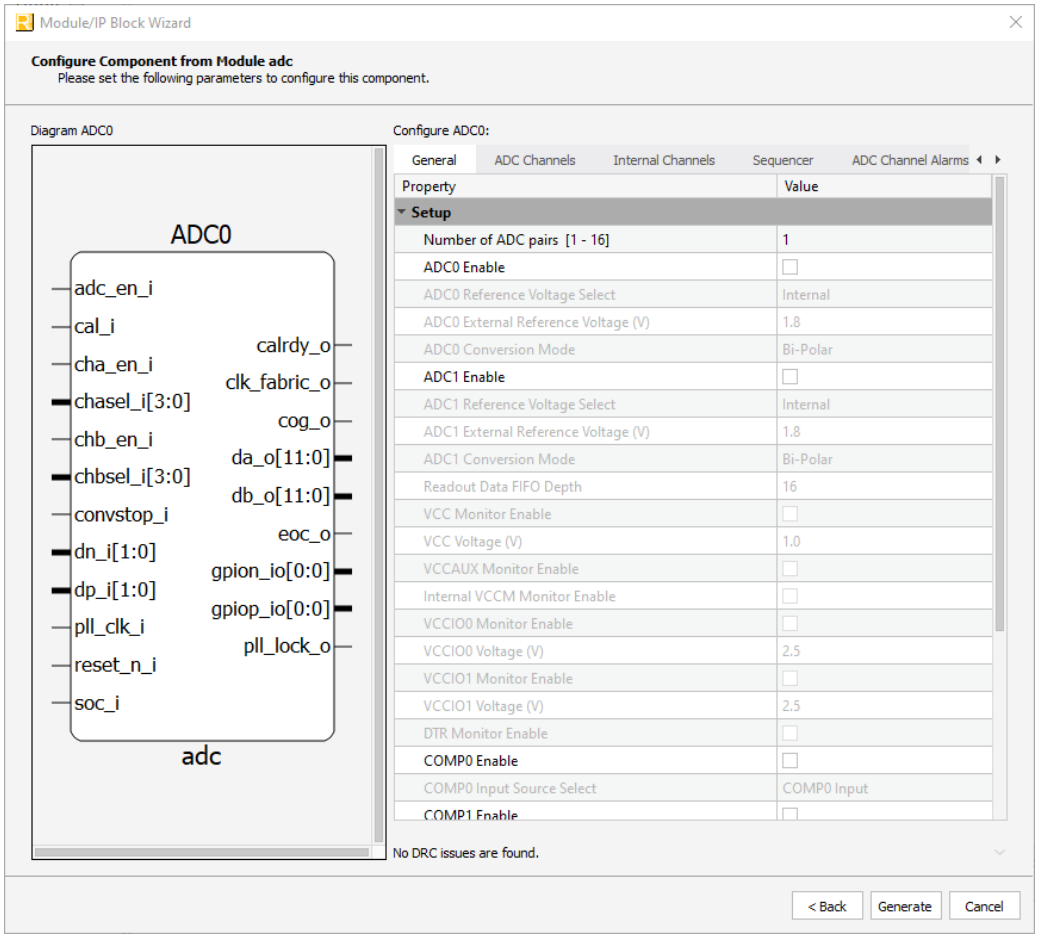

Figure 3.1. Configure Block of ADC Sequencer Module

3. Click **Generate**. The Check Generating Result dialog box opens, showing design block messages and results as shown in Figure 3.2.

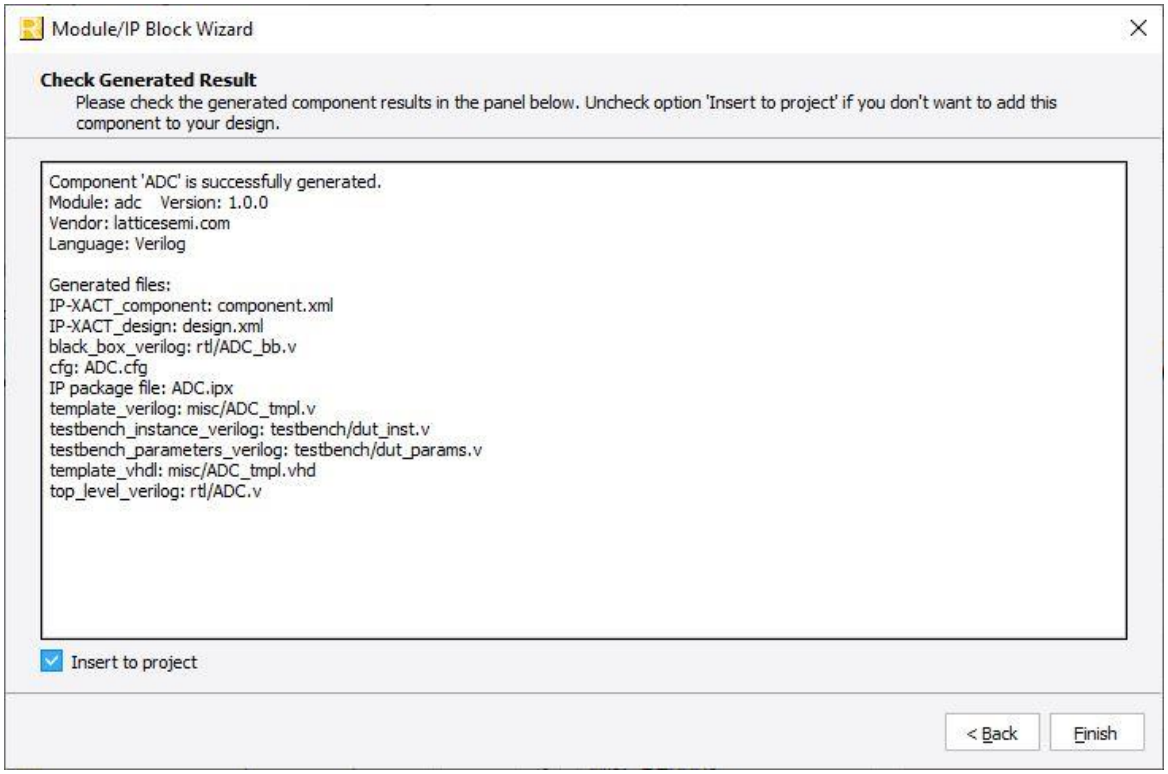

Figure 3.2. Check Generating Result

4. Click **Finish** to generate the Verilog file.
5. Upon generating the desired design, the user can synthesize it by clicking **Synthesize Design** located on the top left corner of the screen, as shown in Figure 3.3.

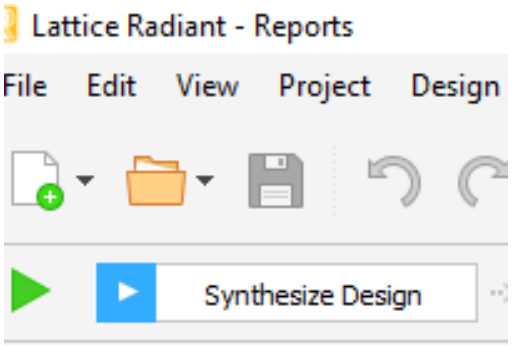

Figure 3.3. Synthesizing Design

3.3. Running the Functional Simulation

To run the simulation, perform the following steps

1. Using the Lattice Radiant software tcl console, go to the newly created *testbench* directory and run the command *source createDefines.tcl* to generate Verilog defines file.
2. Press  button located on the Toolbar on the upper left of the screen to initiate Simulation Wizard, as shown in Figure 3.4.

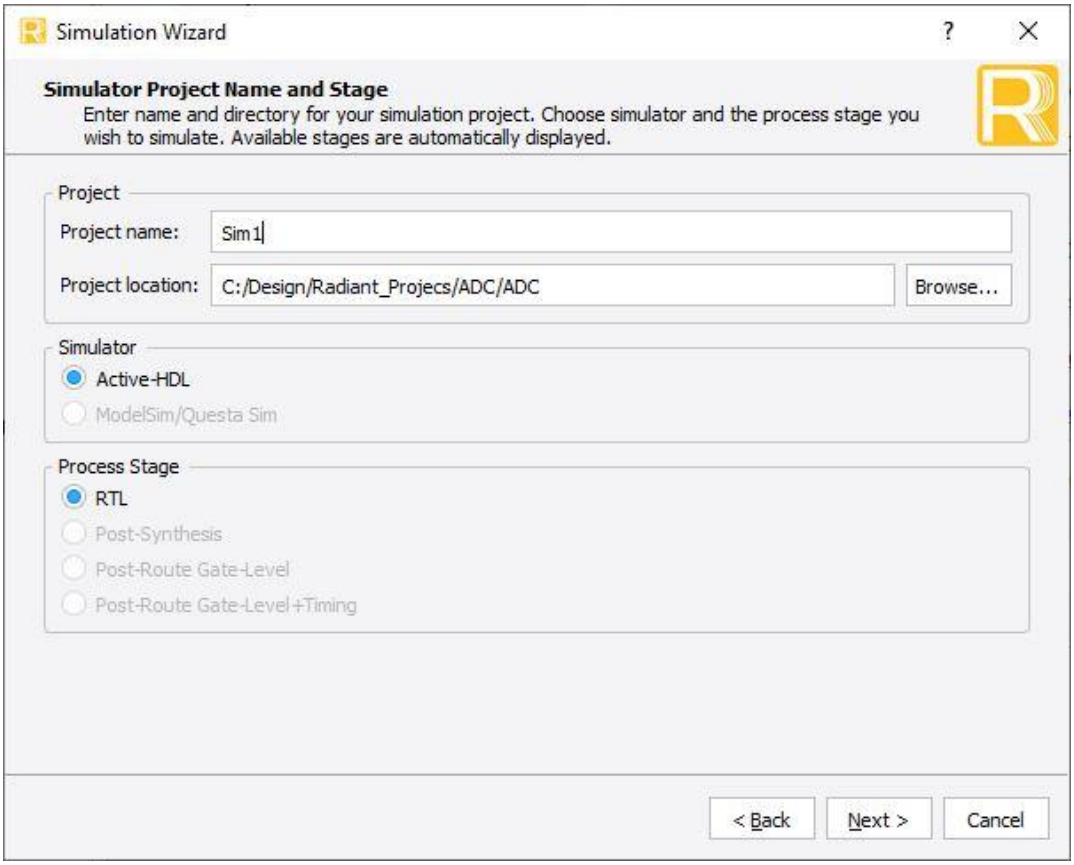

Figure 3.4. Simulation Wizard

3. Double-click **Next** to open the Add and Reorder Source window as shown in Figure 3.5.

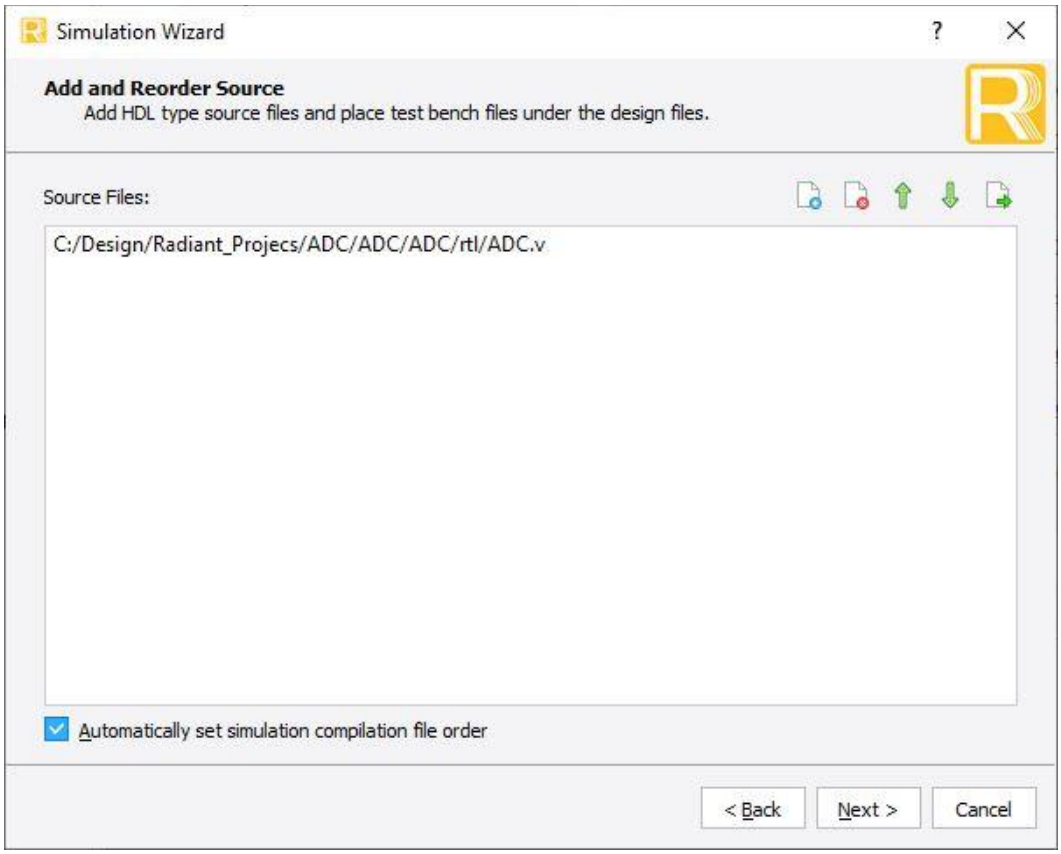

Figure 3.5. Adding and Reordering Source

4. Add *tb_top.v* file from *testbench* directory.
5. Click **Nex**t to run the simulation.

3.4. Core Validation

The functionality of the ADC Sequencer Module is verified through simulation using Lattice's in- house testbench environment and hardware validation.

3.5. Hardware Evaluation

There is no restriction on the hardware evaluation of this module.

Appendix A. Limitations

- LIFCL-17 devices cannot use the ADC because of a missing external reference port.
- Configurations with ADC pairs less than 16 are not supported by the user included testbench.

References

For complete information on Lattice Radiant Project-Based Environment, Design Flow, Implementation Flow and Tasks, as well as on the Simulation Flow, see the Lattice Radiant software user guide.

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, please refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

Revision History

Revision 1.8, February 2023

Section	Change Summary

Functional Description	• Added contents to the ADC0 Reference Voltage Select/ADC1 Reference Voltage Select section.
	• Added adc_sel_i port in Table 2.1. ADC Sequencer Module Ports.
	• Updated Table 2.3. Register Address Map.
	  • Corrected the descriptions of the ADC0_CH8, ADC0_CH9, ADC1_CH8, and ADC1_CH9 registers.
	  • Changed the access type of ADDR_LMMI_ADC_EOC and ADDR_LMMI_ADC_CALRDY from RW to R.
	  • Added ADDR_SEQ_CFG_SEQ_STATE and ADC_CORE_SEL registers.
	• Adjusted VCC, VCCM, VCCIO0, and VCCIO1 indications in the following tables.
	  • Table 2.4. ADC0_CHANNEL_EN and ADC1_CHANNEL_EN Register Details.
	  • Table 2.9. SEQ_CONVSTEPX_ADC0_CH_SEL Register Details.
	  • Table 2.10. SEQ_CONVSTEPX_ADC1_CH_SEL Register Details.
	  • Table 2.12. ADCX_CHY_OVER_VOLT_EN Register Details.
	  • Table 2.15. ADCX_CHY_OVER_STICKY_OUT Register Details.
	  • Table 2.16. ADCX_CHY_UNDER_VOLT_EN Register Details.
	  • Table 2.19. ADCX_CHY_UNDER_STICKY_OUT Register Details.
	  • Table 2.20. LMMI_ADC0_CH_SEL and LMMI_ADC1_CH_SEL Register Details.
	  • Table 2.21. LMMI_INT_STATUS_REG Register Details.
	  • Table 2.22. LMMI_INT_EN_REG Register Details.
	  • Table 2.23. LMMI_INT_SET_REG Register Details.
	• Added contents to the Internal Reference Generation Block section.

Technical Support Assistance	Added reference to the Lattice Answer Database on the Lattice website.

Revision 1.7, November 2022

Section	Change Summary

Functional Description	• Updated description of port names *int_o* and *alarm_event_o[23:0]* in Table 2.1. ADC Sequencer Module Ports.
	• Updated the VCC and VCCM in ADC0 channel and the VCCIO0 and VCCIO1 in ADC1 for below tables:
	  • Table 2.3. Register Address Map
	  • Table 2.4. ADC0_CHANNEL_EN and ADC1_CHANNEL_EN Register Details
	  • Table 2.9. SEQ_CONVSTEPX_ADC0_CH_SEL Register Details
	  • Table 2.10. SEQ_CONVSTEPX_ADC1_CH_SEL Register Details
	  • Table 2.12. ADCX_CHY_OVER_VOLT_EN Register Details
	  • Table 2.15. ADCX_CHY_OVER_STICKY_OUT Register Details
	  • Table 2.16. ADCX_CHY_UNDER_VOLT_EN Register Details
	  • Table 2.19. ADCX_CHY_UNDER_STICKY_OUT Register Details
	  • Table 2.20. LMMI_ADC0_CH_SEL and LMMI_ADC1_CH_SEL Register Details
	  • Table 2.21. LMMI_INT_STATUS_REG Register Details
	  • Table 2.22. LMMI_INT_EN_REG Register Details
	  • Table 2.23. LMMI_INT_SET_REG Register Details

Revision 1.6, January 2022

Section	Change Summary
Functional Description	Removed the *DTR Output Code Values as a Function of Temperature* table.

Revision 1.5, September 2021

Section	Change Summary
Functional Description	Corrected typographical error in Figure 2.13. dout Signal Bits to *Bit9 – Bit 20 (12 bits)* and reordered the bits in the description table (Notes on Figure 2.13).

Revision 1.4, June 2021

Section	Change Summary
All	Minor adjustment in format.
Introduction	Updated content to change information to Lattice Nexus platform.
References	Updated reference to Lattice Radiant software user guide.

Revision 1.3, June 2020

Section	Change Summary
All	• Changed document title to ADC Sequencer Module – Lattice Radiant Software • Added Certus-NX and LFD2NX support. • Updated module name.
Functional Description	• Added ADC Logic Block Clock Frequency (MHz) attribute to Table 2.2. Attribute Table. • Removed statement on enabling DTR from the DTR (Digital Temperature Readout) section.
Appendix A. Limitations	Added this section.
References	Updated reference to Lattice Radiant Software 2.1 User Guide.

Revision 1.2, February 2020

Section	Change Summary
Introduction	Added pin count compatibility under the Features section.
Signal Description	Updated Table 2.1. ADC Sequencer Module Ports. • Changed 15:0 to NUM_PIN-1:0. • Added footnote.
Attribute Summary	Updated Table 2.2. Attribute Table • Added number of ADC pairs as a parameter. • *Number of ADC pairs* selectable values revised to (1 to 16/11 <depending on device>).
Generating and Synthesizing the IP	Updated Figure 3.1. Configure Block of ADC Sequencer Module.

Revision 1.1, December 2019

Section	Change Summary
Acronyms in This Document	Added this section.
All	Minor editorial and formatting changes

Revision 1.0, October 2019

Section	Change Summary
All	Initial release

www.latticesemi.com