iCE40 sysCLOCK PLL Design and Usage Guide

Technical Note

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
CHF	High Frequency Capacitor
CLF	Low Frequency Capacitor
FPGA	Field-Programmable Gate Array
GUI	Graphical User Interface
LSE	Lattice Synthesis Engine
PIO	Programmable Input/Output
PLB	Programmable Logic Block
PLL	Phase Locked Loop
RS	Series Resistor
RTL	Register-Transfer Level

1. Introduction

This technical note discusses the clock resources available in the Lattice Semiconductor (iCE40LP/HX, iCE40LM, iCE40 Ultra™, iCE40 UltraLite™, and iCE40 UltraPlus™). Details are provided for global buffers and sysCLOCK™ PLLs.

The iCE40 devices include an ultra-low power Phase-Locked Loop (PLL) to support a variety of display, imaging and memory interface applications. Table 1.1 shows the number of PLLs in each of the devices in the iCE40 family. For the performance of the PLLs, refer to the device family data sheet.

Table 1.1. Number of PLLs in the iCE40 Device Family

Package	HX1K	HX4K	HX8K
VQ100 100-ball VQFP	0	—	—
CB132 132-ball csBGA	1	2	2
TQ144 144-ball TQFP	1	2	—
CM225 225-ball ucBGA	—	—	2
CT256 256-ball caBGA	—	—	2

Package	LP384	LP640	LP1K	LP4K	LP8K
SQG16 16-ball WLCSP	—	0	—	—	—
SG32 32-ball QFN	0	—	—	—	—
CM36 36-ball ucBGA	0	—	0	—	—
CM49 49-ball ucBGA	0	—	1	—	—
CM81 81-ball ucBGA	—	—	1	1	1
CB81 81-ball csBGA	—	—	0	—	—
QN84 84-ball QFN	—	—	0	—	—
CM121 121-ball ucBGA	—	—	1	2	2
CB121 121-ball csBGA	—	—	1	—	—
CM225 225-ball ucBGA	—	—	—	2	2

Package	LM1K	LM2K	LM4K
SWG25 25-ball WLCSP	0	0	0
CM36 36-ball ucBGA	1	1	1
CM49 49-ball ucBGA	1	1	1

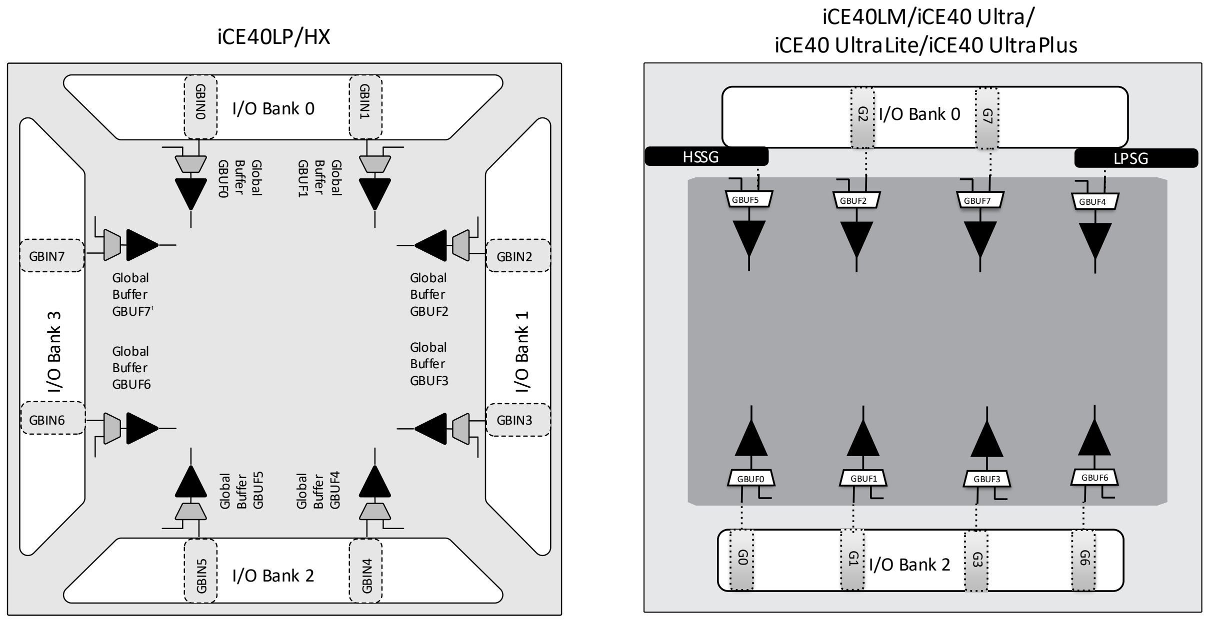
Package	Ultra 1K	Ultra 2K	Ultra 4K
SWG25 25-ball WLCSP	1	1	1

Package	UltraLite 640	UltraLite 1K
SWG16 16-ball WLCSP	1	1
CM36 36-ball ucBGA	1	1

Package	UltraPlus 3K	UltraPlus 5K
UWG30 30-ball WLCSP	1	1
SG48 48-pin QFN	1	1

2. Global Routing Resources

The iCE40 device has eight high drive buffers called global buffers (GBUFx). These are connected to eight low-skew global lines, designed primarily for clock distribution, but also useful for other high-fanout signals such as set/reset and enable signals.



1. GBUF7 and its associated PIO are best for direct differential clock inputs

Figure 2.1. High-drive, Low-skew, High-fanout Global Buffer Routing Resources

The input (sources) to the GBUFx can be:

- Global buffer inputs (GBINx, Gx)[1]
- Programmable interconnect[2]
- PLL output[2]
- Programmable input/output block (PIO)[2]
- Strobe Generators (HSSG, LPSG on iCE40LM devices)
- On-chip Oscillator (LFOSC, HFOSC on UltraPlus devices)

Notes:

1. The associated GBINx/Gx pin represents the best pin to drive a global buffer from an external source. To determine which GBIN pin can be used as a PLL Reference Clock Input, refer to the Hardware Design Considerations section.
2. In iCEcube2, to use a global buffer along with a user interface or PIO, use the SB_GB primitive if it is not inferred automatically.

2.1. Verilog Instantiation (for iCEcube2 only)

```
SB_GB My_Global_Buffer_i (// required for a user’s internally generated FPGA signal that is
heavily loaded and requires global buffering. For example, a user’s logic-generated clock.
.USER_SIGNAL_TO_GLOBAL_BUFFER (Users_internal_Clk),
.GLOBAL_BUFFER_OUTPUT ( Global_Buffered_User_Signal) );
```

2.2. VHDL Instantiation (for iCEcube2 only)

```
component SB_GB
port (
USER_SIGNAL_TO_GLOBAL_BUFFER:input std_logic;
GLOBAL_BUFFER_OUTPUT:output std_logic);
end component;
My_Global_Buffer_i: SB_GB
port map (
USER_SIGNAL_TO_GLOBAL_BUFFER=>Users_internal_Clk,
BUFFER=>Global_Buffered_User_Signal);
```

When using iCEcube2, you may refer to the iCE Technology Library document for more details on device primitives. SB_GB primitive is not available in the Lattice Radiant® software but Global Buffers are automatically inferred when GBIN ports are used as a clock input. Non-direct access ports can be forced to use a primary clock spine through general routing by using the *Use Primary Net* option in the Device Constraint Editor tool in the Lattice Radiant software.

If not used in an application, individual global buffers are turned off to save power.

Table 2.1 lists the connections between a specific global buffer and the inputs on a Programmable Logic Block (PLB).

Refer to the Architecture section of iCE40 Family data sheets for more information on PLBs. All global buffers optionally connect to all clock inputs. Any four of the eight global buffers can drive logic inputs to a PLB. Even-numbered global buffers optionally drive the reset input to a PLB. Similarly, odd-numbered buffers optionally drive the PLB clock-enabled input.

Table 2.1. Global Buffer Connections to a Programmable Logic Block

Global Buffer	LUT Inputs	Clock	Clock Enable	Reset
GBUF0	Yes, any 4 of 8 GBUF Inputs	Yes	—	—
GBUF1		Yes	Yes	Yes
GBUF2		Yes	—	—
GBUF3		Yes	Yes	Yes
GBUF4		Yes	—	—
GBUF5		Yes	Yes	Yes
GBUF6		Yes	—	—
GBUF7		Yes	Yes	Yes

Table 2.2 lists the connections between a specific global buffer and the inputs on a Programmable I/O (PIO) pins. Although there is no direct connection between a global buffer and a PIO output, such a connection is possible by first connecting through a PLB LUT4 function. Again, all global buffers optionally drive all clock inputs. However, even-numbered global buffers optionally drive the clock-enable input on a PIO pair.

Table 2.2. Global Buffer Connections to Programmable I/O Pair

Global Buffer	Output Connections	Input Clock	Output Clock	Clock Enable
GBUF0	None (connect through PLB LUT)	Yes	Yes	Yes
GBUF1		Yes	Yes	—
GBUF2		Yes	Yes	Yes
GBUF3		Yes	Yes	—
GBUF4		Yes	Yes	Yes
GBUF5		Yes	Yes	—
GBUF6		Yes	Yes	Yes
GBUF7		Yes	Yes	—

3. iCE40 sysCLOCK PLL

The iCE40 Phase-Locked Loop (PLL) provides two sets of outputs and a variety of user-synthesizable clock frequencies, along with custom phase delays. The PLL in the iCE40 device can be configured and utilized with the help of software macros or the PLL Module Generation utilities available in iCEcube2 and Lattice Radiant software (see the Module Generation section). These utilities help you to quickly configure the desired settings with the help of a graphical user interface (GUI) and generate Verilog code which configures the PLL macros. Figure 3.1 shows the iCE40 sys-CLOCK PLL block diagram.

3.1. iCE40 sysCLOCK PLL Features

The PLL provides the following functions in iCE40 applications:

- Generates a new output clock frequency
  - Clock multiplication
  - Clock division
- De-skews or phase-aligns an output clock to the input reference clock
  - Faster input set-up time
  - Faster clock-to-output time
- Corrects output clock to have nearly a 50% duty cycle, which is important for Double Data Rate (DDR) applications
- Optionally phase shifts the output clock relative to the input reference clock
  - Optimal data sampling within the available bit period
  - Fixed quadrant phase shifting at 0°, 90°
  - Optional fine delay adjustments of up to 2.5 ns (typical) in 150 ps increments (typical)

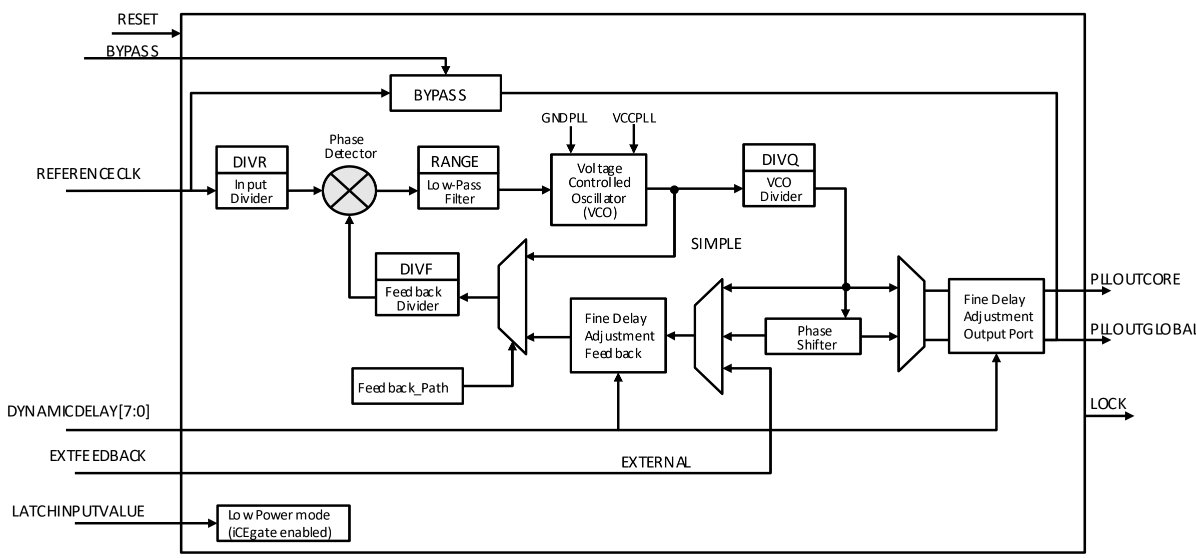


Figure 3.1. iCE40 UltraPlus Phase-Locked Loop (sysCLOCK PLL) Block Diagram

3.2. Signals

Table 3.1 lists the signal names, direction, and function of each connection to the PLL. Some of the signals have an associated attribute or property. Table 3.1. lists these attributes or properties, and the allowable settings for each attribute.

Note: Signals and attribute settings of PLL primitives are for reference only. It is recommended to generate a PLL module with the user interface-based PLL Module Generator or the IP Catalog as explained in the Module Generation section.

Table 3.1. PLL Signals

Signal Name (iCEcube2)	Signal Name (Lattice Radiant)	Direction	Description
REFERENCECLK	ref_clk_i	Input	Input reference clock
RESET	rst_n_i	Input	Active LOW reset
BYPASS	bypass_i	Input	When FEEDBACK_PATH is set to SIMPLE, the BYPASS control selects which clock signal connects to the PLLOUT output. 0 = PLL generated signal 1 = ref_clk_i
EXTFEEDBACK	feedback_i	Input	External feedback input to PLL Enabled when the EXTERNAL_DIVIDE_FACTOR attribute is set to an integer.
DYNAMICDELAY[3:0]	dynamic_delay_i[3:0]	Input	Fine delay adjustment control inputs Enabled when DELAY_ADJUSTMENT_MODE_FEEDBACK is set to DYNAMIC.
DYNAMICDELAY[7:4]/[3:0]	dynamic_delay_i[7:4]/[3:0]	Input	Fine delay adjustment control inputs Enabled when DELAY_ADJUSTMENT_MODE_RELATIVE is set to DYNAMIC. Note: Index is [3:0] when DELAY_ADJUSTMENT_MODE_FEEDBACK is set to FIXED.
LATCHINPUTVALUE	latch_i	Input	When enabled, forces the PLL into low-power mode PLL output is held static at the last input clock value. Set ENABLE ICEGATE_PORTA or PORTB to *1* to enable.
PLLOUTGLOBALA	outglobal_o	Output	Output from the Phase-Locked Loop (PLL) Port A Drives a global clock network on the FPGA. The port has optimal connections to global clock buffers GBUF4 and GBUF5.
PLLOUTCOREA	outcore_o	Output	Output clock generated by the PLL Port A Drives regular FPGA routing. The frequency generated on this output is the same as the frequency of the clock signal generated on the outglobal_o port.
PLLOUTGLOBALB	outglobalb_o	Output	Output from the Phase-Locked Loop (PLL) Port B Drives a global clock network on the FPGA. The port has optimal connections to global clock buffers GBUF4 and GBUF5.
PLLOUTCOREB	outcoreb_o	Output	Output clock generated by the PLL Port B Drives regular FPGA routing. The frequency generated on this output is the same as the frequency of the clock signal generated on the outglobalb_o port.
LOCK	lock_o	Output	When High, indicates that the PLL output is phase aligned or locked to the input reference clock.

Table 3.2. PLL Attributes and Settings in PLL Macro*

Parameter Name	Description	Parameter Value	Description
FEEDBACK_PATH	Selects the feedback path to the PLL.	SIMPLE	Feedback is internal to the PLL directly from VCO.
		DELAY	Feedback is internal to the PLL through the Fine Delay Adjust Block.
		PHASE_AND_DELAY	Feedback is internal to the PLL through the Phase Shifter and the Fine Delay Adjust Block.
DELAY_ADJUSTMENT _MODE_FEEDBACK	Selects the mode for the Fine Delay Adjust block in the feedback path.	FIXED	Delay of the Fine Delay Adjust Block is fixed. The value is specified by the FDA_FEEDBACK parameter setting.
		DYNAMIC	Delay of Fine Delay Adjust Block is determined by the signal value at the dynamic_delay_i[3:0] pins.
FDA_FEEDBACK	Sets a constant value for the Fine Delay Adjust Block in the feedback path	0, 1, … , 15	The PLLOUTGLOBAL and PLLOUTCORE signals are delay compensated by (n+1)*150 ps, where n = FDA_FEEDBACK only if DELAY_ADJUSTMENT_MODE_ FEEDBACK is set to FIXED.
DELAY_ADJUSTMENT _MODE_RELATIVE	Selects the mode for the Fine Delay Adjust block	FIXED	Delay of the Fine Delay Adjust Block is fixed. The value is specified by the FDA_RELATIVE parameter setting.
		DYNAMIC	Delay of the Fine Delay Adjust Block is determined by the signal value at the dynamic_delay_i[7:4]/[3:0] pins.
FDA_RELATIVE	Sets a constant value for the Fine Delay Adjust Block.	0, 1, … , 15	The PLLOUTGLOBALA and PLLOUTCOREA signals are additionally delayed by (n+1)*150 ps, where n = FDA_RELATIVE. Used if DELAY_ADJUSTMENT_MODE_ RELATIVE is set to FIXED.
SHIFTREG_DIV_MODE	Selects shift register configuration	0, 1	Used when FEEDBACK_PATH is set to PHASE_AND_DELAY. 0 = Divide by 4 1 = Divide by 7
PLLOUT_SELECT	Selects the signal to be output at the PLLOUTCORE and PLLOUTGLOBAL ports	SHIFTREG_0deg	0° phase shift only if the setting of FEEDBACK_PATH is set to PHASE_AND_DELAY.
		SHIFTREG_90deg	90° phase shift only if the setting of FEEDBACK_PATH is PHASE_AND_DELAY and SHIFTREG_DIV_MODE = 0.
		GENCLK	The internally generated PLL frequency is outputted without any phase shift.
		GENCLK_HALF	The internally generated PLL frequency is divided by two and then outputted. No phase shift.
DIVR	REFERENCECLK divider	0, 1, 2, … , 15	These parameters are used to control the output frequency, depending on the FEEDBACK_PATH setting.
DIVF	Feedback divider	0, 1, … , 127	
DIVQ	VCO divider	0, 1, … , 7	
FILTER_RANGE	PLL filter range	0, 1, … , 7	
EXTERNAL_DIVIDE _FACTOR	Divide-by factor of a divider in external feedback path	User specified value. Default = *NONE*	Specified only when there is a user-implemented divider in the external feedback path. FEEDBACK_PATH is overridden when value is set to any integer value.
ENABLE_ICEGATE_PORTA		0	Power-down control disabled

Parameter Name	Description	Parameter Value	Description
	Enables the PLL powerdown control for Port A	1	Power-down controlled by the LATCH input
ENABLE_ICEGATE_PORTB	Enables the PLL powerdown control for Port B	0	Power-down control disabled
		1	Power-down controlled by the LATCH input
FREQUENCY_PIN_REFERENCECLK	Reference clock pin constraint	User specified value. Default = *NONE*	Value is extracted from the input frequency setting.

***Note:** The attributes are automatically configured through the PLL Module Generator.

3.3. Clock Input Requirements

Proper operation requires the following considerations:

- A stable monotonic (single frequency) reference clock input
- The reference clock input must be within the input clock frequency range (FREF), specified in the data sheet.
- The reference clock must have a duty cycle that meets the requirement specified in the data sheet.
- The jitter on the reference input clock must not exceed the limits specified in the data sheet.

3.4. PLL Output Requirements

The PLL output clock, PLLOUT, has the following restrictions:

- The PLLOUT output frequency must be within the limits specified in the data sheet.
- The PLLOUT output is not valid or stable until the PLL LOCK output remains high.

3.5. Functional Description

The PLL optionally multiplies and/or divides the input reference clock to generate a PLLOUT output clock of another frequency. The output frequency depends on the frequency of the REFERENCLK input clock and the settings for the DIVR, DIVF, DIVQ, RANGE, and FEEDBACK_PATH attributes settings, as indicated in Figure 3.1.

The PLL's phase detector and Voltage Controlled Oscillator (VCO) synthesize a new output clock frequency based on the attribute settings. The VCO is an analog circuit and has independent voltage supply and ground connections labeled VCCPLL and GNDPLL.

3.5.1. PLLOUT Frequency for FEEDBACK_PATH = DELAY or PHASE_AND_DELAY

For FEEDBACK_PATH modes DELAY and PHASE_AND_DELAY, the PLLOUT frequency is calculated as per the equation below.

$$F_{PLLOUT} = \frac{F_{REFENCECLK} \times (DIVF + 1)}{DIVR + 1}$$

3.5.2. PLLOUT Frequency for FEEDBACK_PATH = SIMPLE

In the SIMPLE feedback mode, the PLL feedback signal taps directly from the output of the VCO, before the final divider stage. Consequently, the PLL output frequency has an additional divider step, DIVQ, contributed by the final divider step as shown in equation below. (DIVF, DIVQ and DIVR are binary).

$$F_{PLLOUT} = \frac{F_{REFERENCECLK} \times (DIVF + 1)}{2^{(DIVQ)} \times (DIVR + 1)}$$

3.5.3. PLLOUT Frequency for FEEDBACK_PATH = EXTERNAL

For EXTERNAL FEEDBACK_PATH mode, the PLLOUT frequency calculated as per the equation below.

$$F_{PLLOUT} = \frac{F_{REFERENCECLK} \times (DIVF+1) \times EXTDIV}{DIVR+1}$$

3.5.4. Fixed Quadrant Phase Shift

The PLL optional phase feature shifts the PLLOUT output by a specified quadrant or quarter clock cycle as shown in Table 3.3 and Figure 3.2. The quadrant phase shift option is only available when the FEEDBACK_PATH attribute is set to PHASE_AND_DELAY.

Table 3.3. PLL Phase Shift Options

PLLOUT_SELECT	Duty Cycle Correction	Phase Shift	Fraction Clock Cycle
SHIFTREG_0deg	Yes	0°	None
SHIFTREG_90deg	Yes	90°	Quarter Cycle

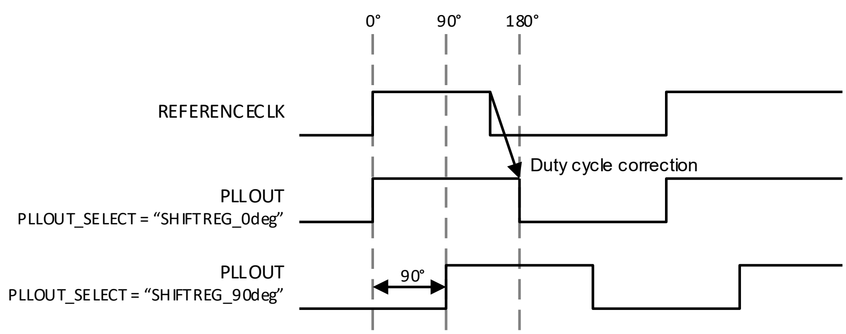


Figure 3.2. Fixed Quadrant Phase Shift Control

Unlike the Fine Delay Adjustment, the quadrant phase shifter always shifts by a fixed phase angle. The resulting phase shift, measured in delay, depends on the clock period and the PLLOUT_PHASE phase shift setting, as shown in the equation below.

$$Delay = \frac{PhaseShift}{360°} \times Clock\_Period$$

3.5.5. Fine Delay Adjustment (FDA)

The PLL provides two optional fine delay adjustment blocks that control the delay of the PLLOUT output relative to the input reference clock, to an external feedback signal, or relative to the selected quadrant phase shifted clock. One FDA is placed in the feedback path, while the other FDA provides delay on the output port directly. If a two-port PLL is used, this additional delay is applied only on Port A. Unlike the Feedback FDA, the output port FDA is not dependent on FEEDBACK_PATH, and can be used even if FEEDBACK_PATH = Simple. The PLL Module Generation utilities provide easy selection of the two fine delay adjust blocks. Figure 3.3 shows the typical first fine delay adjust control block.

The delay is adjusted by selecting one or more of the 16 delay taps inside the fine delay adjustment block. Each tap is approximately 150 ps.

Fine Delay Adjustment (nominal) = (n+1)* 150ps; 0 ≤ n ≤ 15, where *n* is the number of delay taps.

The number of taps can be selected statically (by providing the value within the PLL Module Generation utility), or dynamically by setting the values in DYNAMICDELAY [7:0]. DYNAMICDELAY [3:0] sets the tap numbers for the feedback path fine delay adjustment block while DYNAMICDELAY [7:4] sets values for the output port FDA. Refer to parameters DELAY_ADJUSTMENT_MODE_FEEDBACK and DELAY_ADJUSTMENT_MODE_RELATIVE in Table 3.2 for more details.

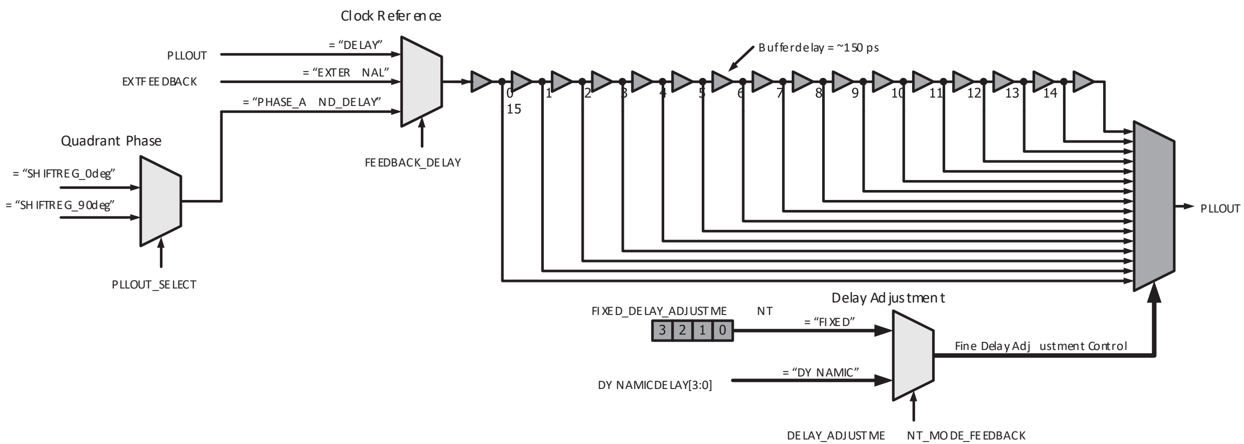


Figure 3.3. Fine Delay Adjust Control

3.5.6. Phase Angle Equivalent

The fine delay adjustment feature injects an actual delay value, rather than a fixed phase angle like the Fixed Quadrant Phase Shift feature. Use the equation below to convert the fine adjustment delay to a resulting phase angle.

$$PhaseShift = \frac{Fine\_Delay\_Adjustment}{ClockPeriod} \times 360°$$

3.5.7. Low Power Mode

The iCE40 sysCLOCK PLL has low operating power by default. The PLL can be dynamically disabled to further reduce power. The low-power mode must first be enabled by setting the ENABLE_ICEGATE attribute to *1*. Once enabled, use the LATCHINPUTVALUE to control the PLL's operation, as shown in Table 3.4. The PLL must reacquire the input clock and LOCK when the LATCHINPUTVALUE returns from *1* to *0*, external feedback is used, and path goes out into the fabric.

Table 3.4. PLL LATCHINPUTVALUE Control

ENABLE_ICEGATE Attribute	LATCHINPUTVALUE Input	Function
0	Don't Care	PLL is always enabled.
1	0	PLL is enabled and operating.
	1	PLL is in low-power mode; PLLOUT output holds last clock state.

4. Module Generation

A graphical user interface-based PLL configuration tool is provided in both iCEcube2 and Lattice Radiant Software. Using these tools, you can configure the iCE40 PLL software macros based on the inputs in the user interface. The resultant HDL code can be used for synthesis. This document uses the Lattice Radiant software version 2.1 and iCEcube2 version 2017-08.

4.1. Using Lattice Radiant Software IP Catalog

Figure 4.1 shows the Start Page of the Lattice Radiant software.

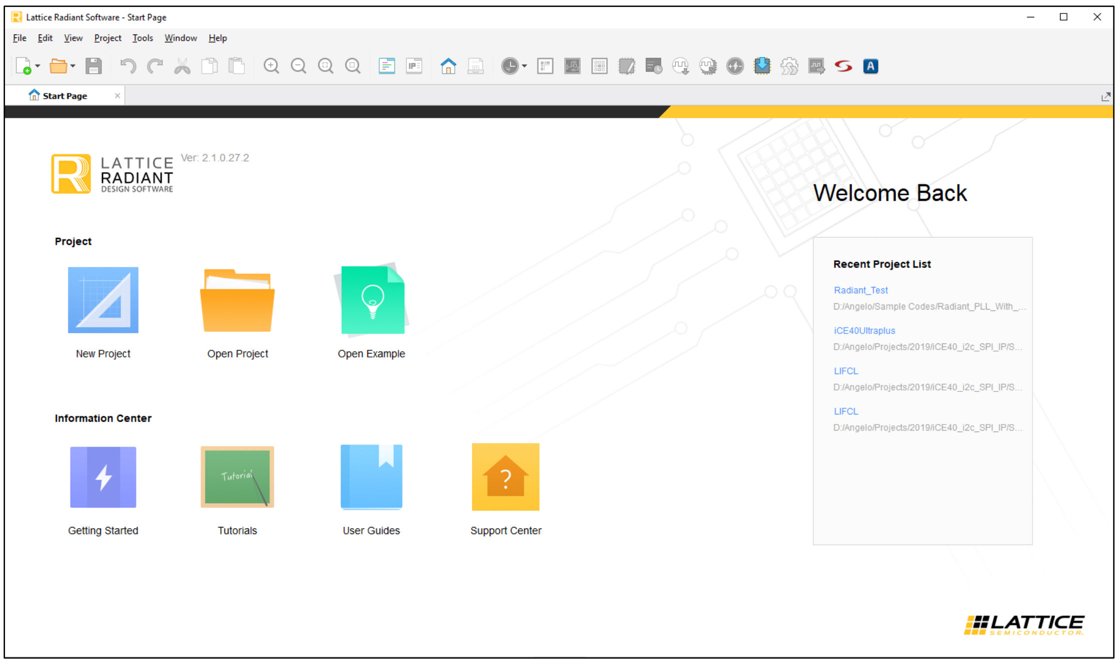


Figure 4.1. Lattice Radiant Software Start Page

To generate the PLL module:

1. Select **New Project** from the Start Page and click **Next**.
2. Provide the project name and directory. Click **Next**.
3. Add the source files if necessary, otherwise, click **Next** to skip this step.
4. In **Select Device** as shown in Figure 4.2, select **iCE40UP** in **Family** and the targeted device in **Device**. Click **Next**.

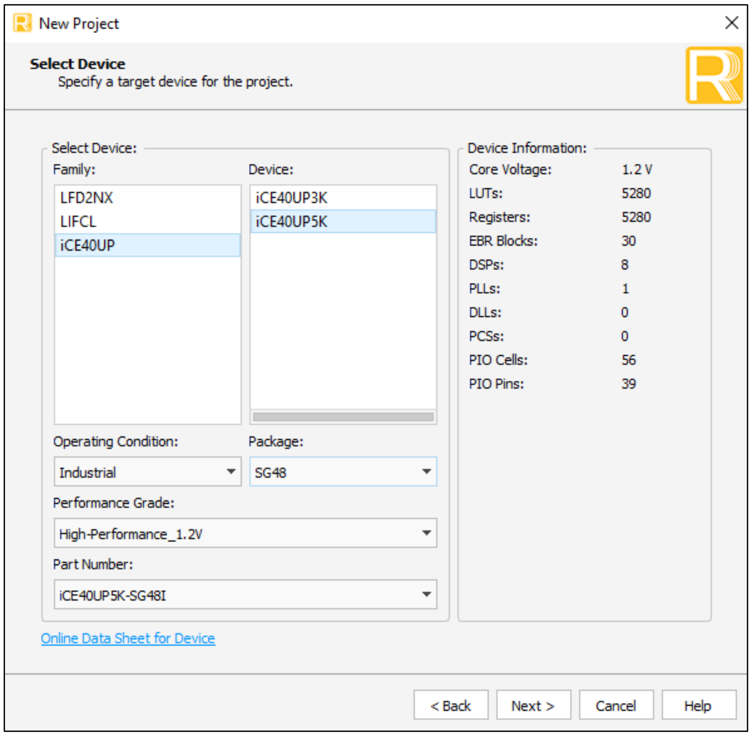


Figure 4.2. Device Family Selection

5. In Select Synthesis Tool, shown in Figure 4.3, select the synthesis tool to use. Click **Next**.

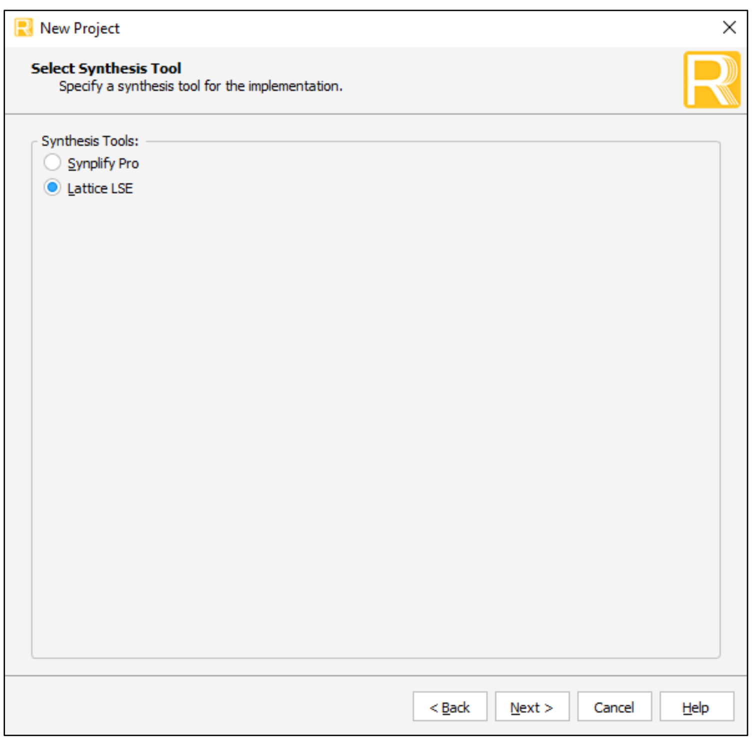


Figure 4.3. Synthesis Tool Selection

6. The project information summary is displayed. If everything is correct, click **Finish** to load the project.
7. In IP Information, shown in Figure 4.4, click IP Catalog on the lower left corner of the window.

8. Double-click PLL under Architecture Module to open the PLL module generator.

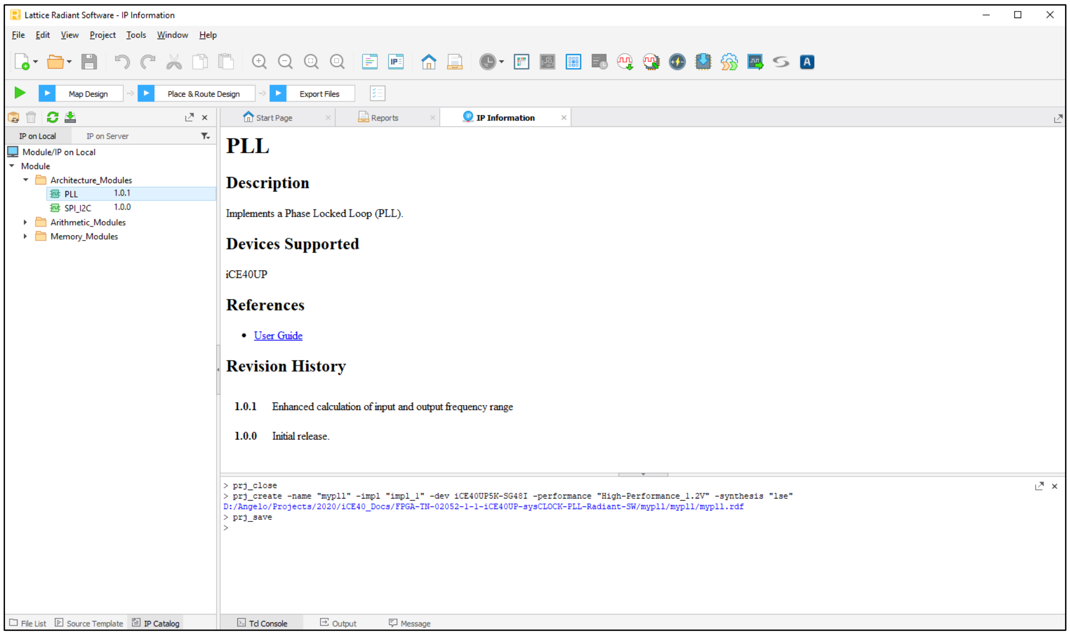


Figure 4.4. IP Catalog

Figure 4.5 shows the PLL configuration interface.

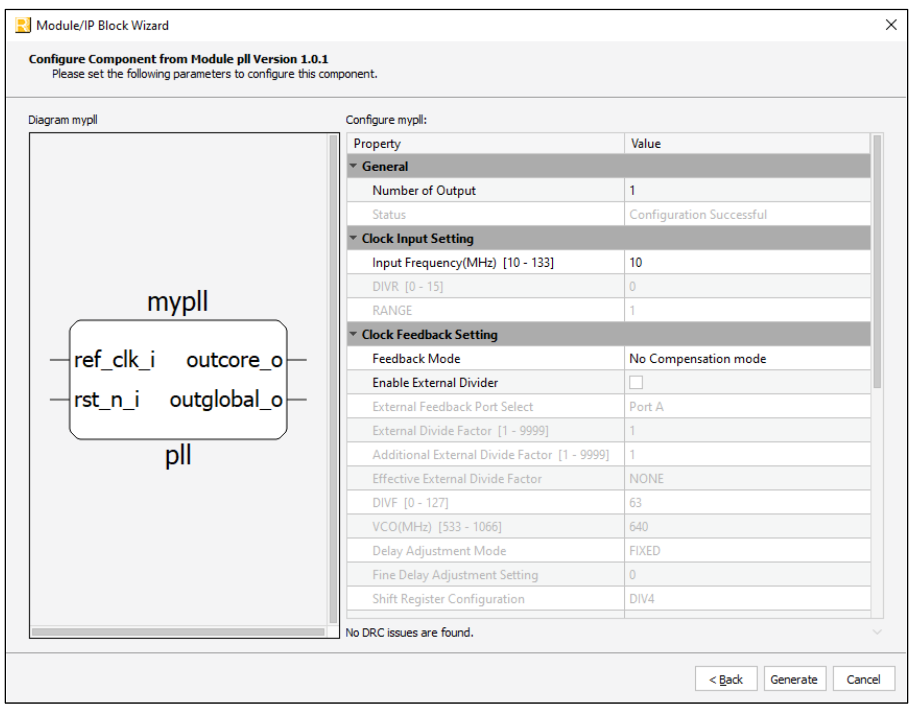


Figure 4.5. PLL Module Generator User Interface

9. Click **the Generate** button if the desired PLL setting is set. A summary of the generated result is shown.
10. If no other changes are needed, click **Finish** to complete the procedure.

Table 4.1. PLL Configuration User Parameters

User Parameter	Description	Value	Description
General			
Number of Output	Setting the value to *1* generates a PLL which drives a single global clock network, as well as regular routing. Setting the value to *2* generates a PLL which drives two global clock networks as well as two regular routing resources.	1	—
		2	—
Clock Input Setting			
Input Frequency (MHz)	PLL reference clock	[10,133]	—
DIVR	Computed reference clock divider value	[0,15]	—
RANGE	Computed PLL filter range	[0,7]	—
Clock Feedback Setting			
Feedback Mode	Feedback path to the PLL	No compensation mode	FEEDBACK_PATH = *SIMPLE*
		Delay compensation using only the Fine Delay Adjustment Block	FEEDBACK_PATH = *DELAY*
		Delay compensation using Phase Shifter and Fine Delay Adjustment Block	FEEDBACK_PATH = *PHASE_AND_DELAY*
Enable External Divider	Feedback path to the PLL is external. This overrides *Feedback Mode* setting.	Enable, Disable	—
External Feedback Port Select	Specifies which PLL output port is linked to external divider circuit. This is only applicable when *Enable External Divider* is enabled.	Port A, Port B	In this scenario, if Port A/B is using either *GENLCK* or *GENCLK_HALF*, the inherent divide factor is included in the computation of *Effective External Divide Factor*.
External Divide Factor	External divider value	[0,∞]	—
Effective External Divide Factor	Actual external divide factor used by PLL	[0,∞]	—
DIVF	Computed feedback divider value	[0,127]	—
VCO(MHz)	Computed VCO frequency	[533,1066]	—
Delay Adjustment Mode	Mode of adjustment for the feedback path	[FIXED, DYNAMIC]	—
Fine Delay Adjustment Setting	Static delay value when *Delay Adjustment Mode* is *FIXED*	[0,15]	—
Shift Register Configuration	Shift register configuration	DIV4	4:1 using *GENCLK* or 2:1 using *GENCLK_HALF*
		DIV7	7:1 using *GENCLK* or 3.5:1 using *GENCLK_HALF*
Phase Shift for Port A	PLL output selection for Port A	*GENCLK, GENCLK_HALF, SHIFTREG_0deg, SHIFTREG_90deg*	Valid selection depends on FEEDBACK_PATH value.

User Parameter	Description	Value	Description
Phase Shift for Port B	PLL output selection for Port B	*GENCLK, GENCLK_HALF, SHIFTREG_0deg, SHIFTREG_90deg*	Valid selection depends on FEEDBACK_PATH value.
PLL Output Setting			
Output Frequency (MHz)	Desired PLL output frequency	[16,275]	—
Actual PLLOUTA Frequency(MHz)	Computed PLL Port A frequency	[16,275]	—
Actual PLLOUTA Frequency(MHz)	Computed PLL Port B frequency	[16,275]	—
Internal PLL Frequency(MHz)	Computed PLL frequency before output divider	[16,275]	—
PLLOUT Tolerance %	Accepted deviation from desired PLL output frequency	[0%, 0.1%, 0.2%, 0.5%, 1%, 2%, 5%, 10%]	—
Actual PLLOUT Tolerance %	Computed deviation from desired PLL output frequency	[0,5]	—
Additional Delay Adjustment Mode	Mode of adjustment for the fine delay adjust block	[FIXED, DYNAMIC]	—
Additional Delay Adjustment Setting	Static delay value when *Additional Delay Adjustment Mode* is *FIXED*	[0,15]	—
DIVQ	Computed VCO divider value	[0,7]	—
Misc			
Enable Lock Port	Enable lock signal	Enable, Disable	—
Enable Bypass Port	Enable bypass control	Enable, Disable	—
Enable ICEGATE Port A	Enable power-down control for Port A	Enable, Disable	—
Enable ICEGATE Port B	Enable power-down control for Port B	Enable, Disable	—
Message			
Status	Indicates possible parameters needed for adjustment to fix flagged DRC errors	Failed, Successful	—

4.1.1. Module Generator Output

The PLL module generator generates two HDL files:

- <module_name>
    - < module _name>.cfg
    - < module _name>.ipx
    - < module _name>_tmpl.v
    - [rtl]
        - < module _name>.v
        - < module _name>_bb.v

<module_name>.cfg

- user configurations file

<module_name>.ipx

- record of generated files

<module_name>_tmpl.v

- instantiation template file

<module_name>.v

- customized generated soft IP

<module_name>_bb.v

- prototype declaration of the instance

4.1.2. Device Constraints

Lattice Radiant software supports automatic device constraint generation for PLL module. Whenever PLL module is instantiated in a design, the tool generates timing constraints based on the set parameters of the device. Reference clock, which is user-defined, is then extracted by the tool to define the PLL reference clock pin. Frequency and phase of generated clocks are obtained automatically from the device. If feedback is internal, the tool uses the delay provided by the device to compute the delay through the PLL. For external feedback, phase difference between reference clock and feedback clock are computed and compensates by subtracting delay.

Consider as an example a PLL module generated with a 10 MHz reference clock frequency and a 40 MHz output. Figure 4.6 shows the synthesis report using Lattice Synthesis Engine (LSE). The automatically generated constraints are shown under *SDC_Constraints*.

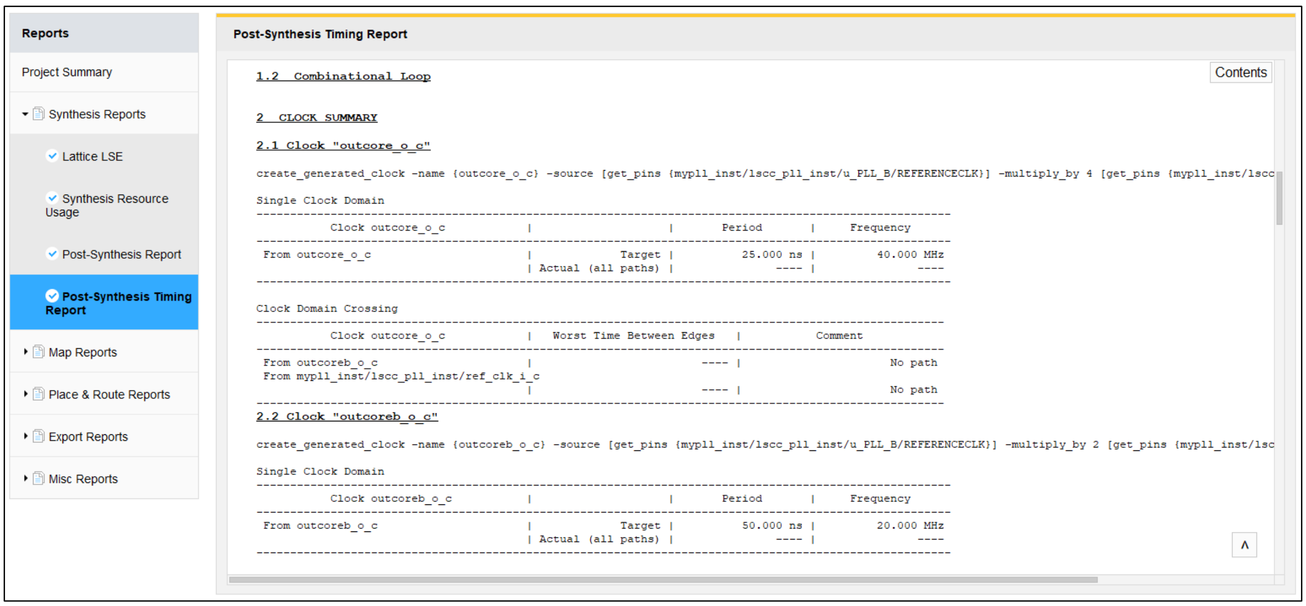


Figure 4.6. Post Synthesis Timing Report

Reference clock constraint with 100 ns period:

```
create_clock -name {lscc_pll_inst/ref_clk_i_c} -period 100 [get_nets ref_clk_i_c]
```

PLLOUTA is *GENCLK* for x4 reference clock multiplier:

```
create_generated_clock -name {outglobal_o_c} -source [get_pins
{lscc_pll_inst/u_PLL_B/REFERENCECLK}] -multiply_by 4 [get_pins
{lscc_pll_inst/u_PLL_B/OUTGLOBAL }]

create_generated_clock -name {outcore_o_c} -source [get_pins
{lscc_pll_inst/u_PLL_B/REFERENCECLK}] -multiply_by 4 [get_pins {lscc_pll_inst/u_PLL_B/OUTCORE
}]
```

PLLOUTB is *GENCLK_HALF* for x2 reference clock multiplier:

```
create_generated_clock -name {outglobalb_o_c} -source [get_pins
{lscc_pll_inst/u_PLL_B/REFERENCECLK}] -multiply_by 2 [get_pins
{lscc_pll_inst/u_PLL_B/OUTGLOBALB }]

create_generated_clock -name {outcoreb_o_c} -source [get_pins
{lscc_pll_inst/u_PLL_B/REFERENCECLK}] -multiply_by 2 [get_pins
{lscc_pll_inst/u_PLL_B/OUTCOREB }]
```

4.1.3. Utilization

The Map Report shows the use of PLL along with other design elements of iCE40 UltraPlus device.

Map

Contents

```
Design Information

Command line:   map pll_test_impl1_syn.udb -o pll_test_impl1.udb -gui

Design Summary
   Number of slice registers:   8 out of  5280 (0%)
   Number of I/O registers:     0 out of    21 (0%)
   Number of LUT4s:             9 out of  5280 (0%)
      Number of logic LUT4s:              5
      Number of inserted feedthru LUT4s:  4
      Number of ripple logic:             0 (0 LUT4s)
   Number of IO sites used:   6 out of 21 (29%)
      Number of IO sites used for general PIOs: 6
      Number of IO sites used for I3Cs: 0 out of 2 (0%)
      Number of IO sites used for PIOs+I3Cs: 6 out of 18 (33%)
      (note: If I3C is not used, its site can be used as general PIO)
      Number of IO sites used for OD+RGB IO buffers: 0 out of 3 (0%)
   Number of DSPs:              0 out of 8 (0%)
   Number of I2Cs:              0 out of 2 (0%)
   Number of HFOSCs:            0 out of 1 (0%)
   Number of LFOSCs:            0 out of 1 (0%)
   Number of LEDDAs:            0 out of 1 (0%)
   Number of RGBAs:             0 out of 1 (0%)
   Number of FILTERs:           0 out of 2 (0%)
   Number of SRAMs:             0 out of 4 (0%)
   Number of WARMBOOTs:         0 out of 1 (0%)
   Number of SPIs:              0 out of 2 (0%)
   Number of EBRs:              0 out of 30 (0%)
   Number of PLLs:              1 out of 1 (100%)
   Number of Clocks:  5
      Pin u_mypll.pll_inst.u_PLLINS_PLL_B_inst/OUTCOREB: 2 loads, 2 rising, 0
     falling (Net: u_mypll/pll_inst/outcoreb)
      Pin u_mypll.pll_inst.u_PLLINS_PLL_B_inst/OUTGLOBALB: 2 loads, 2 rising, 0
     falling (Net: u_mypll/pll_inst/outglobalb)
      Pin u_mypll.pll_inst.u_PLLINS_PLL_B_inst/OUTCORE: 2 loads, 2 rising, 0
     falling (Net: u_mypll/pll_inst/outcore)
      Pin u_mypll.pll_inst.u_PLLINS_PLL_B_inst/OUTGLOBAL: 2 loads, 2 rising, 0
     falling (Net: u_mypll/pll_inst/outglobal)
      Port refclk: 1 loads, 1 rising, 0 falling (Net: u_mypll/pll_inst/refclk_c)
   Number of Clock Enables:  0
   Number of LSRs:  1
      Net reset_N_2: 8 loads, 8 SLICEs
   Top 10 highest fanout non-clock nets:
      Net reset_N_2: 8 loads
      Net r0: 2 loads
      Net r1: 2 loads
      Net r2: 2 loads
      Net r3: 2 loads
      Net u_mypll/pll_inst/reset_c: 2 loads
      Net outb_c: 1 loads


      Net outgb_c: 1 loads
      Net r0_N_4: 1 loads
      Net r1_N_6: 1 loads
```

Figure 4.7. Map Report

4.2. Using iCEcube2 Design Software's PLL Module Generator

Figure 4.8 shows the iceCube2 design software. The PLL module generator user interface can be invoked from the Tool menu.

Figure 4.8. iceCube2 Design Software

Figure 4.9 shows the PLL configuration user interface. Select the device (iCE40 in this case) and other desired operations.

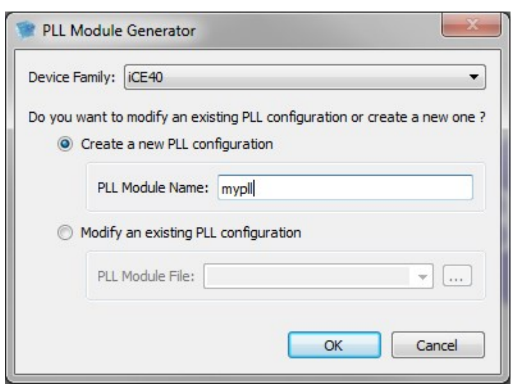


Figure 4.9. PLL Module Generator/Modify Existing PLL Configuration

Click **OK** and the PLL frequency settings window opens, as shown in Figure 4.10.

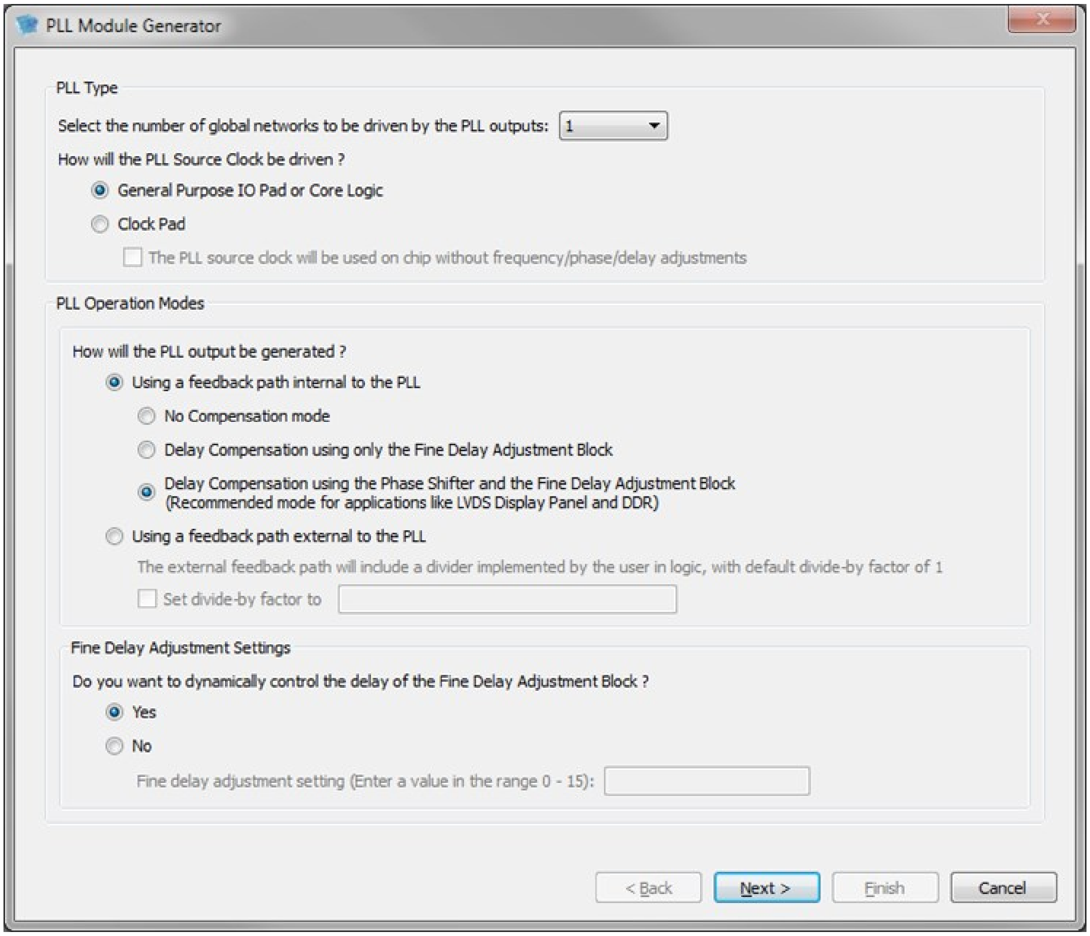


Figure 4.10. Settings Window 1

Refer to Table 4.12 for details on user options. Select desired settings which are self-explanatory. Note that some of the options are only activated when other required selections are made. These settings directly modify the PLL signals and attributes of the PLL software macro, as explained in Table 3.1 and Table 3.2.

Figure 4.11 shows the next setting window.

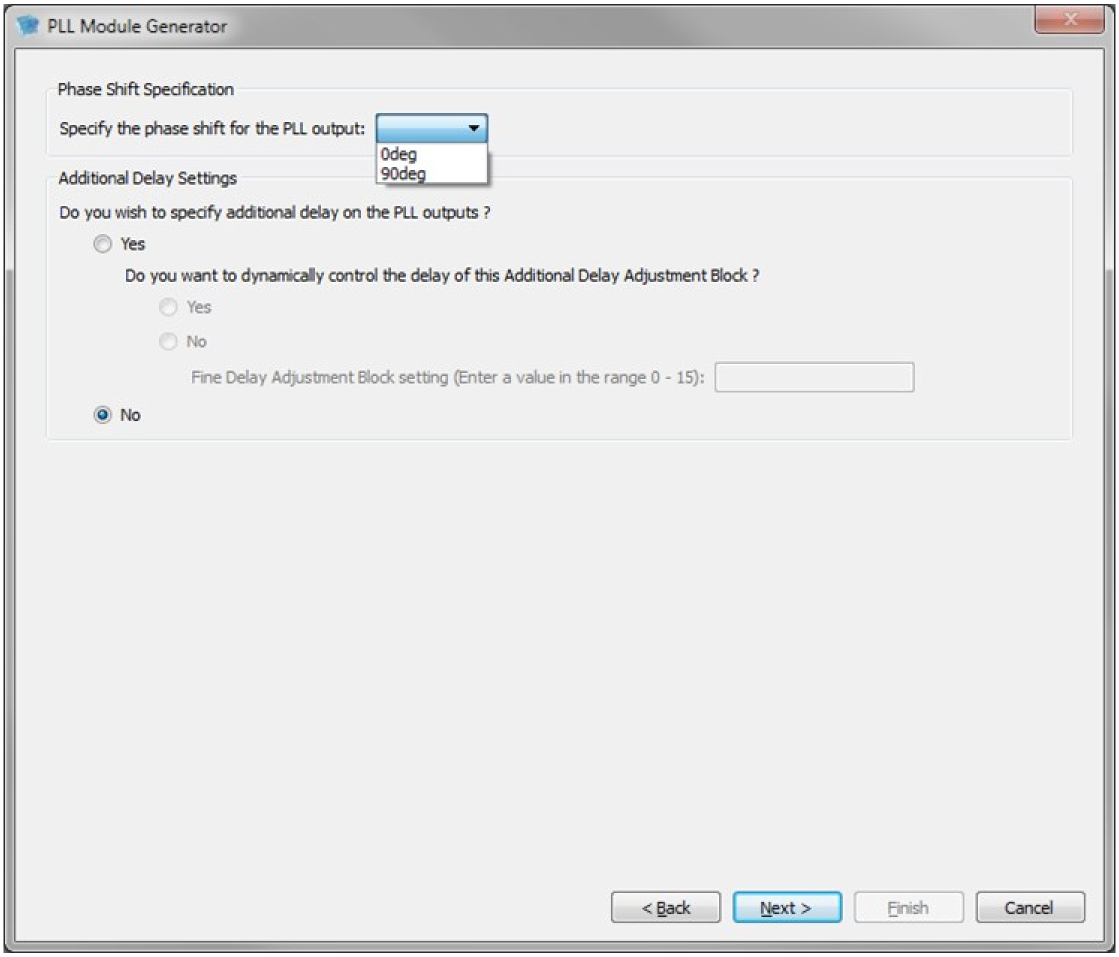


Figure 4.11. Settings Window 2

Select desired values and click **Next**. The last of the settings windows opens, as shown in Figure 4.12.

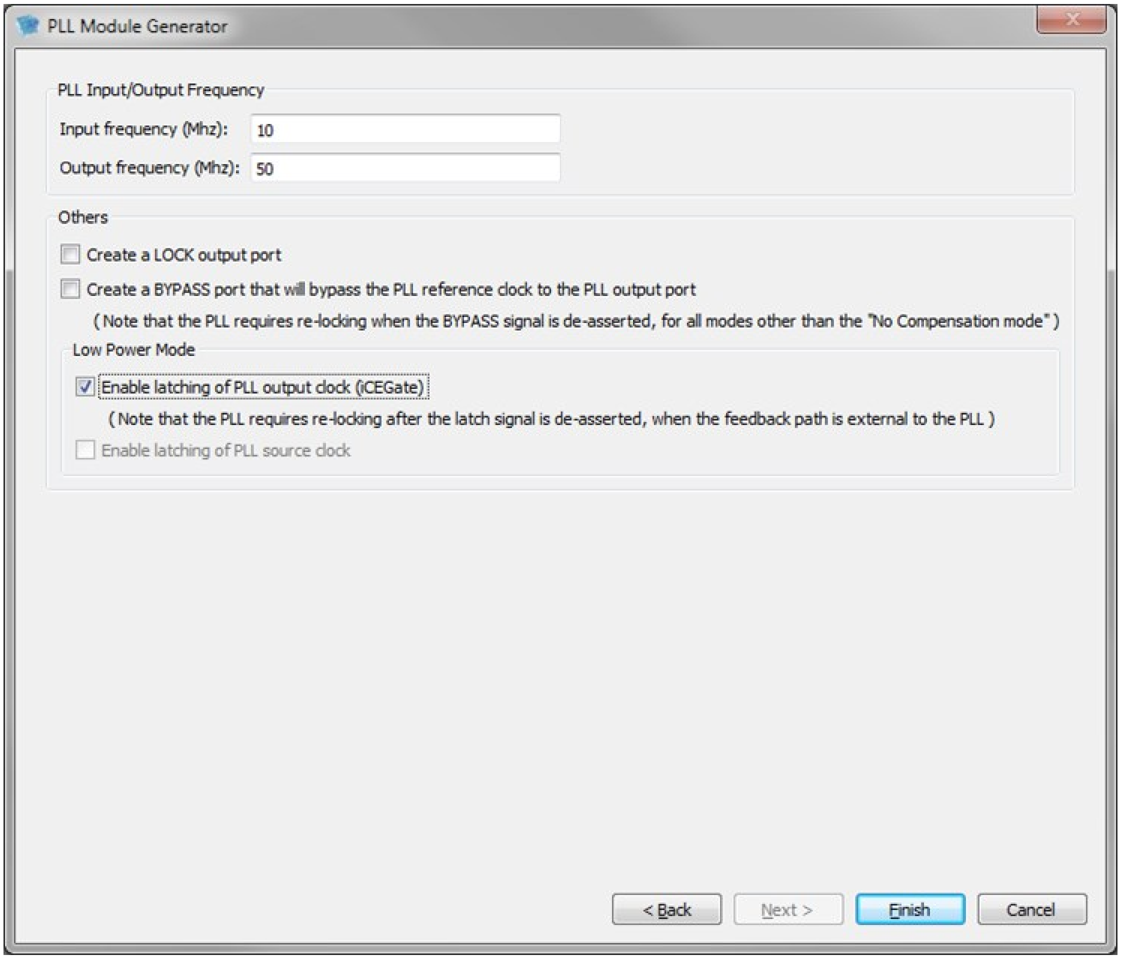


Figure 4.12. Settings Window 3

After selecting the desired values, the final window the PLL Module Generator opens, as shown in Figure 4.13. This window shows all the values of the attributes and parameters that were discussed in the previous sections and in Table 3.1 and Table 3.2. It also shows which PLL Macro type has been selected. The PLL Macro Type used in this example is SB_PLL40_Core.

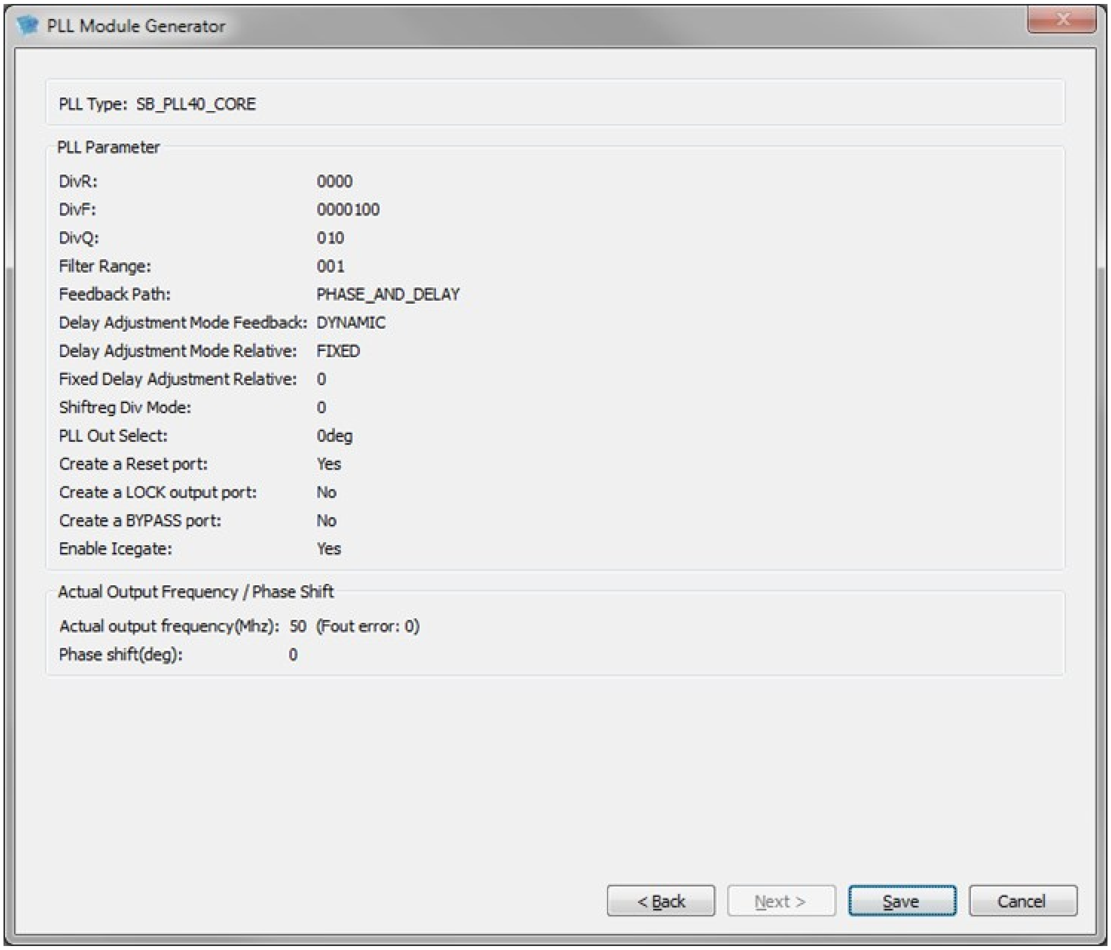


Figure 4.13. PLL Configuration – Final Settings

Table 4.2. PLL Configuration Tool User Parameters

User Parameter	Description	Range	Description
PLL Type			
Select the number of global networks to be driven by the PLL outputs.	Setting the value to *1* generates a PLL which drives a single global clock network, as well as regular routing. Setting the value to *2* generates a PLL which drives two global clock networks as well as two regular routing resources.	1	—
		2	—
How is the PLL Source Clock driven?	—	General Purpose I/O Pad or Core Logic	In this scenario, the PLL input (source clock) is driven by a signal from the FPGA fabric. This signal can either be generated on the FPGA core, or it can be an external signal that was brought onto the FPGA using a General Purpose I/O pad.
	—	Clock Pad	The PLL input clock (source) is driven by a dedicated clock pad located in I/O Bank 2 (bottom bank) or I/O Bank 0 (top bank). If the number of global networks is two, the source clock of the PLL can be used as is (that is. without any frequency, delay compensation or phase adjustments). It is recommended that if the source clock is required on-chip, this option should not be selected.

Table 4.2. PLL Configuration Tool User Parameters *(continued)*

User Parameter	Description	Range	Description
PLL Operation Modes			
How is the PLL output generated?	The PLL can be configured to operate in one of multiple modes. An Operation Mode determines the feedback path of the PLL and enables phase alignment of the generated clock with regard to the source clock.	Using a feedback path internal to the PLL	This option is related to the phase delay introduced in the feedback path. The options are: No Compensation mode – There is no phase delay in the feedback path. Delay compensation using only the Fine Delay Adjustment (FDA) Block – The feedback path traverses through the FDA block, as explained in the Fine Delay Adjustment (FDA) section. Delay compensation using the phase shifter and the Fine Delay Adjustment (FDA) Block – For single-port PLL types, the Phase Shifter provides two outputs corresponding to a phase shift of 0° and 90°. For two-port PLL types, the Phase Shifter has two modes: Divide-by-4 mode and Divide-by-7 mode. In Divide-by-4 mode, the output of the B port can be shifted either 0° or 90° with regard to A port outputs. In Divide-by-7 mode, the B port output frequency can be set to have a frequency ratio of 3.5:1 or 7:1 with regard to the port A output frequency.
		Using a feedback path external to the PLL	The feedback path traverses through FPGA routing (external to the PLL) followed by the FDA block. In effect, two delay controls are available – the external path for coarse adjustment and the FDA block for fine delay adjustment.
Fine Delay Adjustment Settings			
Do you want to dynamically control the delay of the Fine Delay Adjustment block?	Enabled only when Compensation mode or external Feedback mode is selected. The delay contributed by the FDA block can be fixed or controlled dynamically during FPGA operation. If fixed, it is necessary to provide a number (n) in the range of 0-15 to specify the delay contributed to the feedback path. For further details, see Fine Delay Adjustment (FDA).	Yes	—
		No	Enter a value in the range 0–15.
Phase Shift Specification			
Specify the phase shift for the PLL output	Enabled only when delay compensation using the phase shifter is selected. Gives a phase shift of 0° and 90° to the output clock.	0°	—
		90°	—
Target Application*			
LVDS Display Panel	Two different frequencies can be observed on different ports (A and B).	3.5:1	The frequency of port B is 3.5x of Port A.
		7:1	The frequency of Port B is 7x of Port A.
DDR Application	The signal on Port B can be phase shifted by 90° with respect to signal A.	0°	—
		90°	—

Table 4.2. PLL Configuration Tool User Parameters *(continued)*

User Parameter	Description	Range	Description
Additional Delay Settings			
Do you wish to specify additional delay on the PLL outputs?	In addition to Fine Delay Adjustment in the feedback path, you can specify additional delay on the PLL output ports.	Yes	The delay contributed by the delay block can be fixed or controlled dynamically during FPGA operation. If fixed, it is necessary to provide a number (n) in the range 0–15 to specify the delay contributed to the feedback path. The delay for a setting *n* is calculated as follows: FDA delay = (n+1)*0.15 ps, range of n = 0 to 15. **Note:** This additional delay is applied on the output of single-port PLL and port A of two-port PLL Types.
		No	
PLL Input/output Frequency			
Input Frequency (MHz)	Specify input frequency. Refer to the iCE40 Family Data Sheet for the input range.	—	—
Output Frequency (MHz)	Specify desired output frequency. Refer the iCE40 Family Data Sheet for the output frequency range.	—	—
Others			
Create a LOCK output port	A lock signal is provided to indicate that the PLL has locked on to the incoming signal. Lock asserts High to indicate that the PLL has achieved frequency lock with a good phase lock.	—	—
Create a BYPASS port that bypasses the PLL reference clock to the PLL output port	A BYPASS signal is provided which both powers-down the PLL core and bypasses it such that the PLL output tracks the input reference frequency.	—	—
Low Power Mode	A control is provided to dynamically put the PLL into a lower power mode through the iCEGate feature. The iCEGate feature latches the PLL output signal and prevents unnecessary toggling.	Enable latching of PLL clock (iCEGate)	Dynamically controls power by enabling the signal LATCHINPUTVALUE. Refer to the Low Power Mode section.
		Enable latching of PLL source clock	Default setting

***Note:** Enabled when the Number of Global Networks to be Driven by the PLL Outputs option is set to 2.

4.2.1. PLL Module Generator Output

The PLL module generator generates two HDL files:

- <module_name>_inst.v
- <module_name>.v

The <module_name>_inst.v is the instantiation template to be used in the custom top level design. The <module_name>.v contains the PLL software macro with the required attributes and signal values, calculated based on the inputs to the user interface.

4.2.2. iCEcube2 Design Software Report File

The placer.log file (Final Design Statistics section) shows the use of PLLs and GBUFs (global buffers) along with other design elements of the iCE40 device. Note that when GBUF is instantiated in the RTL to connect to a PIO, an extra slice is utilized for connection.

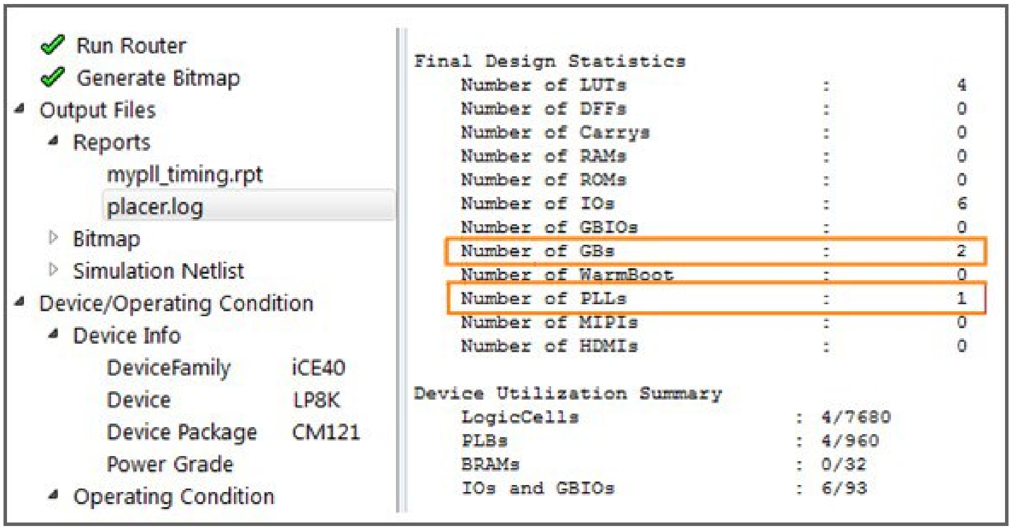


Figure 4.14. Report File Showing the Use of PLLs and Global Buffers

5. Hardware Design Considerations

5.1. PLL Placement Rules

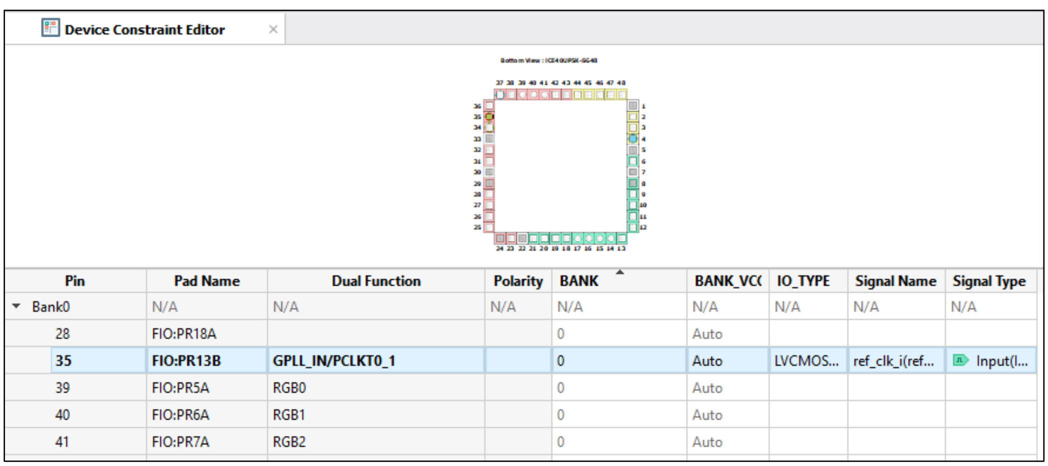
There are minor differences in how iCEcube2 and Lattice Radiant software label the I/O site in iCE40 devices. The hardware limitations below should be considered by the designer to determine which pin qualifies as a PLL input and if it incur a limitation when a PLL is utilized in the design. Figure 5.1 shows an iCE40 UltraPlus device viewed in the Device Constraint Editor of the Lattice Radiant software. Figure 5.2 and Figure 5.3 shows the same device viewed in the Floor Planner of the iCEcube2 software.

5.1.1. Lattice Radiant Software

If the PLL requires an external reference clock source driven through the Globar Buffer Input(GBIN), only a GPLL_IN pad can be used and it becomes no longer available as an input pad for other purposes. As an example shown in Figure 5.1, Pin 35 (Pad name PR13B) can only be used exclusively as a PLL clock input for an external oscillator. However, if the PLL uses an internal oscillator or does not use a GBIN to drive the PLL reference clock input, Pin 35 can still be used but only as an output.

5.1.2. iCEcube2 Software

- If any instance of PLL is placed in the location of the I/O cell, then, an instance of SB_GB_IO cannot be placed in that particular I/O cell.
- If an instance of ice40_PLL_CORE or ice40_PLL_2F_CORE is placed, an instance of SB_IO in *output-only* mode can be placed in the associated I/O cell location.
- If an instance of ice40_PLL_PAD, ice40_PLL_2F_PAD, ice40_PLL_2_PAD is placed, the associated I/O cell cannot be used by any SB_IO or SB_GB_IO.
- If an instance of ice40_PLL_2F_CORE, ice40_PLL_2F_PAD, ice40_PLL_2_PAD is placed, an instance of SB_IO in *output-only* mode can be placed in the right neighboring I/O cell.



Pin	Pad Name	Dual Function	Polarity	BANK	BANK_VC(	IO_TYPE	Signal Name	Signal Type
Bank0	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
28	FIO:PR18A			0	Auto			
35	FIO:PR13B	GPLL_IN/PCLKT0_1		0	Auto	LVCMOS...	ref_clk_i(ref...	Input(I...
39	FIO:PR5A	RGB0		0	Auto			
40	FIO:PR6A	RGB1		0	Auto			
41	FIO:PR7A	RGB2		0	Auto			

Figure 5.1. Device Constraint Editor of Lattice Radiant Software

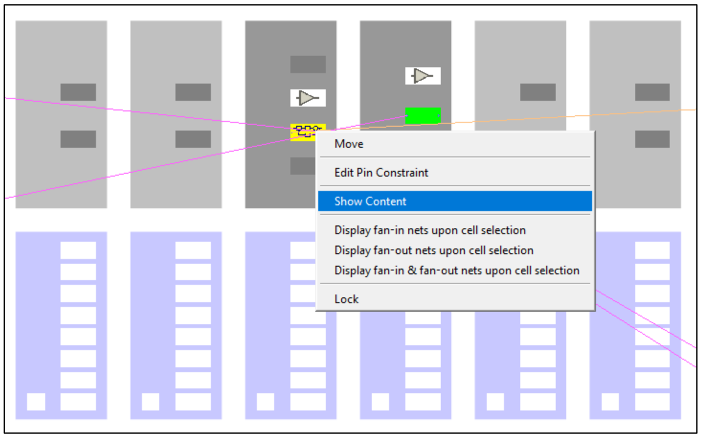


Figure 5.2. Floor Planner View showing the specific I/O Cell that Contains the PLL

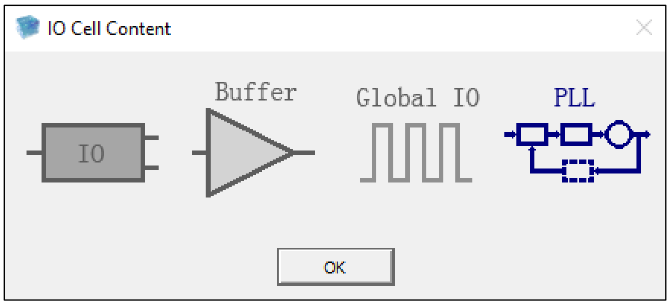


Figure 5.3. I/O Cell Contents

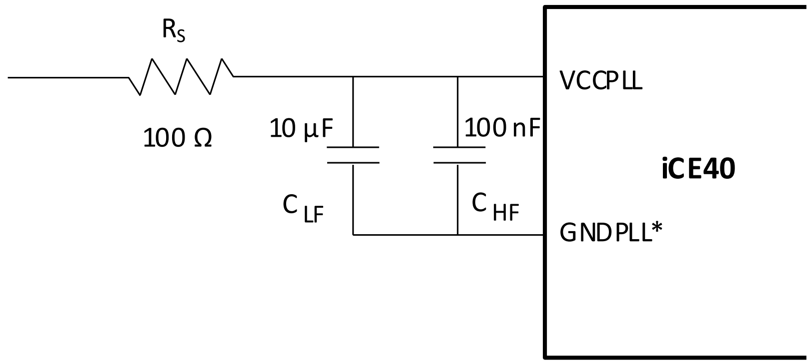
5.2. Analog Power Supply Filter for PLL

The iCE40 sysCLOCK PLL contains some analog blocks. On some devices, the PLL requires a separate power and ground that is quiet and stable, to reduce the output clock jitter of the PLL. On some devices with low pin count, the PLL is not available.

On devices with external power and ground for the PLL, an R-C filter as shown in Figure 5.4 is used as a power supply filter on the PLL power and ground pins. The series resistor (RS) limits the voltage drop across the filter. A high frequency non-electrolytic capacitor (CHF) is placed in parallel with a lower frequency electrolytic capacitor (CLF). CHF is used to attenuate high frequency components while CLF is used for low frequency cut-off.

Board layout around the high frequency capacitor and the path to the pads is critical. The PLL power (VCCPLL) path must be a single wire from the FPGA pin to the high frequency capacitor (CHF), then to the low frequency capacitor (CLF), through the series resistor (RS) and then to board power VCC. The distance from the FPGA pin to the high frequency capacitor should be as short as possible. Similarly, the PLL Ground (GNDPLL) path should be from the FPGA pin to the high frequency capacitor (CHF) and then to the low frequency capacitor (CLF), with the distance from the FPGA pin to the CHF being as short as possible.

The sysCLOCK PLL has the DC ground connection made on the FPGA, so the external PLL ground connection (GNDPLL) must NOT be connected to the board's ground except when a particular iCE40 device does not have a dedicated GNDPLL ball. Figure 5.4 also includes sample values for the components that make up the PLL power supply filter.



***Note:** GND PLL should not be connected to the board's ground except when a particular iCE40 device does not have a dedicated GND PLL ball. This filter requirement should be applied even if the PLL is not utilized in the design.

Figure 5.4. Power Supply Filter for VCCPLL and GNDPLL

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Revision 1.3, July 2021

Section	Change Summary
Hardware Design Considerations	• Updated Analog Power Supply Filter for PLL. • Updated the note in Figure 5.4.

Revision 1.2, August 2020

Section	Change Summary
All	• Changed document title to iCE40 sysCLOCK PLL Design and Usage Guide. • Merged contents with iCE40 sysCLOCK PLL Design and Usage Guide (TN1251).
Disclaimers	Added this section.

Revision 1.1, March 2019

Section	Change Summary
Module Generation	Removed error in step 9 of the PLL module generation procedure.
—	Minor adjustments in style and formatting.

Revision 1.0, February 2018

Section	Change Summary
—	Initial release.