



## **CrossLink VIP Input Bridge Board**

## **Evaluation Board User Guide**

FPGA-EB-02002 Version 1.4

October 2018

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## Acronyms in This Document

A list of acronyms used in this document.

| Acronym          | Definition                              |
|------------------|-----------------------------------------|
| CMOS             | Complementary Metal-Oxide Semiconductor |
| CSI-2            | Camera Serial Interface                 |
| DDR              | Double Data Rate                        |
| DSI              | Display Serial Interface                |
| FTDI             | Future Technology Devices International |
| GPIO             | General Purpose Input/Output            |
| I <sup>2</sup> C | Inter-Integrated Circuit                |
| LDO              | Low Dropout                             |
| LVDS             | Low-Voltage Differential Signaling      |
| MIPI             | Mobile Industry Processor Interface     |
| MSPI             | Master SPI                              |
| SMA              | SubMiniature version A                  |
| SPI              | Serial Peripheral Interface             |
| SSPI             | Slave SPI                               |
| VIP              | Video Interface Platform                |
| VTT              | Tracking Termination Voltage            |

# 1. Introduction

This document describes the Lattice Semiconductor CrossLink™ Video Interface Platform (VIP) Input Bridge Board that supports bridging of Dual MIPI® CSI-2 to parallel interfaces. The board's key component is the Lattice CrossLink FPGA, which receives input from the dual on-board Sony IMX214 cameras, and bridges CSI-2 to parallel interfaces.

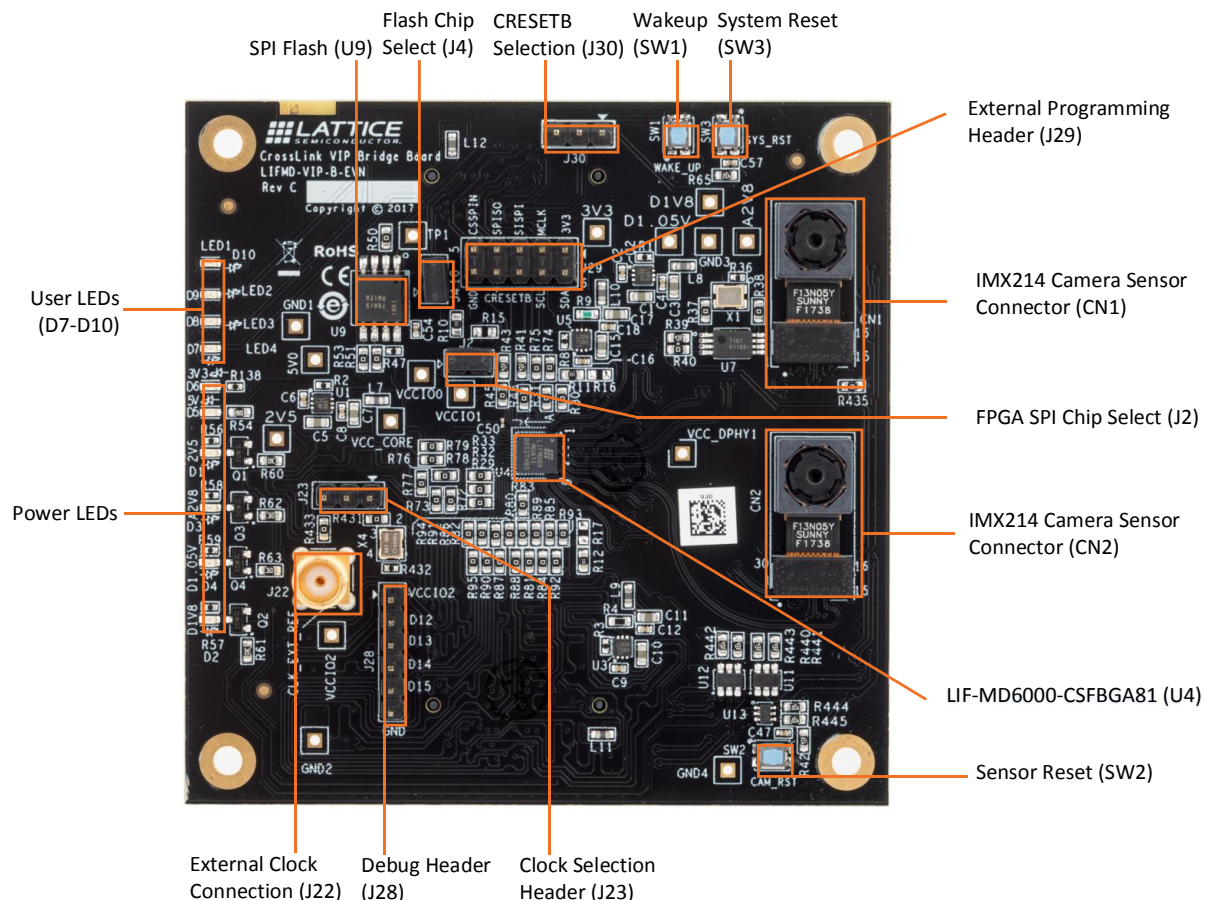
This board is designed to work with the Lattice VIP board interconnect system. Typically, this board will be connected to the ECP5 VIP Processor Board, which can be programmed for a wide range of video processing applications.

The content of this user guide includes descriptions of on-board jumper settings, programming circuit, a complete set of schematics, and bill of materials for CrossLink VIP input bridge board.

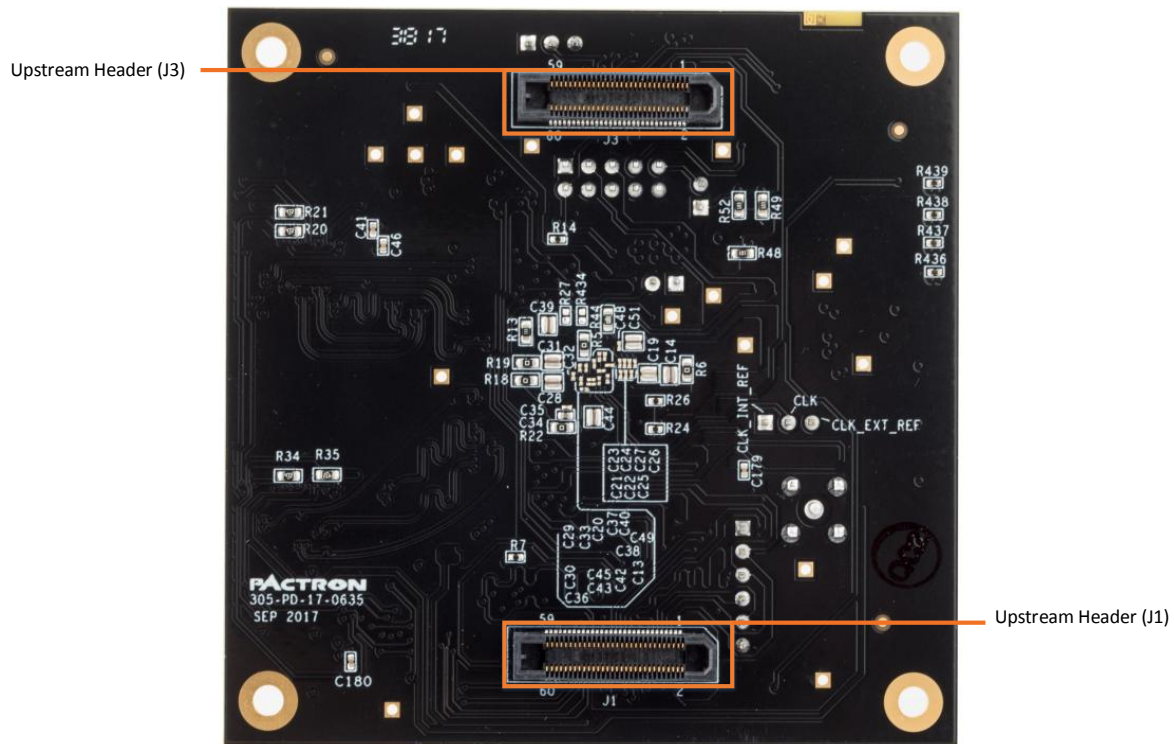
Key features of the Crosslink VIP input bridge board include:

- CrossLink FPGA
  - Dual 4-lane MIPI CSI-2 receiver interface
  - SPI flash configuration
  - 24-bit parallel interface
  - General Purpose Input/Output
- Programming Circuit
  - From external board through board to board connector
  - SPI external programmer using header
- Dual camera interface
  - Dual 4-lane MIPI CSI-2 transmitter interface

Figure 1.1 and Figure 1.2 show the top and bottom views of the CrossLink VIP Input Bridge Board and its key components. This document primarily describes Revision C of the Crosslink VIP Input Bridge Board. Refer to the Appendix for a description of earlier revisions' significant differences.



**Figure 1.1. Top View of CrossLink VIP Input Bridge Board**



**Figure 1.2. Bottom View of CrossLink VIP Input Bridge Board**

To view Revision B of the CrossLink VIP Input Bridge Board, see [Appendix C. CrossLink VIP Input Bridge Board Revision B Camera Orientation](#).

## 1.1. Further Information

The following references provide detailed information on the CrossLink VIP Input Bridge Board and the CrossLink FPGA device:

- [Appendix A. CrossLink VIP Input Board Schematics](#)
- [Appendix B. CrossLink VIP Input Bridge Board Bill of Materials](#)
- [www.latticesemi.com/boards](http://www.latticesemi.com/boards) for more information on boards and kits available for the VIP (Video Interface Platform) system
- [CrossLink Family Data Sheet \(FPGA-DS-02007\)](#) for details on the CrossLink FPGA

## 2. Headers and Test Connections

Table 2.1 lists the headers and test connectors as shown in Figure 1.1.

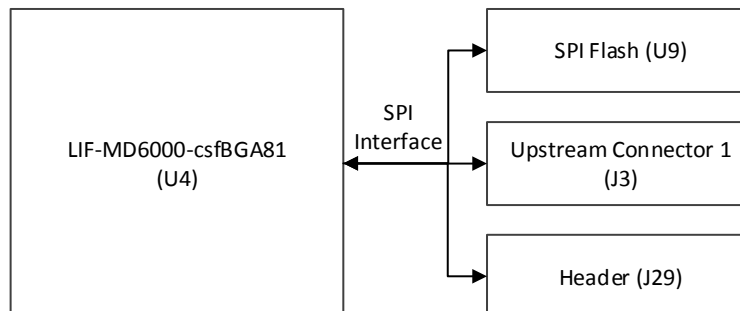
**Table 2.1. Headers and Test Connectors**

| Part | Description                  | Setting                                        |
|------|------------------------------|------------------------------------------------|
| J2   | LIFMD6000 chip select        | Short                                          |
| J4   | SPI Flash chip select        | Short                                          |
| J23  | Clock input source selection | 1–2 (Internal Oscillator.), 2–3 (External SMA) |
| J28  | Debug Header                 | —                                              |
| J29  | External programming header  | —                                              |
| J30  | LIFMD6000 CRESET selection   | 1–2 (External RESET), 2–3 (GND), Open (Normal) |

### 3. Programming Circuit

CrossLink can be programmed by an external programmer connected to Header J29 or through the SPI interface on the upstream connector (J3) by using Lattice Diamond® programmer software.

Figure 3.1 shows the programming block of CrossLink VIP input bridge board.



**Figure 3.1. Programming Block**

The SPI interface is used to program both CrossLink and SPI Flash Memory (see Table 3.1). When programming using an external programmer in SSPI mode, jumpers J2 and J4 on CrossLink VIP Input Bridge Board enable the programming of CrossLink and SPI Flash Memory respectively. For MSPI mode of CrossLink, both jumper J2 and J4 must be shorted for the configuration.

**Table 3.1. SPI Flash Memory**

| Board Revision | Family | Device                |
|----------------|--------|-----------------------|
| B              | Micron | M25PX16               |
| C              | Micron | M25PX16 or MT25QL128A |

## 4. CrossLink Interface Support

The CrossLink VIP input bridge board supports various onboard interfaces and external interfaces through board-to-board connectors. The sections below describe key onboard interfaces supported on CrossLink VIP Input Bridge Board.

### 4.1. Camera Sensor Interface

Figure 4.1 shows the block diagram of dual camera sensor interface. The Sony IMX214 image sensor is used as input source on the camera sensor connectors. The data path interface between the camera sensor module and Crosslink is CSI-2. The cameras are configured using I<sup>2</sup>C interface by the external board through upstream connectors.

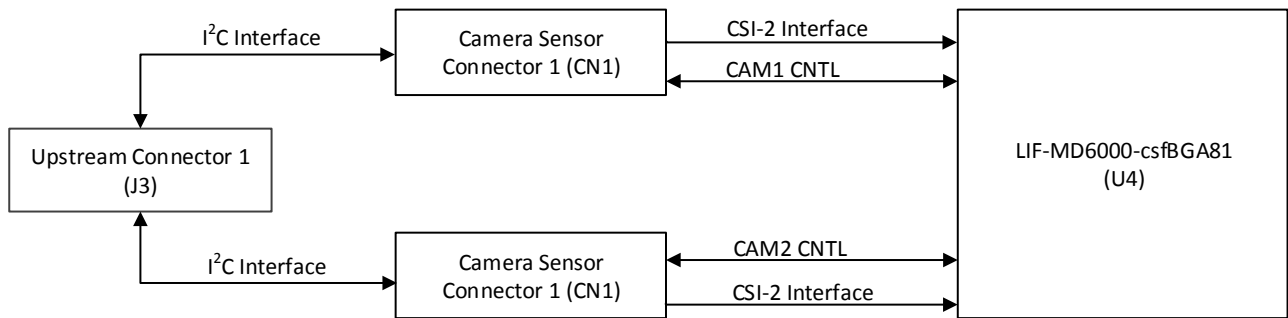


Figure 4.1. Camera Sensor Interface

### 4.2. Upstream Connector Interface

Figure 4.2 shows the block diagram of the upstream connector. The upstream connector acts as board-to-board connector and interfaces CrossLink VIP Input Bridge Board to the ECP5 VIP processor board for bridging applications. The interface between the CrossLink device and the upstream connector is 24-bit parallel data and control interface.

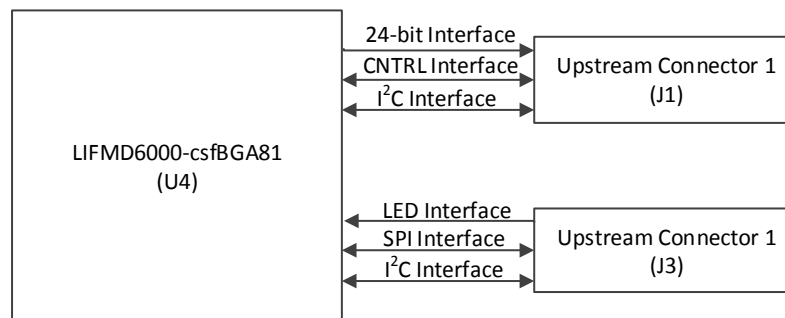


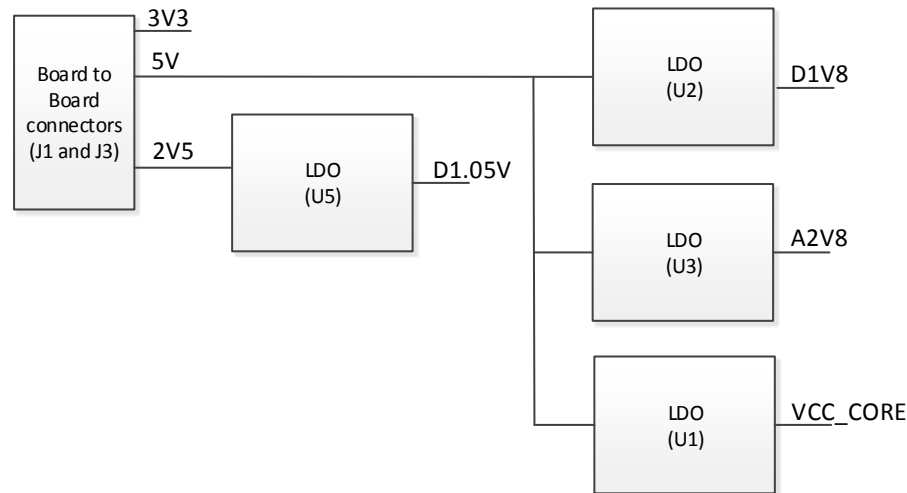
Figure 4.2. Upstream Connector Interface



## 5. Power Supply

The power supply to CrossLink VIP Input Bridge Board is provided from board-to-board connectors (J1 and J3).

Figure 5.1 shows the power supply block of CrossLink VIP Input Bridge Board. The external board (ECP5 VIP processor board) must be connected to power source for the onboard regulators for normal operation and successful programming. The board-to-board connector provides 5 V, 3.3 V, 2.5 V power source to the board and the onboard regulators to generate remaining power rails. Each I/O and core voltage rail on the board is accessible by a test point on the board.



**Figure 5.1. Power Supply Block**

Table 5.1 lists the board voltage rails, including the rail source voltage, test point number, and voltage on net.

**Table 5.1. Device Power Rail Summary**

| Voltage Rail | Source Rail | Test Points | Voltage on Net (V) | Status LED | LED Color |
|--------------|-------------|-------------|--------------------|------------|-----------|
| 5V0          | —           | —           | 5                  | D5         | Green     |
| 3V3          | 3V3_EXT     | 3V3         | 3.3                | D6         | Green     |
| A2V8         | 5V          | A2V8        | 2.8                | D3         | Green     |
| 2V5          | 5V          | 2V5         | 2.5                | D1         | Green     |
| D1V8         | 2V5         | D1V8        | 1.8                | D2         | Green     |
| D1.05V       | 2V5         | D1.05V      | 1.05               | D4         | Green     |
| VCC_CORE     | 5V          | VCC_CORE    | 1.2                | —          | —         |
| VCC_DPHY     | VCC_CORE    | VCC_DPHY    | 1.2                | —          | —         |

## 6. CrossLink I/O Ball Mapping to Connectors

Table 6.1. Upstream Connector Mapping

| J1                      |          |             | J3                      |              |             |
|-------------------------|----------|-------------|-------------------------|--------------|-------------|
| Pin Number on Connector | Net Name | Ball Number | Pin Number on Connector | Net Name     | Ball Number |
| 1                       | 3V3_EXT  | —           | 1                       | 3V3_EXT, L12 | —           |
| 2                       | 3V3_EXT  | —           | 2                       | 5V           | —           |
| 3                       | 3V3_EXT  | —           | 3                       | 3V3_EXT, L12 | —           |
| 4                       | 3V3_EXT  | —           | 4                       | 5V           | —           |
| 5                       | D12      | D9          | 5                       | GND          | —           |
| 6                       | D0       | F9          | 6                       | 5V           | —           |
| 7                       | D13      | D8          | 7                       | GPIO3        | J6          |
| 8                       | D1       | F8          | 8                       | GND          | —           |
| 9                       | D14      | J7          | 9                       | —            | —           |
| 10                      | D2       | G9          | 10                      | LED4         | —           |
| 11                      | D15      | H7          | 11                      | GND          | —           |
| 12                      | D3       | G8          | 12                      | —            | —           |
| 13                      | D16      | J5          | 13                      | LED2         | —           |
| 14                      | D4       | E9          | 14                      | GND          | —           |
| 15                      | D17      | H5          | 15                      | —            | —           |
| 16                      | D5       | E8          | 16                      | —            | —           |
| 17                      | GND      | —           | 17                      | GND          | —           |
| 18                      | GND      | —           | 18                      | —            | —           |
| 19                      | GND      | —           | 19                      | LED3         | —           |
| 20                      | GND      | —           | 20                      | GND          | —           |
| 21                      | D18      | E1          | 21                      | —            | —           |
| 22                      | GND      | —           | 22                      | 2V5_EXT      | —           |
| 23                      | D19      | E2          | 23                      | GND          | —           |
| 24                      | D6       | H9          | 24                      | 2V5_EXT      | —           |
| 25                      | D20      | J4          | 25                      | —            | —           |
| 26                      | D7       | H8          | 26                      | —            | —           |
| 27                      | D21      | H4          | 27                      | MCLK         | H1          |
| 28                      | D8       | F7          | 28                      | RESET        | —           |
| 29                      | D22      | J3          | 29                      | SISPI        | F1          |
| 30                      | D9       | E7          | 30                      | —            | —           |
| 31                      | D23      | H3          | 31                      | SPISO        | J1          |
| 32                      | D10      | J9          | 32                      | —            | —           |
| 33                      | GND      | —           | 33                      | CSSPIN       | G1          |
| 34                      | D11      | J8          | 34                      | GND          | —           |
| 35                      | GND      | —           | 35                      | CDONE        | H2          |
| 36                      | GND      | —           | 36                      | —            | —           |
| 37                      | —        | —           | 37                      | CRESETB      | G2          |
| 38                      | GND      | —           | 38                      | —            | —           |
| 39                      | GPIO2    | G6          | 39                      | —            | —           |
| 40                      | GND      | —           | 40                      | GND          | —           |
| 41                      | LED1     | —           | 41                      | SCL          | F2          |
| 42                      | SDA2     | —           | 42                      | —            | —           |

**Table 6.1. Upstream Connector Mapping**

| J1                      |              |             | J3                      |          |             |
|-------------------------|--------------|-------------|-------------------------|----------|-------------|
| Pin Number on Connector | Net Name     | Ball Number | Pin Number on Connector | Net Name | Ball Number |
| 43                      | GPIO4        | H6          | 43                      | SDA      | J2          |
| 44                      | SCL2         | —           | 44                      | —        | —           |
| 45                      | GPIO5        | D1          | 45                      | —        | —           |
| 46                      | CAM_RESET    | —           | 46                      | GND      | —           |
| 47                      | GPIO6        | D2          | 47                      | —        | —           |
| 48                      | SDA1         | —           | 48                      | —        | —           |
| 49                      | —            | —           | 49                      | —        | —           |
| 50                      | SCL1         | —           | 50                      | —        | —           |
| 51                      | —            | —           | 51                      | —        | —           |
| 52                      | —            | —           | 52                      | GND      | —           |
| 53                      | GND          | —           | 53                      | —        | —           |
| 54                      | GND          | —           | 54                      | —        | —           |
| 55                      | GND          | —           | 55                      | GND      | —           |
| 56                      | GND          | —           | 56                      | —        | —           |
| 57                      | 2V5_EXT, L11 | —           | 57                      | GND      | —           |
| 58                      | 2V5_EXT      | —           | 58                      | GND      | —           |
| 59                      | 2V5_EXT, L11 | —           | 59                      | GND      | —           |
| 60                      | 2V5_EXT      | —           | 60                      | —        | —           |

**Table 6.2. Camera Sensor Connector Pin Mapping**

| CN1                     |           |             | CN2                     |           |             |
|-------------------------|-----------|-------------|-------------------------|-----------|-------------|
| Pin Number on Connector | Net Name  | Ball Number | Pin number on Connector | Net Name  | Ball Number |
| 1                       | —         | —           | 1                       | —         | —           |
| 2                       | SLVS_CN_1 | A2          | 2                       | SLVS_CN_2 | A9          |
| 3                       | SLVS_CP_1 | A1          | 3                       | SLVS_CP_2 | A8          |
| 4                       | GND       | —           | 4                       | GND       | —           |
| 5                       | SLVS_3N_1 | B4          | 5                       | SLVS_3N_2 | C9          |
| 6                       | SLVS_3P_1 | A4          | 6                       | SLVS_3P_2 | C8          |
| 7                       | GND       | —           | 7                       | GND       | —           |
| 8                       | SLVS_1N_1 | B3          | 8                       | SLVS_1N_2 | B9          |
| 9                       | SLVS_1P_1 | A3          | 9                       | SLVS_1P_2 | B8          |
| 10                      | GND       | —           | 10                      | GND       | —           |
| 11                      | SLVS_ON_1 | B2          | 11                      | SLVS_ON_2 | A7          |
| 12                      | SLVS_OP_1 | B1          | 12                      | SLVS_OP_2 | B7          |
| 13                      | GND       | —           | 13                      | GND       | —           |
| 14                      | SLVS_2N_1 | C2          | 14                      | SLVS_2N_2 | A6          |
| 15                      | SLVS_2P_1 | C1          | 15                      | SLVS_2P_2 | B6          |
| 16                      | GND       | —           | 16                      | GND       | —           |
| 17                      | GND       | —           | 17                      | GND       | —           |
| 18                      | A2V8      | —           | 18                      | A2V8      | —           |
| 19                      | —         | —           | 19                      | —         | —           |
| 20                      | CAM_CLK1  | —           | 20                      | CAM_CLK2  | —           |
| 21                      | —         | —           | 21                      | —         | —           |
| 22                      | CAM_SDA1  | —           | 22                      | CAM_SDA2  | —           |
| 23                      | CAM_SCL1  | —           | 23                      | CAM_SCL2  | —           |
| 24                      | CAM_RST1  | —           | 24                      | CAM_RST2  | —           |
| 25                      | D1.05V    | —           | 25                      | D1.05V    | —           |
| 26                      | D1V8      | —           | 26                      | D1V8      | —           |
| 27                      | GND       | —           | 27                      | GND       | —           |
| 28                      | GND       | —           | 28                      | GND       | —           |
| 29                      | A2V8      | —           | 29                      | A2V8      | —           |
| 30                      | GND       | —           | 30                      | GND       | —           |

## 7. Status Indicators

The LED status indicators on the board show the application status. [Table 7.1](#) lists the status LED I/O map.

**Table 7.1. Status LED I/O Map**

| Net Name | LED | Connector/Pin | Color |
|----------|-----|---------------|-------|
| LED1     | D10 | J1/41         | Green |
| LED2     | D9  | J3/13         | Green |
| LED3     | D8  | J3/19         | Green |
| LED4     | D7  | J3/10         | Green |

## 8. Ordering Information

This board is included as part of a kit, and not available as a separate item. The below part number is for reference only, so it is clear which board is described in this document. Please visit [www.latticesemi.com/boards](http://www.latticesemi.com/boards) for the latest ordering information.

**Table 8.1. Reference Part Number**

| Description                      | Ordering Part Number |
|----------------------------------|----------------------|
| CrossLink VIP Input Bridge Board | LIFMD-VIP-IB-EVN     |

## References

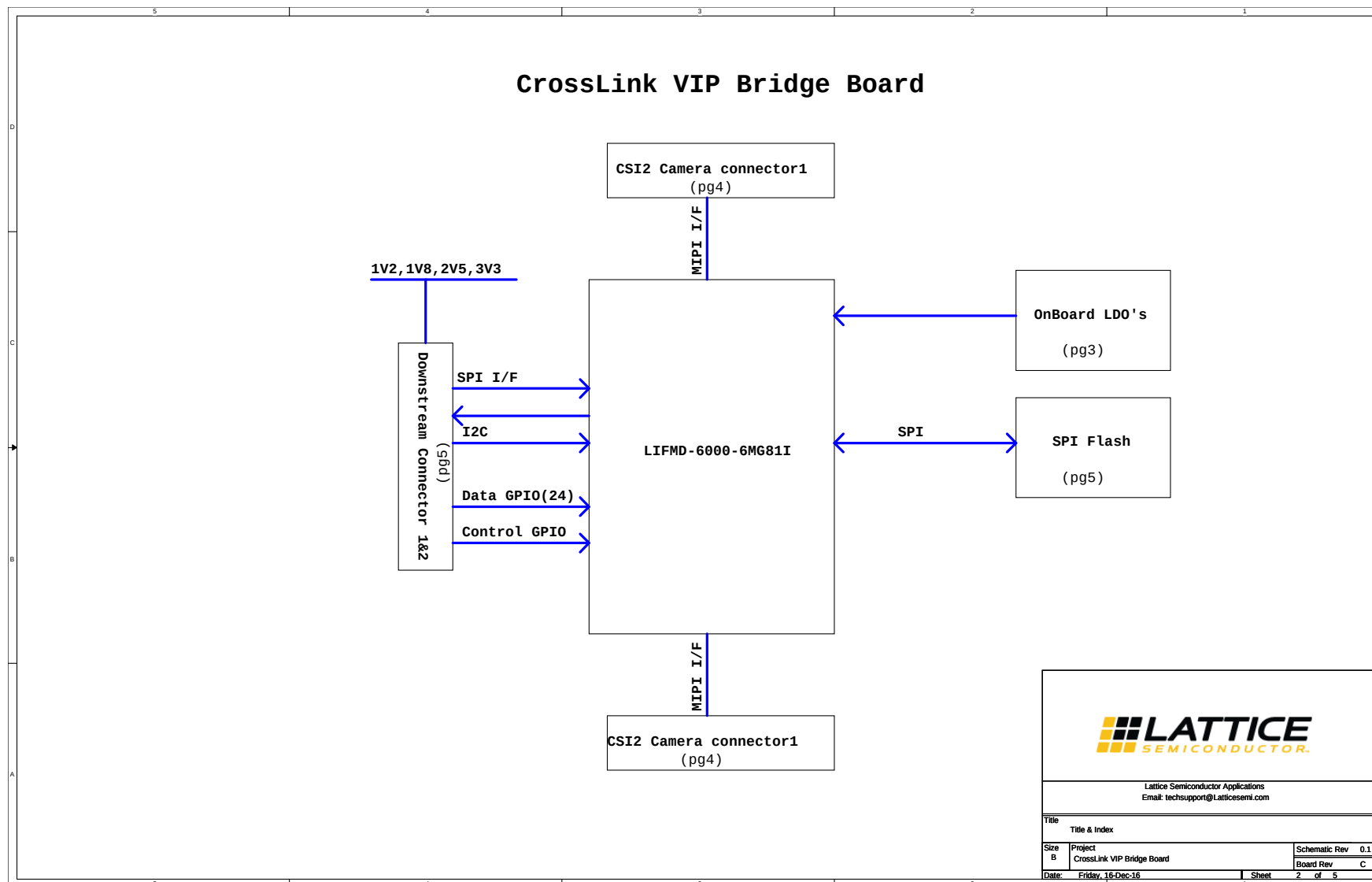
For more information, refer to

- [CrossLink Family Data Sheet \(FPGA-DS-02007\)](#).
- [Lattice Embedded Vision Development Kit User Guide \(FPGA-UG-02015\)](#)
- [ECP5 VIP Processing Board \(FPGA-EB-02001\)](#)
- [HDMI VIP Output Bridge Board \(FPGA-EB-02003\)](#)

## Technical Support Assistance

Submit a technical support case through [www.latticesemi.com/techsupport](http://www.latticesemi.com/techsupport).

## Appendix A. CrossLink VIP Input Board Schematics



**Figure A.1. Block Diagram**

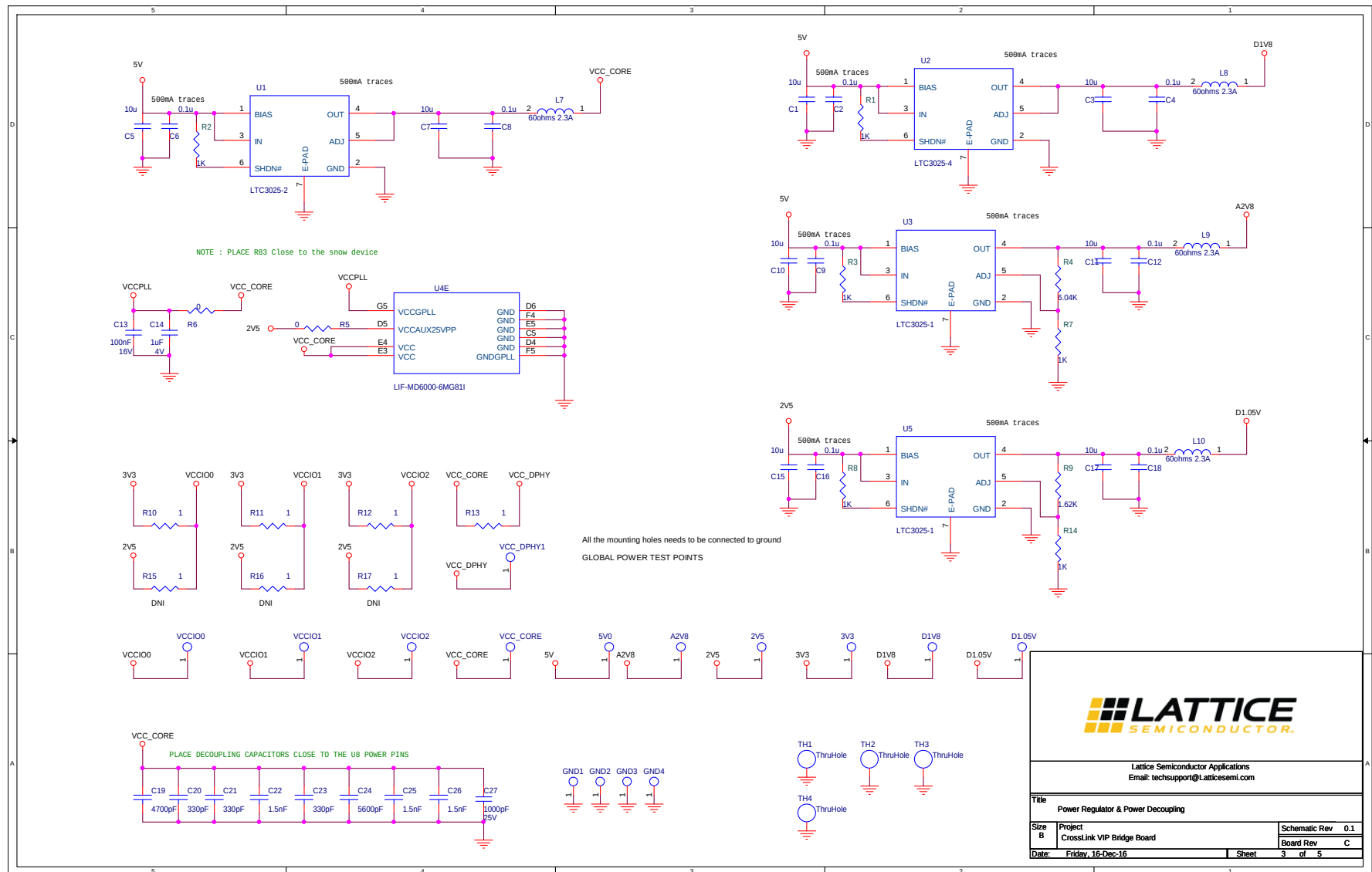


Figure A.2. Power Regulator and Power Decoupling







## Appendix B. CrossLink VIP Input Bridge Board Bill of Materials

| Item | Reference                                                                                                   | Qty | Part                 | PCB Footprint    | Comments                 | Part Number          | Manufacturer            | Description                                                     |
|------|-------------------------------------------------------------------------------------------------------------|-----|----------------------|------------------|--------------------------|----------------------|-------------------------|-----------------------------------------------------------------|
| 1    | VCC_DPHY1, VCCIO1, GND1, VCCIO2, GND2, GND3, GND4, D1V8, 2V5, A2V8, 3V3, 5V0, D1.05V, VCC_CORE, VCCIO0, TP1 | 16  | TP_S_40_63           | tp_s_40_63       | DNL                      | —                    | —                       | Square test point, 40 mil inner diameter, 63 mil outer diameter |
| 2    | CN1, CN2                                                                                                    | 2   | 24-5804-030-030-829+ | 245804030 030829 | Module info in BAG & TAG | 24-5804-030-030-829+ | Kyocera / Sunny Optical | Sony IMX214 CSI Camera sensor                                   |
| 3    | C1, C3, C5, C7, C10, C11, C15, C17                                                                          | 8   | 10 $\mu$ F           | C0603            | —                        | CL10X106MP8 NRNC     | Samsung                 | CAP CER 10 $\mu$ F 10 V 20% X6S 0603                            |
| 4    | C2, C4, C6, C8, C9, C12, C16, C18                                                                           | 8   | 0.1 $\mu$ F          | C0402            | —                        | CL05A104MP5 NNNC     | Samsung                 | Cap Ceramic 0.1 $\mu$ F 10 V X5R 20% SMD 0402 85C Paper T/R     |
| 5    | C13, C37, C42, C50                                                                                          | 4   | 100 nF               | C0201            | —                        | C0603X5R1C1 04K030BC | TDK                     | CAP CER 0.1 $\mu$ F 16 V X5R 0201                               |
| 6    | C14, C28, C31, C39, C44, C51                                                                                | 6   | 1 $\mu$ F            | C0306            | —                        | LLR185C70G1 05ME05L  | Murata                  | CAP CER 1 $\mu$ F 4 V X7S 0306                                  |
| 7    | C19                                                                                                         | 1   | 4700 pF              | C0306            | —                        | LLL185R71H47 2MA01L  | Murata                  | CAP CER 4700 pF 50 V X7R 0306                                   |
| 8    | C20, C21, C23                                                                                               | 3   | 330 pF               | C0201            | —                        | GRM033R71H 331KA12D  | Murata                  | CAP CER 330 pF 50 V X7R 0201                                    |
| 9    | C22, C25, C26, C38, C43                                                                                     | 5   | 1.5 nF               | C0201            | —                        | GRM033R71A 152KA01D  | Murata                  | CAP CER 1500 pF 10 V X7R 0201                                   |
| 10   | C24                                                                                                         | 1   | 5600 pF              | C0201            | —                        | GRM033R71A 562KA01D  | Murata                  | CAP CER 5600 pF 10 V X7R 0201                                   |
| 11   | C27                                                                                                         | 1   | 1000 pF              | C0201            | —                        | GRM033R61E 102KA01D  | Murata                  | CAP CER 1000 pF 25 V X5R 0201                                   |
| 12   | C29, C32                                                                                                    | 2   | 0.01 $\mu$ F         | C0201            | —                        | GRM033R61C 103KA12D  | Murata                  | CAP CER 10000 pF 16 V X5R 0201                                  |
| 13   | C30, C33, C35, C40, C45, C49                                                                                | 6   | 470 pF               | C0201            | —                        | GRM033R71C 471KA01D  | Murata                  | CAP CER 470 pF 16 V X7R 0201                                    |
| 14   | C34                                                                                                         | 1   | 1 $\mu$ F            | C0402            | —                        | GRM155R61C 105KA12D  | Murata                  | CAP CER 1 $\mu$ F 16 V X5R 0402                                 |
| 15   | C36                                                                                                         | 1   | 0.1 $\mu$ F          | C0201            | —                        | GRM033R61C 104KE84D  | Murata                  | CAP CER 0.1 $\mu$ F 16 V X5R 0201                               |

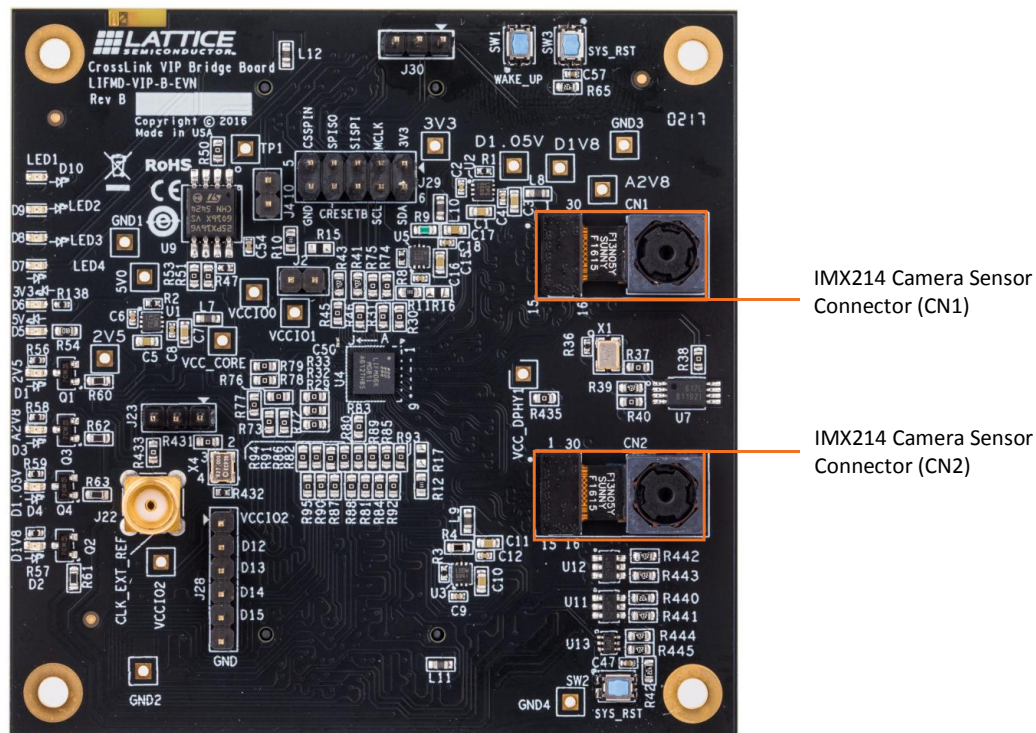
| Item | Reference                               | Qty | Part                   | PCB Footprint          | Comments | Part Number            | Manufacturer      | Description                                                                    |
|------|-----------------------------------------|-----|------------------------|------------------------|----------|------------------------|-------------------|--------------------------------------------------------------------------------|
| 16   | C41, C46, C54, C179, C180               | 5   | 100 nF                 | C0402                  | —        | 885012205018           | Würth             | CAP CER 0.1 µF 10 V X7R 0402                                                   |
| 17   | C47, C57                                | 2   | 0.1 µF                 | C0402                  | —        | 885012205037           | Würth             | CAP CERAMIC 0.1 µF 16 V X7R 0402                                               |
| 18   | C48                                     | 1   | 2200 pF                | C0201                  | —        | GRM033R71E222KA12D     | Murata            | CAP CER 2200 pF 25 V X7R 0201                                                  |
| 19   | D1, D2, D3, D4, D5, D6, D7, D8, D9, D10 | 10  | Green                  | led_0603               | —        | LTST-C190KGKT          | LITE-On INC       | LED SUPER GREEN CLEAR 0603 SMD                                                 |
| 20   | J1, J3                                  | 2   | ERF5-030-070-L-DV-K-TR | ERF5-030-070-L-DV-K-TR | —        | ERF5-030-070-L-DV-K-TR | Samtec Inc        | Conn High Speed Edge Rate Terminal Strip HDR 60 POS 0.5 mm Solder ST SMD T/R - |
| 21   | J2, J4                                  | 2   | CON2                   | CON2                   | —        | 61300211121            | Würth             | 2 Positions Header, Unshrouded Connector 0.100" (2.54 mm) through Hole Gold    |
| 22   | J22                                     | 1   | 73391-0060             | 73391-0060             | —        | 73391-0060             | Molex             | Molex Straight 500 Through Hole SMA Connector, jack, Solder Termination        |
| 23   | J23, J30                                | 2   | CON3                   | CON3                   | —        | 61300311121            | Würth             | 3 Positions Header, Unshrouded Connector 0.100" (2.54 mm) through Hole Gold    |
| 24   | J28                                     | 1   | CON6                   | HDR1X6                 | —        | 61300611121            | Würth             | 6 Positions Header, Unshrouded Connector 0.100" (2.54 mm) through Hole Gold    |
| 25   | J29                                     | 1   | CONN PWR 5x2-H         | 5X2_CONN               | —        | 61301021121            | Würth             | 10 Positions Header, Unshrouded Connector 0.100" (2.54 mm) through Hole Gold   |
| 26   | L7, L8, L9, L10, L11, L12               | 6   | 60 Ω 2.3 A             | FB0603                 | —        | 742792602              | Würth             | EMI Filter Beads, Chips & Arrays 60 Ω Power                                    |
| 27   | Q1, Q2, Q3, Q4                          | 4   | MMBT2222A              | SM_SOT23-3             | —        | MMBT2222A, 215         | NXP Semiconductor | Bipolar Transistors - BJT NPN Gen Pur SS                                       |

| Item | Reference                                                                                                                                                                                                                        | Qty | Part  | PCB Footprint | Comments | Part Number         | Manufacturer              | Description                                                                        |
|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-------|---------------|----------|---------------------|---------------------------|------------------------------------------------------------------------------------|
| 28   | R1, R2, R3, R7, R8, R14, R24, R26, R27, R47, R56, R57, R58, R59, R434                                                                                                                                                            | 15  | 1K    | R0402         | —        | RMCF0402JT1 K00     | Stackpole Electronics Inc | RES 1K $\Omega$ 1/16 W 5% 0402                                                     |
| 29   | R4                                                                                                                                                                                                                               | 1   | 6.04K | R0603         | —        | ERA-3ARB6041V       | Panasonic                 | RES SMD 6.04K $\Omega$ 0.1% 1/10 W 0603                                            |
| 30   | R5, R6, R18, R19, R22, R29, R30, R31, R32, R33, R37, R38, R40, R45, R46, R50, R51, R53, R72, R73, R74, R75, R76, R77, R78, R79, R80, R81, R82, R83, R84, R85, R86, R87, R88, R89, R90, R91, R92, R93, R94, R95, R431, R433, R435 | 45  | 0     | R0603         | —        | RC0603JR-070RL      | Yageo                     | Res 1/10 W 0.0 $\Omega$ 5% 0603                                                    |
| 31   | R9                                                                                                                                                                                                                               | 1   | 1.62K | R0603         | —        | RN731JT1D16 21B25   | KOA Speer                 | Thin Film Resistors 1.62K $\Omega$ , 0603, 0.1%, 2 5 ppm, 63 mW, 50 V              |
| 32   | R10, R11, R12, R13                                                                                                                                                                                                               | 4   | 1     | R0603         | —        | CRCW06031R 00JNEAHP | Vishay/Dale               | RES 1.0 $\Omega$ 0.25 W 5% 0603 SMD                                                |
| 33   | R15, R16, R17                                                                                                                                                                                                                    | 3   | 1     | R0603         | DNL      | CRCW06031R 00JNEAHP | Vishay/Dale               | RES 1.0 $\Omega$ 0.25 W 5% 0603 SMD                                                |
| 34   | R20, R21, R34, R35, R39, R41, R42, R43, R65, R440, R441, R442, R443, R444, R445                                                                                                                                                  | 15  | 4.7k  | R0603         | —        | CRCW06034K 70FKEA   | Vishay                    | Thick Film Resistors - SMD 1/10 W 4.7K $\Omega$ 1%                                 |
| 35   | R36, R432                                                                                                                                                                                                                        | 2   | 100K  | R0402         | —        | RMCF0402JT1 00K     | Stackpole Electronics Inc | RES 100K $\Omega$ 1/16 W 5% 0402                                                   |
| 36   | R44                                                                                                                                                                                                                              | 1   | 30E   | R0603         | —        | RC0603FR-0730RL     | Yageo                     | RES SMD 30 $\Omega$ 1% 1/10 W 0603                                                 |
| 37   | R48, R49, R52                                                                                                                                                                                                                    | 3   | 10K   | R0603         | —        | RMCF0603JT1 0K0     | Stackpole Electronics Inc | Res Thick Film 0603 10K $\Omega$ 5% 1/10 W $\nabla$ 100 ppm/C Molded SMD Paper T/R |
| 38   | R54                                                                                                                                                                                                                              | 1   | 1K    | R0603         | —        | RC0603FR-071KL      | Yageo                     | Res Thick Film 0603 1K $\Omega$ 1% 1/10 W $\nabla$ 100 ppm/C                       |
| 39   | R60, R61, R62, R63                                                                                                                                                                                                               | 4   | 10K   | R0603         | —        | ERJ-3EKF1002V       | Panasonic                 | RES SMD 10K $\Omega$ 1% 1/10 W 0603                                                |
| 40   | R138, R436, R437, R438, R439                                                                                                                                                                                                     | 5   | 330E  | R0402         | —        | CRCW040233 0RFKED   | Vishay / Dale             | Thick Film Resistors - SMD 1/16 W 330 $\Omega$ 1%                                  |

| Item | Reference          | Qty | Part                   | PCB Footprint      | Comments | Part Number            | Manufacturer                          | Description                                                                   |
|------|--------------------|-----|------------------------|--------------------|----------|------------------------|---------------------------------------|-------------------------------------------------------------------------------|
| 41   | SW1                | 1   | WAKE_UP                | 4psmd_switch       | —        | 434153017835           | Würth                                 | SWITCH TACTILE SPST-NO 0.05 A 12 V                                            |
| 42   | SW2, SW3           | 2   | SYS_RST                | 4psmd_switch       | —        | 434153017835           | Würth                                 | SWITCH TACTILE SPST-NO 0.05 A 12 V                                            |
| 43   | TH1, TH2, TH3, TH4 | 4   | ThruHole               | MTG125             | DNL      | —                      | —                                     | —                                                                             |
| 44   | U1                 | 1   | LTC3025-2              | LTC3025-DFN        | —        | LTC3025EDC-2#PBF       | Linear Tech                           | LDO Regulator Pos 1.2 V 0.5 A 6-Pin DFN EP T/R                                |
| 45   | U2                 | 1   | LTC3025-4              | LTC3025-DFN        | —        | LTC3025EDC-4#PBF       | Linear Tech                           | LDO Regulator Pos 1.8 V 0.5 A 6-Pin DFN EP T/R                                |
| 46   | U3                 | 1   | LTC3025-1              | LTC3025-DFN        | —        | LTC3025EDC-1#PBF       | Linear Tech                           | LDO Regulator 0.5 A 6-Pin DFN EP T/R                                          |
| 47   | U4                 | 1   | LIFMD6000-csfBGA81     | LIFMD6000-csfBGA81 | —        | LIFMD6000-csfBGA81     | Lattice Semiconductor                 | Lattice semiconductor 6K CrossLink family FPGA                                |
| 48   | U5                 | 1   | LTC3025-1              | LTC3025-DFN        | —        | LTC3025EDC-1#PBF       | Linear Tech                           | LDO Regulator 0.5 A 6-Pin DFN EP T/R                                          |
| 49   | U7                 | 1   | 5PB1102PGGI            | 5PB1102PGGI        | —        | 5PB1102PGGI            | IDT,-Integrated-Device-Technology-Inc | Clock Fanout Buffer (Distribution) IC 200 MHz 8-TSSOP (0.173", 4.40 mm Width) |
| 50   | U9                 | 1   | M25PX16-VMW6TG         | SOIC8              | Rev B    | M25PX16-VMW6TG         | Micron                                | IC FLASH 16 Mbit 75 MHz 8SO                                                   |
|      |                    |     | MT25QL128A BA1ESE-OSIT |                    | Rev C    | MT25QL128A BA1ESE-OSIT | Micron                                | IC FLASH 128 Mbit 90 MHz 8SO                                                  |
| 51   | U11, U12           | 2   | FDC6301N               | FDC6301N           | —        | FDC6301N               | ON Semiconductor/Fairchild            | Mosfet Array 2 N-Channel (Dual) 25 V 220 mA 700 mW Surface Mount SuperSOT™-6  |
| 52   | U13                | 1   | NC7WZ07P6X             | NC7WZ07P6X         | —        | NC7WZ07P6X             | Fairchild Semiconductor Corporation   | IC BUFF DL UHS O/DRAIN SC70-6                                                 |
| 53   | X1                 | 1   | ASE3-27.000MHz-K-T     | 27MHZ              | —        | ASE3-27.000MHz-K-T     | ABRACON                               | Standard Clock Oscillators 27.000 MHz 1.8 V 30 ppm                            |

| Item | Reference                                           | Qty | Part                     | PCB Footprint | Comments | Part Number              | Manufacturer    | Description                              |
|------|-----------------------------------------------------|-----|--------------------------|---------------|----------|--------------------------|-----------------|------------------------------------------|
| 54   | X4                                                  | 1   | KC3225A27.00<br>00C30E0A | 27MHZ_<br>OSC | —        | KC3225A27.00<br>00C30E0A | AVX Corporation | Standard Clock Oscillators<br>27.000 MHz |
| 55   | CrossLink Video Processing Input Board<br>Rev B PCB | 1   | —                        | —             | —        | 305-PD-16-<br>0XXX       | PACTRON         | —                                        |

On Revision B Crosslink VIP Input Bridge boards, [Figure C.1](#), the camera orientation is over/under. Later revision boards have the camera orientation side by side, refer to [Figure 1.1](#).



**Figure C.1. Top View of the CrossLink VIP Input Bridge Board Revision B**



## Revision History

### Revision 1.4, October 2018

| Section                                          | Change Summary                                                                            |
|--------------------------------------------------|-------------------------------------------------------------------------------------------|
| Programming Circuit                              | Changed value of device in Revision C under <a href="#">Table 3.1. SPI Flash Memory</a> . |
| Appendix A. CrossLink VIP Input Board Schematics | Added note in <a href="#">Figure A.4. Board to Board Connector and Flash Interface</a> .  |
| Revision History                                 | Updated revision history table to new template.                                           |

### Revision 1.3, February 2018

| Section                                                                    | Change Summary                                                                                                                                                                                                        |
|----------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Introduction                                                               | Updated board pictures to Revision C: <ul style="list-style-type: none"> <li>Figure 1.1. Top View of CrossLink VIP Input Bridge Board</li> <li>Figure 1.2. Bottom View of CrossLink VIP Input Bridge Board</li> </ul> |
| Programming Circuit                                                        | Added Table 3.1. SPI Flash Memory.                                                                                                                                                                                    |
| Power Supply                                                               | <ul style="list-style-type: none"> <li>Removed Power LEDs table (previously Table 5.1).</li> <li>Added information to Table 5.1. Device Power Rail Summary.</li> </ul>                                                |
| Appendix C. CrossLink VIP Input Bridge Board Revision B Camera Orientation | Added this section in this document.                                                                                                                                                                                  |

### Revision 1.2, January 2018

| Section      | Change Summary                                                                                |
|--------------|-----------------------------------------------------------------------------------------------|
| All          | Updated Lattice Semiconductor Logo on the cover pages, headers, and footers of this document. |
| Introduction | Changed CrossLink pASSP to CrossLink FPGA.                                                    |

### Revision 1.1, June 2017

| Section              | Change Summary  |
|----------------------|-----------------|
| Ordering Information | General update. |

### Revision 1.0, April 2017

| Section | Change Summary   |
|---------|------------------|
| All     | Initial release. |



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