

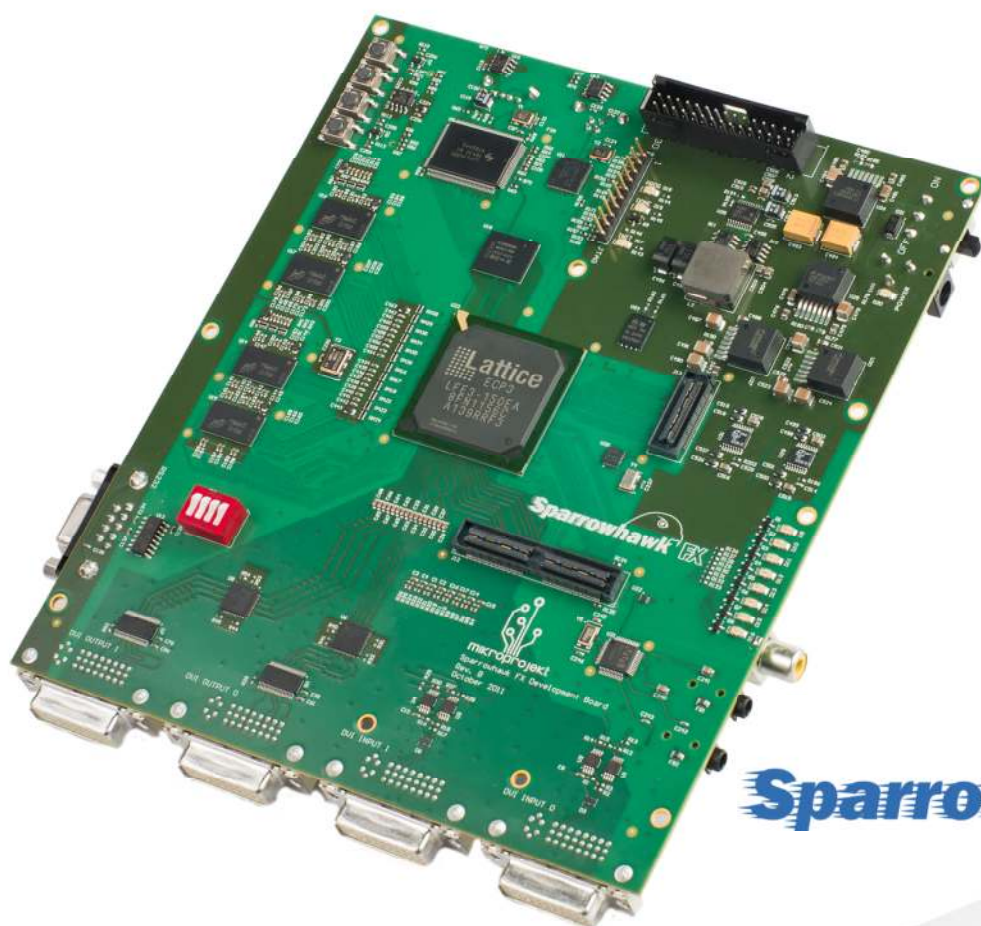
Sparrowhawk FX FPGA Video Processing Board

Overview Document

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The logo for Sparrowhawk FX, featuring a stylized blue bird head icon above the text "Sparrowhawk FX" in a bold, blue, sans-serif font.

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Contact info

Mikroprojekt d.o.o.

Aleja Blaža Jurišića 9

10040 Zagreb

Croatia

tel: +385 1 2455 659

fax: +385 1 2455 659

mail: contact@mikroprojekt.hr

web: <http://www.mikroprojekt.hr>

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Revision History

Revision	Date	Author	Modification
0.1	02.05.2011.	MR	Initial, Preliminary
0.2	25.05.2011.	MR	Corrected DDR3 speed grade to proper JEDEC name, Preliminary
0.3	26.07.2011.	MR	Added detailed subsystem descriptions, Preliminary
0.4	29.09.2011.	MR	Added details on audio. Added board photos.
0.5	14.02.2012.	MR	Added photos of board Rev.B (production)

Related Documents

ID	Code	Description

1 Introduction

The Sparrowhawk FX is an FPGA development board targeted for video acquisition, processing, and display applications, based on the award-winning Lattice ECP3 FPGA.

The Sparrowhawk FX board implements Mikroprojekt's IQ-Video solution, powered by the Peregrine system interconnect and Mikroprojekt's IP cores, enabling high performance computation. In conjunction with fast DDR3 Memory, the Sparrowhawk FX allows for reception, processing, arbitrary mixing and display of 4 independent DVI/HDMI video input and output streams in full HD 1080p60 resolution (1920x1080 @ 60 Hz, 24-bit color), with room to handle also the emerging 4k*2k video for next generation digital cinemas.

The IQ-Video solution employs Mikroprojekt's IP cores for video reception, display driving, and memory control to receive high definition video from the external interfaces. The IQ-ScaIR IP core allows for high quality, gradual scaling effects on video reception, after which the image is received and recorded to the memory by the IQ-VIN frame grabber. The IQ-DispML Multilayer Display Controller allows the display and compositing of multiple video streams and graphics by means of alpha blending, enabling Picture-in-Picture (PIP) and On-Screen Display (OSD) functionalities.

Reception and transmission of HDMI video streams is performed by Mikroprojekt's IQ-HDMI-Rx and IQ-HDMI-Tx IP cores, serving as DVI/HDMI video decoders and encoders, able to receive and transmit both video data and HDMI info frames, enabling the Sparrowhawk Fx to transmit, receive and process HDMI audio data. Sound input and playback is also supported through an onboard AC'97 audio codec.

While two inputs and two outputs are implemented on the board as DVI/HDMI, the remaining 2 SERDES I/O quads are connected to expansion ports. This allows the board to be expanded not only with the DVI/HDMI, but also with SDI and HD-SDI, DisplayPort, V-by-One HS, or other interfaces, such as Gigabit Ethernet.

The solution is controlled by the Lattice Mico32 Soft CPU implemented within the FPGA fabric. The Mico32 CPU allows precise control of the video timing, transition effects, and also supports the generation of OSD graphics within the solution, allowing the board to operate as a stand-alone video processor. Multiple Mico32 CPU cores can be added to control specific tasks. For high-quality OSD graphics generation, Mikroprojekt's IQ-GraphBlit 2D accelerator can be integrated.

Program data, graphics data and various parameters can be stored in the onboard parallel NOR flash device, or the SPI flash device used also for the FPGA design storage. An SD

Card slot with a full SD card interface is also provided. Buttons, DIP switches and LEDs are provided for basic communication and control of the system.

A high speed USB interface/debug link is supported, as well as the USB host functionality, allowing the board to interface to USB touchscreens or Web cameras. A standard RS-232 port is also provided for debug and configuration purposes.

1.1 Applications

- Digital signage
 - Video walls
 - Visual installations
- 3D display systems
 - Stereoscopic displays
 - Projection systems
 - Autostereoscopic displays
- Video acquisition systems
- Real-time video processing and mixing
- Machine vision
- Real time video format conversion/transcoding
- Multiple display driving

2 Board Features

Category	Features
FPGA	Lattice ECP3 LFE3-150EA-8FN1156 149.000 LUTs 372 Block RAMs 320 18x18 Multipliers 586 IO pins 16 SERDES channels (In/out) 400 MHz DDR3 Memory Support 10 PLLs, 2 DLLs
Video Memory	DDR3-800 (4) 4x Micron MT41J64M16JT-15E 400 MHz Clock Dual 32-bit channel (2x2 chips) 6.4 GB/s (theoretical maximum) 512 MB Total memory (expandable to 1024 MB)
Video interfaces	2x DVI/HDMI Input (DVI connector) 2x DVI/HDMI Output (DVI connector) DDC Supported on all in/out connectors
Nonvolatile storage	Numonyx M29EW Parallel NOR Flash 512Mbits (64MB) – expandable to 2Gbits (256 MB) ST M25P32 SPI Flash (Stores FPGA Configuration) Secure Digital Card slot
Audio Interfaces	Wolfson WM9707 AC'97 2.1 Audio Codec Stereo Line Out Stereo Line In S/PDIF Out
Communication Interfaces	Cypress CY7C68013A USB 2.0 Device STEricsson ISP1760 USB 2.0 Host RS-232 Interface I2C Bus (On all expansion connectors)
Expansion ports	Expansion Connectors (3) 1x Low Cost Expansion 2.54mm 30-pin header (22 GPIOs) 1x Samtec QSH-060 Expansion Connector (48 GPIOs, 8 SERDES In, 8 SERDES Out, 1 dedicated clock input) 1x Samtec QSH-030 Expansion Connector (44 GPIOs, 2 dedicated clock inputs) 114 GPIO pins in total
Other peripherals	Push-buttons (4) DIP Switches (4) LEDs (8)

Category	Features
Power Supply	12V Input Power switch Onboard 5V, 3V3 Switching power supplies Onboard 1V5 DDR3 Switching power supply Onboard FPGA 1V2 Core voltage linear regulator
Clocking	Onboard 100MHz Oscillator Onboard Programmable Clock Generator for SERDES/Video Interfaces – SiLabs
Manufacturing	RoHS Compliant

Table 1: Sparrowhawk FX feature list

2.1 Block schematic

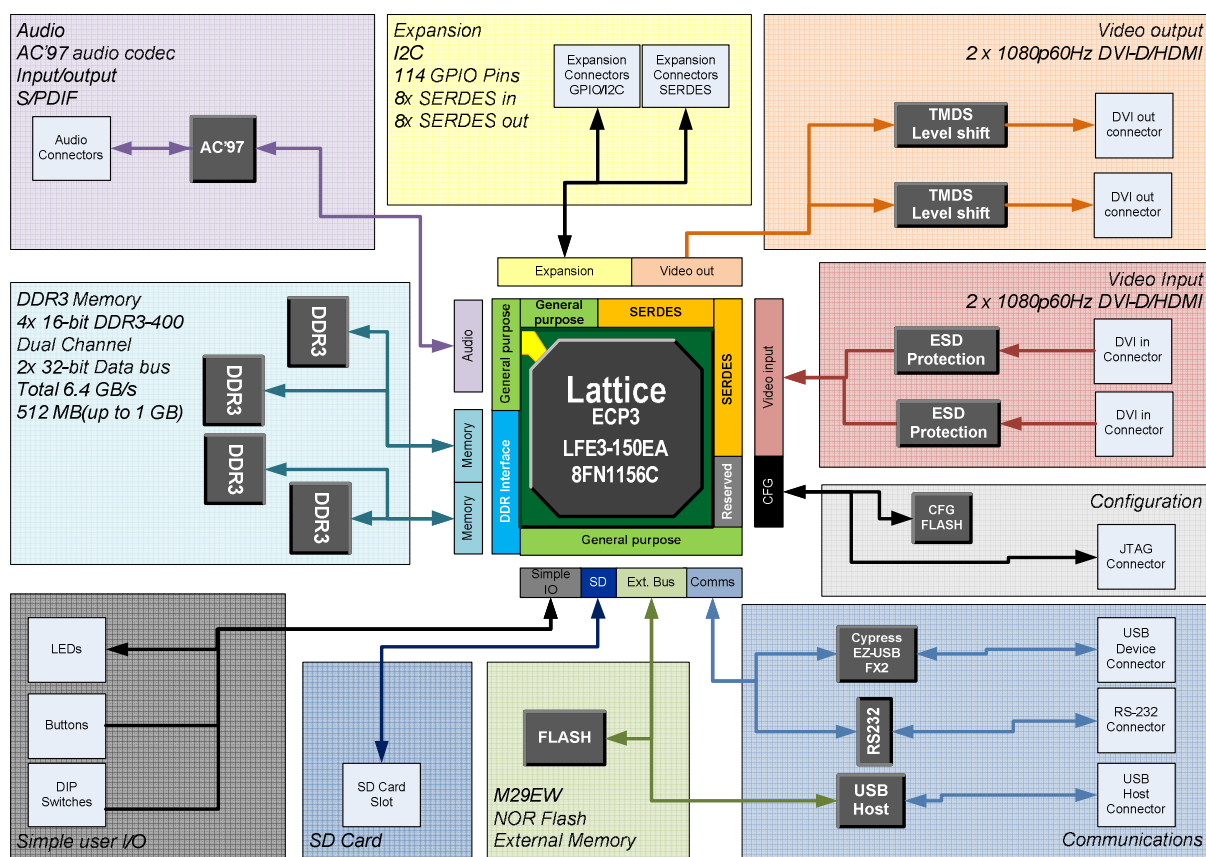


Figure 1: Sparrowhawk FX block diagram

2.2 Board layout

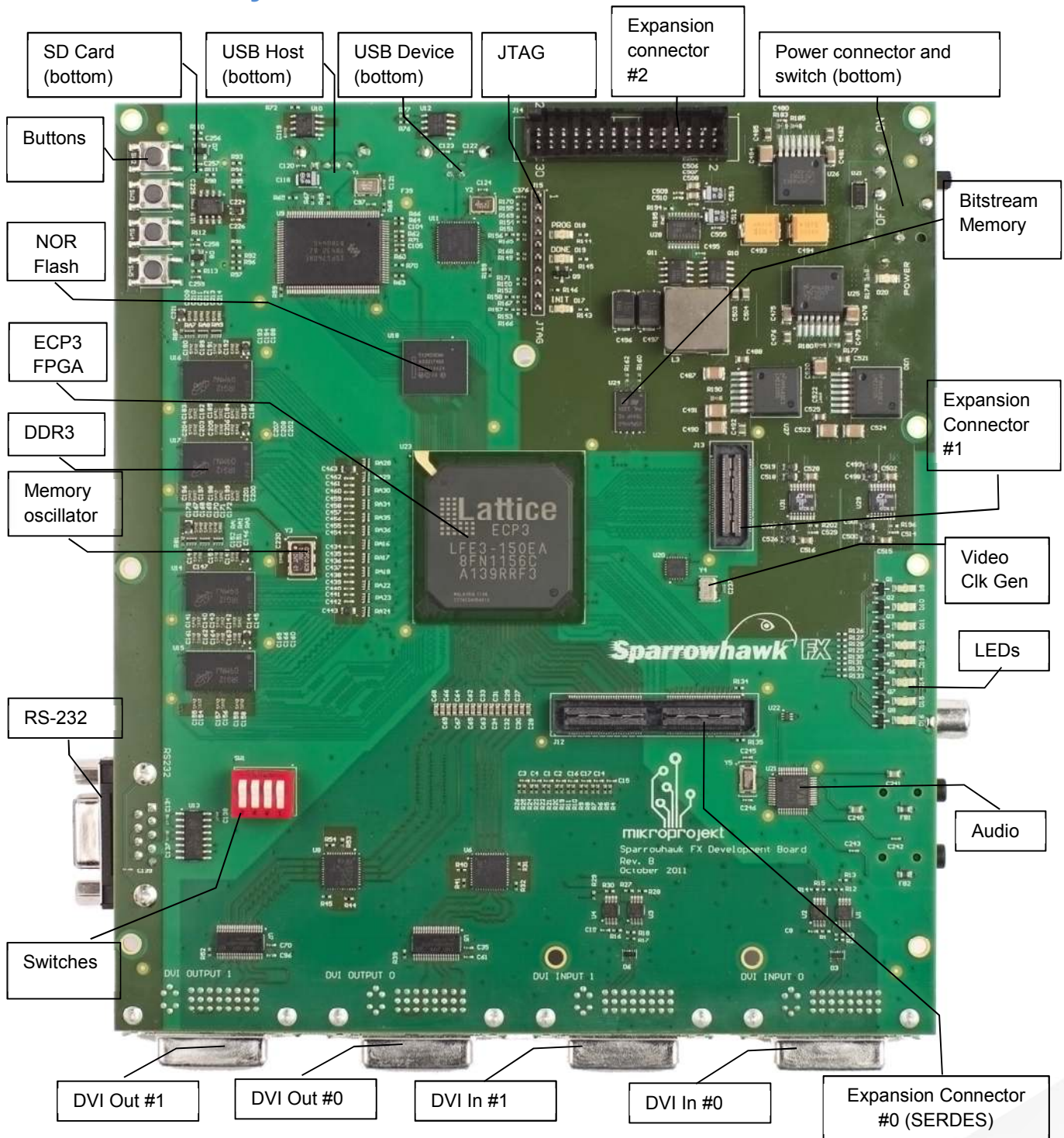
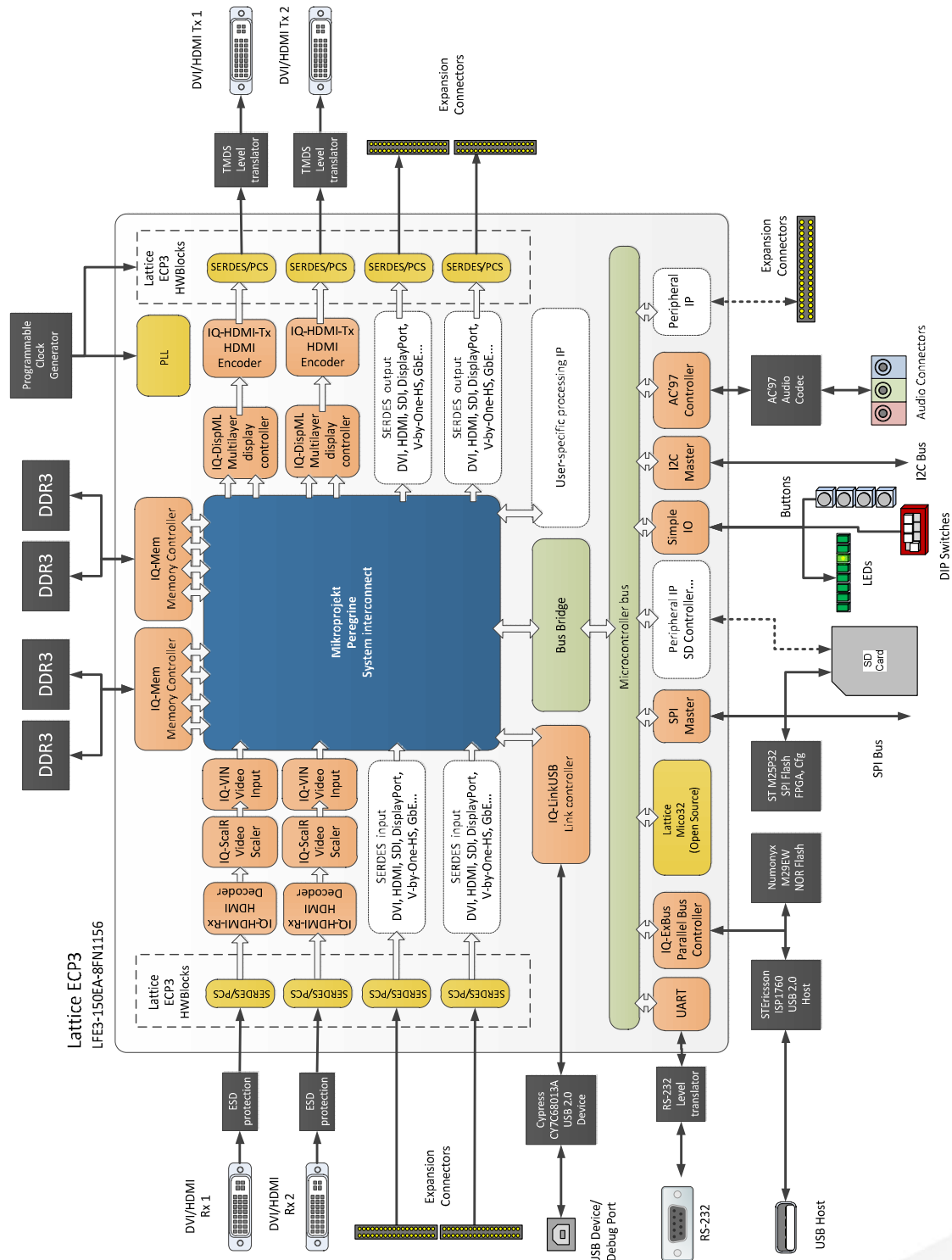


Figure 2: Sparrowhawk FX board layout

3 Reference design SoC Architecture



3.1 Basic architecture

The basic architecture of the Sparrowhawk FX SoC is built around Mikroprojekt's IQ-Video video processing solution, based on the Peregrine system interconnect.

3.1.1 Peregrine system interconnect

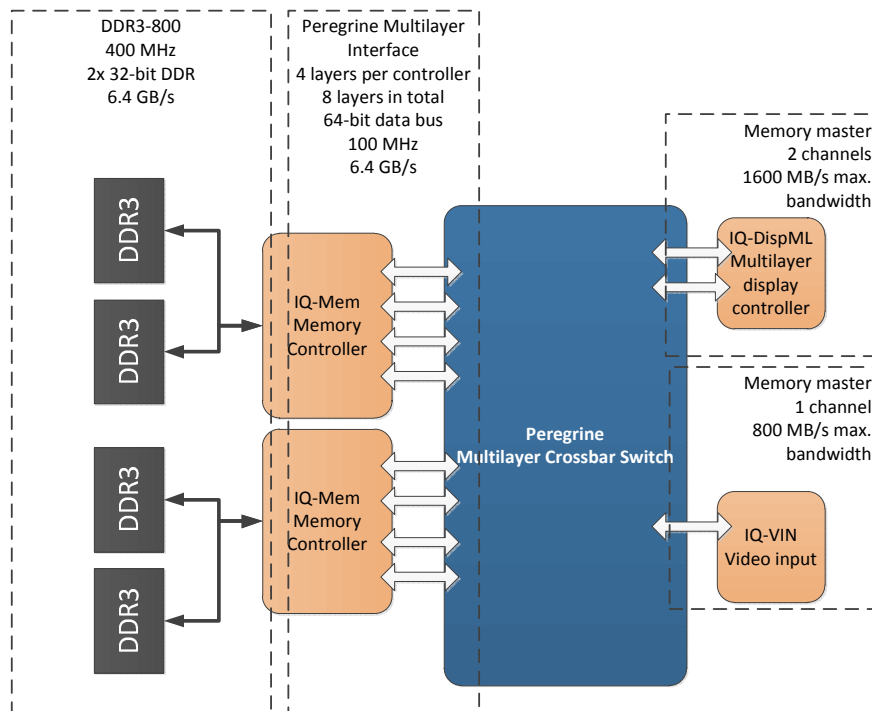


Figure 3: The Peregrine System Interconnect Architecture

The Peregrine system interconnect architecture is Mikroprojekt's answer to the bandwidth issues in high performance video applications on FPGAs. The Peregrine bus is a multi-layered crossbar switch allowing the connection of multiple bus masters to bus slaves over multiple data channels, reducing bus congestion and allowing higher throughputs.

The bus transactions are optimized for long sequential burst accesses commonly encountered in video applications. The memory controller is a vital part of the architecture, providing multiple separated access channels, which additionally allow for zoning and hardware decoupling of individual bandwidth utilization regimes, to ensure the maximum efficiency of operations on the memory interface. The memory controllers also integrate intelligent arbiters which optimize the order of accesses received over the multiple channels.

The Peregrine crossbar switch allows multiple masters to be connected to the memory over multiple layers. The total number of master channel connections can be greater than the number of slave channels. The Peregrine crossbar switch performs access arbitration between multiple masters. The arbiter can be programmed either to ensure priority and/or fairness between multiple masters.

The total delivered bandwidth to a single master is limited by the number of individual channel it can access. In the proposed configuration, each channel can deliver 800 MB/s of bandwidth, which is sufficient to simultaneously input and output one 1920x1080 full HD video stream at 60Hz.

3.2 Memory

The two IQ-MEM memory controller instances are used to drive a 2x2 memory array of DDR3 memory, running at 400 MHz (DDR3-800). Each pair of chips shares an address bus, and each chip has an independent data bus.

3.3 Video out

Video output is handled by Mikroprojekts IQ-HDMI-Tx and IQ-DispML IP Cores, enabling the driving of various display systems and panels through DVI/HDMI. The IQ-DispML display controller can also be used to drive a panel directly.

The IQ-DispML IP core allows mixing of video streams of various resolutions and color depths, combining multiple image layers into one output image with windowing, alpha blending and per-pixel transparency.

3.4 Video in

The solution integrates IQ-HDMI-Rx, IQ-VIN and IQ-ScalR IP cores for video reception. IQ-HDMI-Rx decodes the HDMI output and outputs the HDMI video data, audio and info frames to the IQ-VIN.

Within the IQ-VIN, the video data is first driven into the integrated IQ-ScalR IP core, where optional image scaling is supported, and one or more additional processing modules conforming to a standard interface. The HDMI audio data is bypassed directly to the output stage. Additional processing modules can be integrated into the datapath.

The output stage performs the final data encoding and transmits the video data to the memory, with support for various memory configurations (stripe and addressing, interleaving) and frame handling (frame skip).

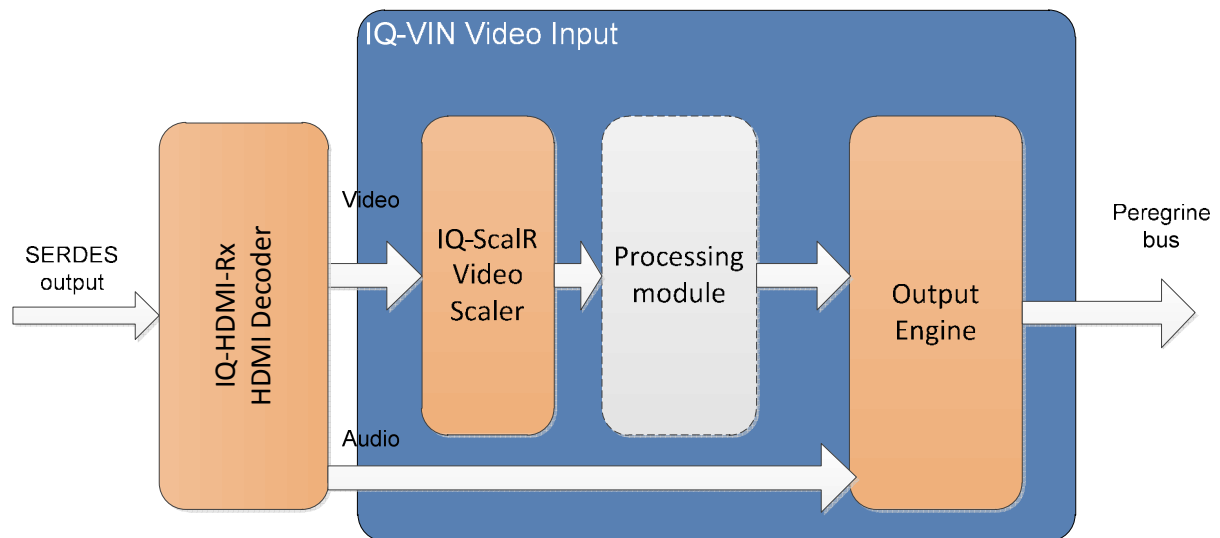


Figure 4: Video input processing

3.5 Peripherals

External connectivity to other systems is provided through several interfaces.

3.5.1 IQ-LinkUSB USB slave controller

The IQ-LinkUSB is an interface controller serving as a bus master on the Peregrine bus, performing operations delivered over the IQ-Link protocol from the external USB interface. The USB interface operation is handled through a Cypress CY7C68013A USB controller, integrating an 8051 microcontroller core to handle USB protocol requests, and providing a high-speed endpoint FIFO interface which allows high-bandwidth USB 2.0 transfers up to 30 MB/s delivered by the bulk endpoint transfers.

Single and burst read and write transfers can be issued by the USB host, which are executed on the Peregrine bus, with the results subsequently transferred back to the host.

The IQ-LinkUSB is employed as a debug and control link. The high bandwidth of USB 2.0 allows:

- download of test images and data,
- memory readback of various intermediate processing results
- run-time reconfiguration and download of software
- register setting and readout
- complete solution control

3.5.2 UART

The UART interface is a standard UART supporting speeds up to 115200 bps with hardware flow control on RS-232, or up to 3 Mbps for IrDA or other application. One RS-232 interface is included on the Sparrowhawk FX board, and is under control of the embedded microcontroller. Additional UART interfaces can be added using expansion.

3.5.3 I2C

Standard I2C bus controller is integrated and output to the expansion connectors. It is controlled by the embedded microcontroller.

3.5.4 SPI

An SPI master controller is embedded to support access and programming of the onboard SPI flash and the SD card. The master supports SPI access in all 4 modes with frequencies up to 50 MHz. Optionally, it can be expanded to support quad-speed SPI or higher frequencies.

3.5.5 Buttons, switches and LEDs

The system integrates 8 status LEDs, 4 DIP-style switches and 4 push buttons.

3.6 Nonvolatile storage

Several nonvolatile storage devices are supported:

3.6.1 Numonyx Axcell M29EW NOR Flash

The board integrates a parallel asynchronous NOR flash for storage of bulk data with fast access, such as test images, splash screens, and microcontroller software. The internal flash controller supports fast page read mode to extract maximum reading performance, up to 30 MB/s. TrueFFS flash file system implementation is feasible on the device.

3.6.2 SD Card slot

Secure digital cards (SD/SDHC/SDXC) are supported on the Sparrowhawk FX board, and a slot is present on the board. The default access method is through the SPI bus. Additionally, a SD controller IP core can be integrated to support high-speed data reads and writes. SD cards support multi-gigabyte storage for embedded video and graphics.

3.6.3 SPI Flash

An ST M25P32 SPI flash is connected to the FPGA. This device serves as the FPGA design storage, and can be accessed for field updates of the board's FPGA over software. Additionally it can hold an additional "safe" FPGA image for dual boot, software for an embedded microprocessor, or application-specific data.

3.6.4 USB Host

Optionally, USB mass storage devices can be supported through the onboard USB 2.0 host.

3.7 Audio

The board comprises a Wolfson WM9707 AC'97 audio controller. 3,5mm stereo input and output jacks are available, as well as an RCA S/PDIF connector.

3.8 Embedded Microcontroller

3.8.1 Hardware description

The embedded microcontroller is a Lattice Mico32 32-bit Harvard RISC microprocessor. The processor is optimized for Lattice FPGA devices. It has 32 32-bit general purpose registers. The processor employs a 6-stage pipeline for higher throughput, and achieves up to 115 MHz within the Lattice ECP3.

For highly embedded operations, or to accelerate certain applications, Inline memory can be attached to the processors for fast access, avoiding the cache. Both instruction and data inline memory is supported.

The processor is available in multiple configurations, ranging from Basic, highly embedded version with no multipliers, caches and pipelined shifters, Standard, with no caches, but fully pipelined and with hardware multipliers, and Full, with caches added.

The implementation data for Standard and Full configurations is given in Table 2. Beside the numbers is the total percentage of the ECP3-150 resources.

Version	LUT4s	REGs	MULs	ALUs	EBRs
Standard	2702(2%)	1296(1%)	8(1%)	4(1%)	4(1%)
Full	3361(3%)	1645(2%)	8(1%)	4(1%)	14(4%)

Table 2: FPGA utilization of Mico32 CPU variants usable for computation

The microcontroller is sufficiently small to facilitate use of multiple processors embedded.

3.8.2 Functionality

The Software embedded in the primary microcontroller controls the overall system, providing control for:

- device power-up
- system state
- initialization of hardware such as video inputs, display controllers and video processors
- ddc readout
- service and test patterns
- UART communication

A bootloader can be programmed in the SPI flash and loaded on system startup, after which the microcontroller can load additional software and data from other nonvolatile storage.