MachXO2 Family Data Sheet Supplement for LVCMOS10 Inputs and BIDIs

Data Sheet

FPGA-DS-02062-1.3

July 2021

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1. Overview

This document is a supplement to the MachXO2 Family Data Sheet and provides the following additions or customizations:

- Support for LVCMOS10R33 and LVCMOS10R25 inputs and BIDIs for all ZE devices and –6 speed grade for HE and HC devices

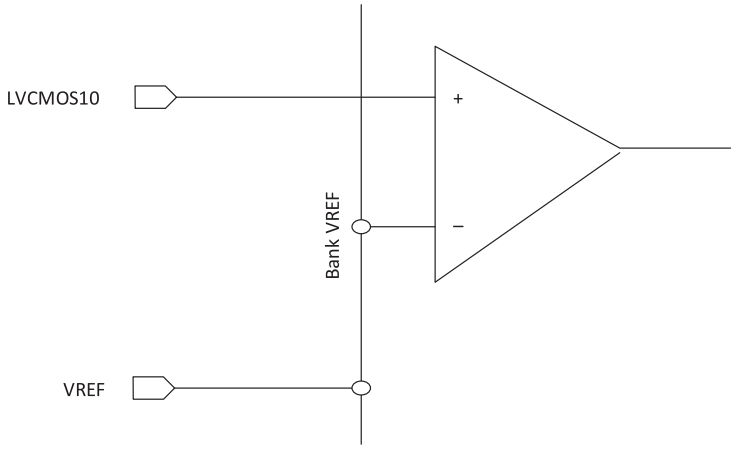

Figure 1.1.

2. sysI/O Recommended Operating Conditions

Table 2.1. sysI/O Recommended Operating Conditions

Standard	V_{CCIO} (V)			V_{REF} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVCMOS10R33	3.135	3.3	3.6	0.35	0.5	0.65
LVCMOS10R25	2.375	2.5	2.625	0.35	0.5	0.65

3. sysI/O Single-Ended DC Electrical Characteristics

Table 3.1. sysI/O Single-Ended DC Electrical Characteristics[1]

Input/Output Standard	V_{IL}		V_{IH}		V_{OL} Max. (V)	V_{OH} Min. (V)	I_{OL} (mA)	I_{OH1} (mA)
	Min. (V)	Max. (V)	Min. (V)	Max. (V)				
LVCMOS10R33	-0.3	VREF – 0.1	VREF + 0.1	3.465	0.40	N/A Open Drain	16, 12, 8, 4	N/A Open Drain
LVCMOS10R25	-0.3	VREF – 0.1	VREF + 0.1	3.465	0.40	N/A Open Drain	12, 8, 4	N/A Open Drain

1. For I/Os with mixed voltage support, V_{OH} follows respective sysI/O bank V_{CCIO} supply voltage, and V_{IL} / V_{IH} follows the I/O signaling standard.

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Revision 1.3, July 2021

Section	Change Summary
sysI/O Single-Ended DC Electrical Characteristics	Added note 1 in Table 3.1 to better clarify the voltage specifications for I/Os with mixed voltage support.

Revision 1.2, November 2019

Section	Change Summary
All	• Changed document number from DS1035 S to FPGA-DS-02062. • Updated document template.
Disclaimers	Added this section.

Revision 1.1, November 2015

Section	Change Summary
Overview	Corrected typo error in this section.

Revision 1.0, November 2015

Section	Change Summary
All	Initial release.

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