SiI9616 4K Video Processor with Integrated 300 MHz HDMI Receiver and Transmitter

Data Sheet

SiI-DS-1119-B

June 2017

Contents

Figures

Tables

1. General Description

The Lattice Semiconductor SiI9616 video processor supports all the video processing requirements for an Audio Video Receiver (AVR), Blu-ray player/recorder, and other video processors. It also incorporates an integrated HDMI/MHL™ receiver, and HDMI transmitter that supports HDCP repeaters.

Lattice Semiconductor VRS® ClearView video processing enhances video streaming quality with noise reduction, Video Smoothing™, and picture enhancement. VRS® ClearView also includes a 4K adaptive scaler to drive the emerging 4K display market.

The SiI9616 device is preprogrammed with High-bandwidth Digital Content Protection (HDCP) keys for both receiver and transmitter, which helps reduce programming overhead and lowers manufacturing costs.

The SiI9616 video processor is designed for AVR applications that require support for HDMI and video processing as shown in Figure 1.1.

1.1. Video Processor

- Supports video input formats up to 1080p and UXGA, including 4K x 2K pass-through
- Supports video output formats up to 1080p, WUXGA, and 4K x 2K
- Full 10-bit Adaptive Scaler
- Mosquito Noise Reduction
- Supports upscaling to 4K x 2K
- Supports downscaling from 1080p 60 Hz
- Video smoothing (pre- and postscaler)
- Detail and edge enhancement (prescaler)
- 12-bit preprocessing including color space conversion and picture control
- 12-bit post processing including color space conversion
- Overlay mixer of HDMI and parallel video paths
- Picture controls
- Test Pattern Generator

1.2. On-screen Display (OSD)

- Character-based
- Supports OSD over 3D video
- Supports alpha blending

1.3. Video Inputs

- 300 MHz HDMI receiver port with 3D support
- MHL with 1080p 60 Hz support
- 165 MHz 36-bit parallel video input with genlock support

1.4. Video Outputs

- 300 MHz HDMI transmitter port
- 165 MHz 36-bit parallel video output

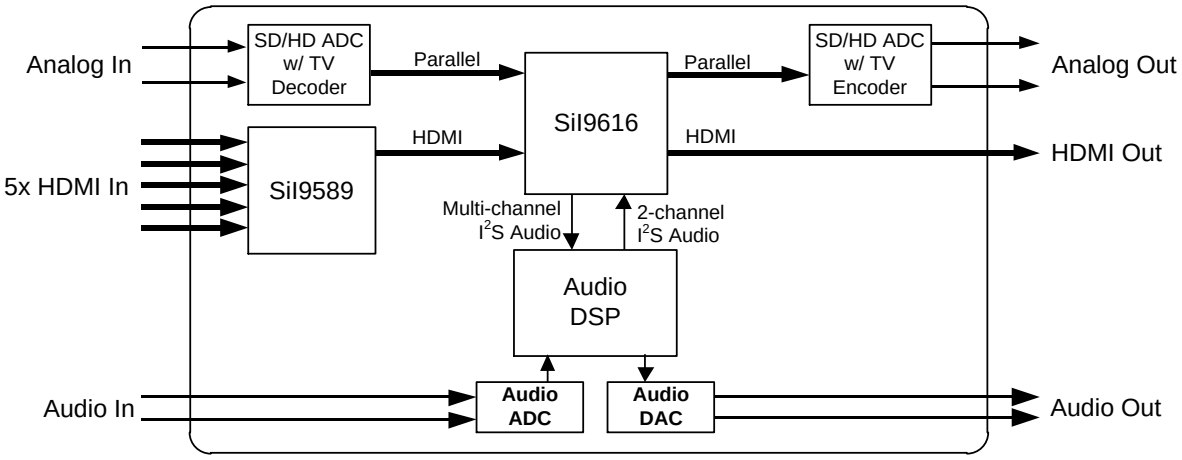


Figure 1.1. Typical Application

1.5. Digital Audio Interface

- Inputs
  - I^2S input with multichannel support
  - S/PDIF input
  - Audio Return Channel (ARC) input
- Outputs
  - I^2S output with four data signals for multichannel formats, and flexible programmable channel mapping, including DSD
  - High Bitrate Audio output including Dolby® TrueHD and DTS-HD Master Audio™
  - S/PDIF output supports LPCM, Dolby Digital, DTS digital audio transmission with a 32 kHz - 192 kHz f_S sample rate
- Intelligent audio mute capability avoids pops and noise with automatic soft mute and unmute
- IEC60958 or IEC61937 compatible

1.6. Control

- I^2C and Serial Peripheral Interface (SPI) Bus
- DDC for HDMI receiver and transmitter
- Consumer Electronics Control (CEC) interface incorporates an HDMI CEC I/O and an integrated CEC Programming Interface (CPI)

1.7. Package

- 20 mm x 20 mm 176 pin TQFP package with an exposed pad (ePad)

2. Functional Description

The SiI9616 video processor is ideally suited for A/V receivers, Blu-ray player/recorders, and video processing applications. It features a digital processing core that performs real-time video format conversion and image improvement. Format conversion is achieved through an innovative adaptive scaler that allows the device to upscale from any input format to 4K x 2K resolutions. Proprietary video processing algorithms improve the picture quality by removing unnaturally appearing noise or artifacts, smoothing edges, and sharpening the image. Image improvement is supported for both standard and high-definition video.

An on-chip character generated On-screen Display (OSD), organized as 108 x 30 rows and columns, is included in the SiI9616 device. The OSD has split-screen mode to support display of the OSD over a 3D image.

The SiI9616 device provides a Test Pattern Generator (TPG) that is fully programmable by software and is able to generate test patterns without a valid input signal. With a maximum supported resolution of 4096 x 2208, it is able to generate test patterns for both 4K x 2K and 1080p 3D video output formats.

The SiI9616 video processor integrates a full 300 MHz HDMI receiver and HDMI transmitter. Mobile High-definition Link (MHL™) technology is available on the HDMI receiver. The MHL receiver supports PackedPixel mode. The Audio Return Channel (ARC), provided for the HDMI transmitter port, allows the SiI9616 device to receive a S/PDIF signal from the connected DTV.

In addition to HDMI input and output, the SiI9616 device also supports a 36-bit parallel video input and 36-bit parallel video output. These parallel video ports are highly configurable through software and support a wide range of input and output data mappings.

The parallel video input accepts video from an external source such as another HDMI receiver or a video decoder, or it can accept an externally generated OSD, which the SiI9616 device can overlay on top of the primary video stream. The SiI9616 video processor provides a set of software programmable genlock signals that an external OSD generator can use for timing synchronization.

The parallel video output can be active at the same time as the HDMI output. It can select among the processing output, HDMI input, or parallel input as its source independent of what is selected for the HDMI output. So, it is ideal for driving an external video encoder to support simultaneous analog and digital video outputs typically seen on A/V receivers.

The SiI9616 video processor supports audio extraction and insertion. Audio extracted from the HDMI receiver can be output simultaneously to a S/PDIF port, a multichannel I^2S port, and to the HDMI transmitter for repacketization. Audio to be transmitted on the HDMI output can be selected from one of four other sources: S/PDIF input, two-channel I^2S input, multichannel I^2S input, and ARC input. The video processor can also convert the LPCM data received from the two-channel I^2S input or the I^2S output of the HDMI receiver to an IEC60958 stream to output on the S/PDIF port.

Figure 2.1 below and Figure 2.2 on the next page show the functional blocks of the chip.

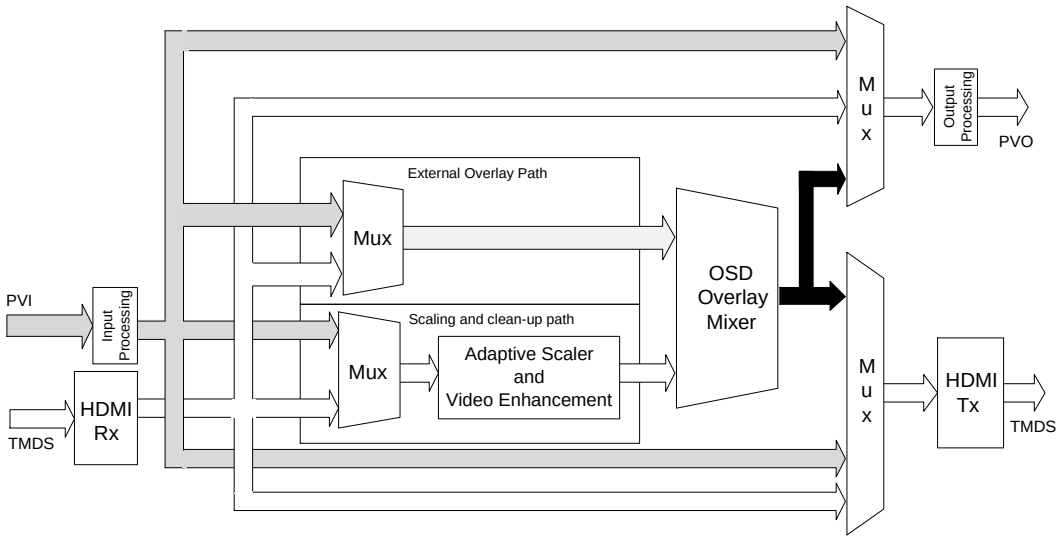


Figure 2.1. Functional Video Path Block Diagram

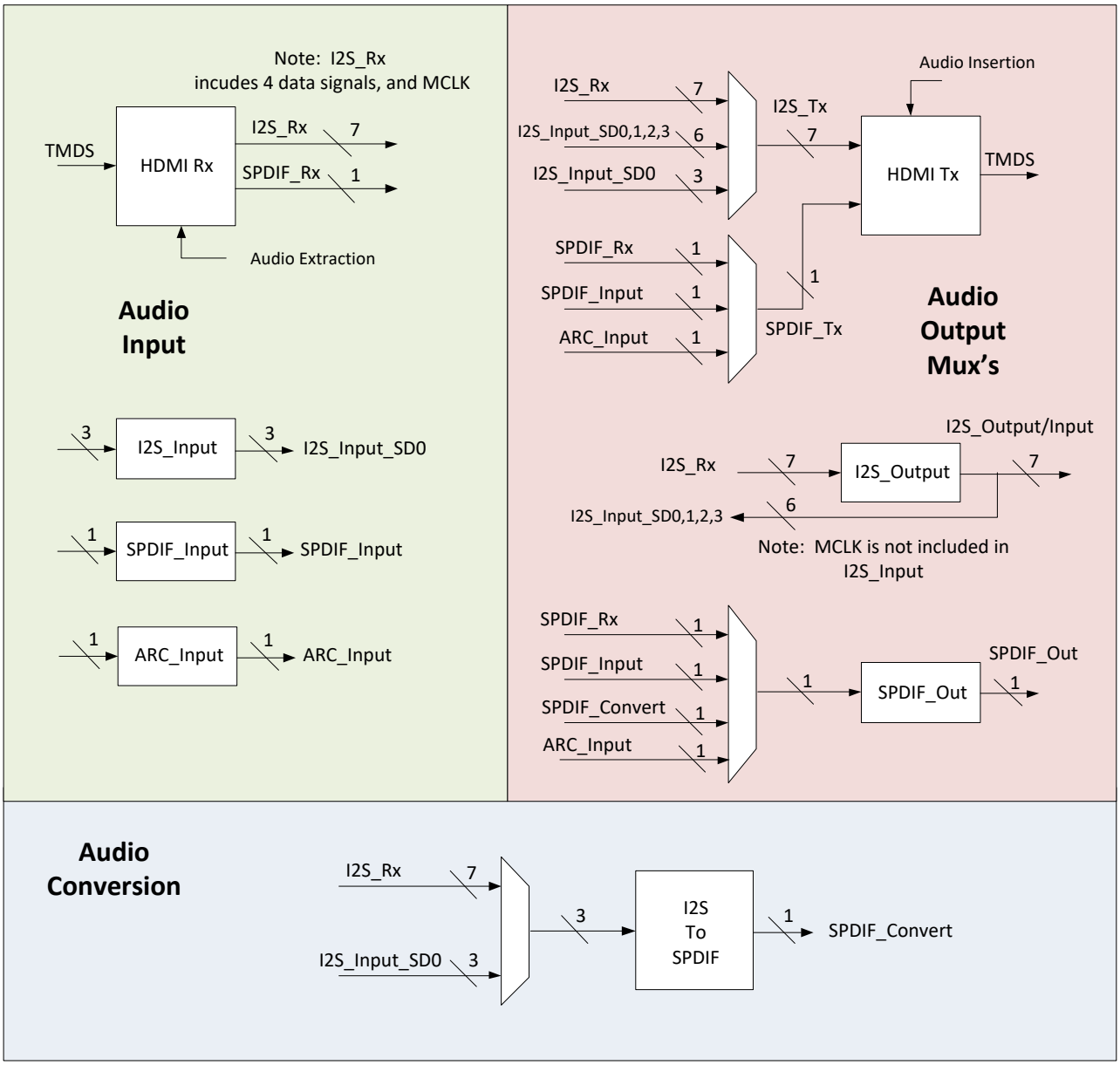


Figure 2.2. Audio Path Block Diagram

Table 2.1 summarizes the audio outputs that are available with each audio input.

Table 2.1. Audio Multiplexing Options

Audio Input	Audio Output			
	SPDIF_Out	I2S_Output	HDMI SPDIF_Tx	HDMI I2S_Tx
SPDIF_Input	Supported	—	Supported	—
I2S_Input	Supported (2-ch formats)	Supported	—	Supported
HDMI SPDIF_Rx	Supported	—	Supported	—
HDMI I2S_Rx	Supported (2-ch formats)	Supported	—	Supported
ARC_Input	Supported	—	Supported	—

2.1. Video Processor

The SiI9616 video processor features the latest VRS® technologies from Lattice Semiconductor, including a 4K Adaptive Scaler, Video Smoothing, enhanced Mosquito Noise Reduction, and Detail and Edge Enhancement. These technologies improve the picture quality of highly compressed video sources by enhancing resolution through scaling and removing video noise without side effects. Adaptive scaling delivers automatically optimized performance for all sources including internet video, high-definition video, and computer graphics. All processing resources are included on-chip and external RAM is not required.

2.1.1. Supported Input Resolutions to Video Processing Core

The SiI9616 video processing core supports several input formats per the CEA-861E Specification. It also supports several PC formats. Supported formats include, but are not limited to, the following:

- 720 x 480i
- 720 x 576i
- 1440 x 480i
- 1440 x 576i
- 720 x 480p
- 720 x 576p
- 1280 x 720p50
- 1280 x 720p60
- 1920 x 1080i50
- 1920 x 1080i60
- 1920 x 1080p50
- 1920 x 1080p60
- VGA
- SVGA
- XGA
- SXGA
- UXGA
- 4K x 2K (at 23.98 Hz, 24 Hz, 25 Hz, 29.97 Hz, and 30 Hz) pass-through
- 4K x 2K YCbCr 4:2:0 (at 59.94 Hz, 60 Hz, and 50 Hz) pass-through

1080p resolutions may require a small amount of vertical zoom when scaling down to certain SD resolutions.

The SiI9616 video processor does not support frame rate conversion. The output frame rate always needs to be the same as the input frame rate.

2.1.2. Special Considerations for 4K x 2K Inputs

4K x 2K inputs must bypass all major processing blocks. In this mode, color space conversion and picture controls are still available. The exception is YCbCr 4:2:0-encoded 4K x 2K 60 Hz (59.94 Hz) and 50 Hz inputs, in which color space conversion and picture controls must also be bypassed.

Figure 2.4 on page 14 shows the bypass modes available on the SiI9616 video processor.

2.1.3. Supported Output Resolutions

The SiI9616 video processing core supports several output formats including the following:

- 480i
- 480p
- 576i
- 576p
- 720p
- 1080i
- 1080p
- VGA
- SVGA
- XGA
- SXGA
- UXGA
- 4K x 2K (at 23.98 Hz, 24 Hz, 25 Hz, 29.97 Hz, and 30 Hz)
- 4K x 2K YCbCr 4:2:0 (at 59.94 Hz, 60Hz, 50Hz)

The SiI9616 device does not support frame rate conversion. The output frame rate always needs to be the same as the input frame rate.

2.1.4. Video Processing Blocks

The SiI9616 video processor contains the following video processing blocks:

- Input Preprocessing reformats the input signal to YCbCr 4:2:2 format
- Mosquito Noise Reduction
- Standard Definition Edge Smoothing
- High-definition Detail and Edge Enhancement
- Adaptive Video Scaling
- High-Definition Edge Smoothing
- Test Pattern Generation
- External OSD Blending
- Internal OSD Blending
- Output Postprocessing reformats the video data to many different output formats

Figure 2.3 on the next page shows a block diagram indicating the placement of these blocks in the video path.

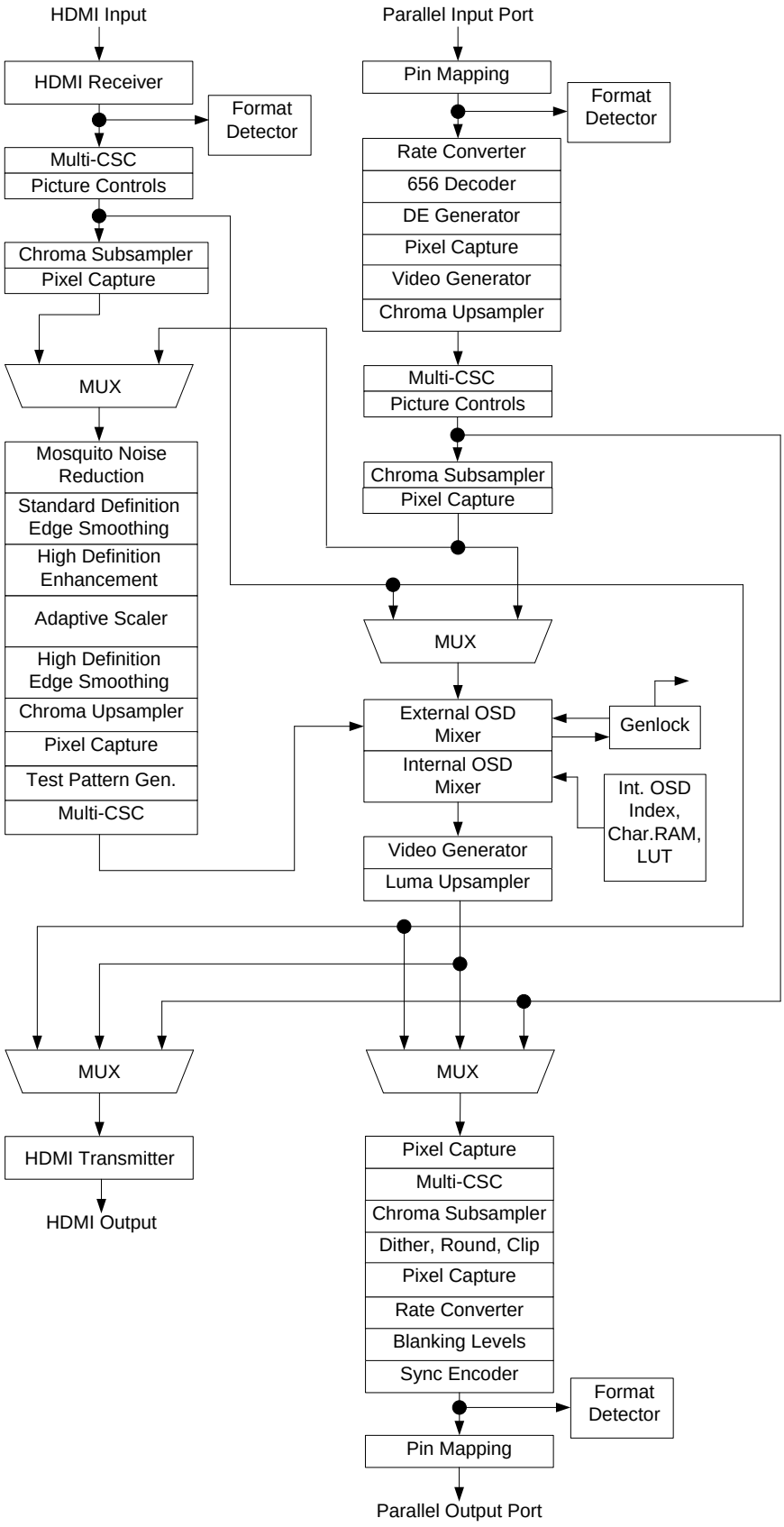


Figure 2.3. Video Processing Block Diagram

2.1.5. Bypass Modes

The SiI9616 device has several options for bypassing the internal processing blocks using control registers that are described in the SiI9616 Programmers Reference *(SiI-PR-1069; Requires NDA with Lattice Semiconductor)*. Figure 2.4 shows the available bypass options.

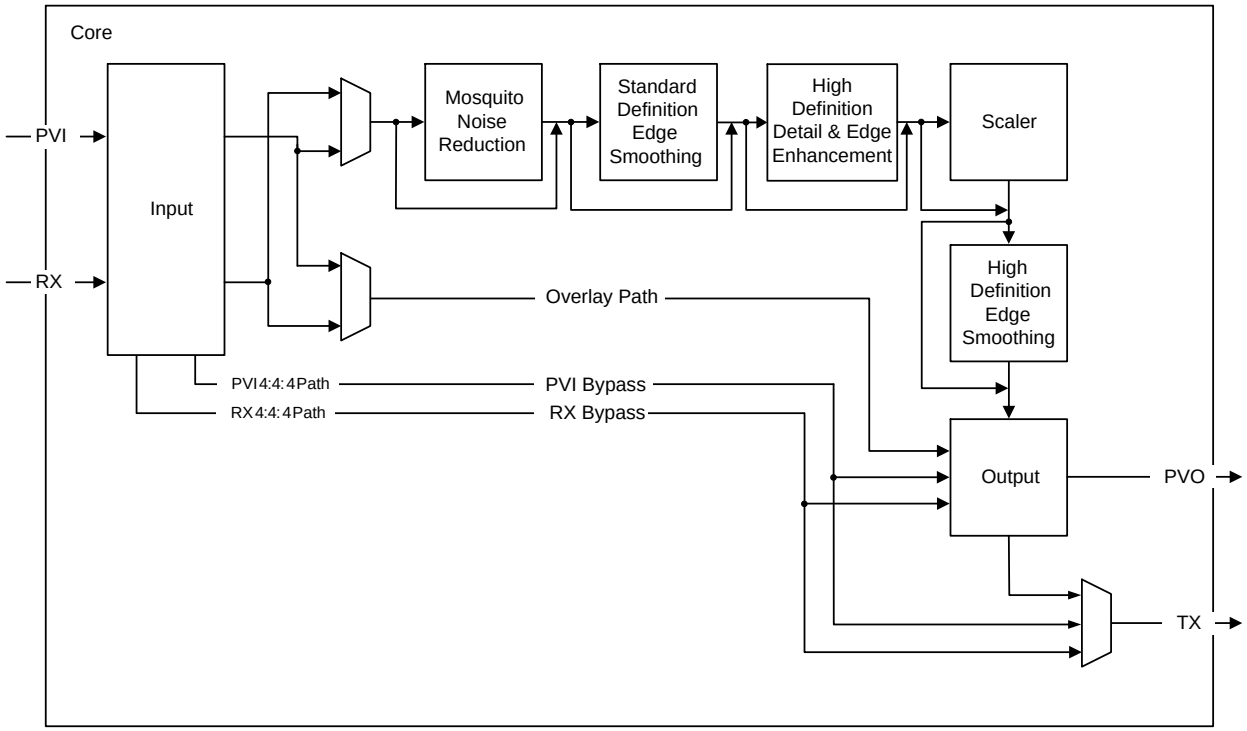


Figure 2.4. Bypass Options

2.1.6. Processing Mode

In processing mode, the output of the SiI9616 video processor can be in RGB or YCbCr mode. Multiple color space converters, chroma upsampler, and chroma downsampler logic blocks are available on the input and output of the processing block to ensure support for a wide range of applications. The pins of the parallel video input and output can be remapped to meet the specific requirement of the application.

2.2. Input Preprocessing

The SiI9616 device provides a number of video processing functions, which can be used to adjust the incoming video signal before it is sent to the scaler and enhancement blocks. These functions are color space conversion, picture controls, and chroma upsampling/subsampling. All processing is done in 36 bits.

2.2.1. Picture Controls

Picture controls are used to adjust the following aspects of the video input signal:

- Input Black Level
  - 4096 levels of black level control
- Contrast
  - 1 integer bit, 8 fractional bits. Range is from 0 to 1.996 with a 1/256 resolution for a total of 512 levels of contrast control
- Saturation
  - 1 integer bit, 8 fractional bits. Range is from 0 to 1.996 with a 1/256 resolution for a total of 512 levels of saturation control

2.2.2. 3 x 3 Matrix (Multicolor Space Converter)

In addition to the built-in picture controls, the SiI9616 device features two 3 x 3 matrix modules at the input path. These can be used as programmable linear control to adjust the brightness, contrast, saturation, and hue in the three components of the input signal. They can also be used to perform RGB-to-YCbCr and YCbCr-to-RGB color space conversions.

The 3x3 matrix also comes with 64 sets of predefined coefficients to support all standard color space conversions.

Table 2.2 shows the eight possible formats available for the input and output of the 3 x 3 matrix.

Table 2.2. Multicolor Space Converter Input/Output Formats

Color Space	Levels	Colorimetry
YCbCr	Video	709
YCbCr	Video	601
YCbCr	PC	709
YCbCr	PC	601
RGB	Video	709
RGB	Video	601
RGB	PC	709
RGB	PC	601

2.2.3. Chroma Upsampler/Subsampler

The chroma upsampler converts YCbCr 4:2:2 input signals to YCbCr 4:4:4 format while the chroma subsampler module performs the reverse operation, it converts YCbCr 4:4:4 input signals to YCbCr 4:2:2 format.

2.3. Mosquito Noise Reduction

The SiI9616 video processor detects and removes mosquito noise. Mosquito noise is a common compression artifact caused by MPEG decoders, and is often exhibited around the edges of text and computer generated graphics. The SiI9616 algorithm detects areas where mosquito noise would be the most likely, and then works to diminish the mosquito noise without blurring the edge of the text or graphic. The maximum resolution supported by mosquito noise reduction is 576p.

2.4. Video Smoothing

The Lattice Semiconductor Video Smoothing™ technology removes the rough edges in an image, such as the staircase appearance of a diagonal line drawn on the screen without edge smoothing (stair stepped effect). Digital compression, scaling artifacts, poor quality deinterlacing, or resolution limitations in the digital sampling of an image cause these effects. Smoothing technology creates the effect of a high-resolution image without softening the entire image.

The SiI9616 device offers two smoothing blocks. The Standard Definition Edge Smoothing block comes before the scaler and removes any rough edges on the original image. The High-definition Edge Smoothing block comes after the scaler and and it reduces rough edges caused by upscaling the video.

2.5. Detail/Edge Enhancement

There are two types of sharpening in the SiI9616 device: general and edge-qualified. Sharpening is done before scaling in the High-definition Enhancement block. The High-definition Enhancement block works well for sharpening both SD and HD video.

Detail enhancement can be used to increase fine detail or reduce noise for overly enhanced images. Detail enhancement is controlled with an 8-bit signed register. Positive control numbers from 1 to 127 increase sharpening and negative numbers in two's-complement format decrease sharpening. This means that if the control word is negative, the image is low-pass filtered. The control register defaults to 0, which does not apply any sharpening.

Edge enhancement can be used to sharpen edges or reduce overly enhanced edges. The edge-qualified sharpening or edge enhancement works only on object edges. It also uses an 8-bit signed control word, like general sharpening, so sharpening can increase around object edges if the control word is positive, and edges of objects can be filtered if the control word is negative. There is a *clipping* control for edge-qualified sharpening that allows for adjustment of edge sensitivity. The clipping control is also an 8-bit number, but it is unsigned. The clipping control allows the user to select the strength of object edges to which sharpening is applied.

The detail enhancement and edge-qualified enhancement methods are additive, so the results of both sharpening methods are combined. An example of this would be to use general sharpening to increase detail in the entire image. If object edges are overenhanced, then negative edge-qualified sharpening is applied to reduce the overenhancement of the edges. If general sharpening is applied to a noisy image, the increase in noise may be objectionable. In that case, positive edge-qualified sharpening should be applied to sharpen object edges, but not increase the noise level.

2.6. Scaler

The scaler provides format conversion capability to the SiI9616 video processor. It reads the input data from internal line memory and applies horizontal and vertical scaling. Adaptive scaling ensures that the converted format is free of ringing artifacts regardless of content, whether video, graphic, or a mix of both. Format conversion is supported for both video and PC formats.

The scaler does not support a frame buffer. The output frame rate is locked to the input frame rate. A small amount of vertical zoom is necessary when scaling down from 1080p resolutions to some SD resolutions, such as 480p.

The scaler can perform scaling on a limited set of Frame Packed 3D formats. The only 3D format conversions that work are conversions from 720p Frame Packed to 1080p Frame Packed, or from 1080p Frame Packed to 720p Frame Packed.

The scaler supports panorama mode, that changes the aspect ratio of the image. It can be used to fit a 4:3 SD image into a 16:9 HD format with minimal distortion. This is achieved by keeping the original image aspect ratio in the center of the scaled image, and gradually stretching the image towards its left and right edges. This results in no distortion at the image center while horizontal distortion gradually increases towards the left and right edges of the image. The panorama mode features an enhanced algorithm that reduces the distortion at the far edges of the image.

The scaler also includes both a border generator and a mask generator. The border generator is used to create a grey frame about the video image whereas the mask generator can be used to create a black frame around the border. Borders provide another method for correcting the aspect ratio of the displayed image, such as displaying a 4:3 image on a 16:9 frame without horizontal distortion by adding appropriately sized pillars on the left and right side of the image.

Other functions supported by the scaler block include: Y/C delay that allows a horizontal offset between the chroma and luma signal to compensate for delay differences caused by other parts of the system; automatic chroma upsampling error (CUE) correction, which detects chroma data that has been upsampled incorrectly in the vertical direction and suppresses the visual artifacts caused by these errors; and user-defined zoom and pan functions.

Scaler processing is done in YCbCr 4:2:2, 20-bit (10 bits per component) color space format.

2.7. Keystoning

The SiI9616 device supports Keystoning. Keystoning is necessary when an image is projected onto a surface at an angle resulting in a distorted image of a trapezoid. For example, if a projector is lower than the surface onto which it is projecting, the image is larger at the top than at the bottom.

2.8. Standalone Video Timing Generators

There are two standalone Video Timing Generators (VTG) in the SiI9616 video processor. One of the VTGs is available in the parallel video input data path while the other is located inside the scaler block. Both VTGs can be used to generate a solid colored screen with any output format supported by the device. For example, a 1080p signal which produces a solid blue screen, can be output when there are no inputs to the video processor.

The input clock for the VTGs can be selected from among these clock sources: 27 MHz system clock, PVI clock, HDMI input clock and internal PLLs.

2.9. Test Pattern Generator

The SiI9616 video processor has a programmable Test Pattern Generator (TPG). The TPG is flexible and under software control. It is able to generate test patterns without a valid input signal. The maximum output resolution of the TPG is 4096 x 2208. The 4096 horizontal resolution supports all 4K x 2K formats. The 2208 vertical resolution supports Frame Packed 3D formats up to 1080p.

The TPG operates in YCbCr 4:4:4 color space format at 12 bits per color component.

2.10. On-screen Display

The SiI9616 video processor comes with a built-in character-based On-screen Display (OSD). The OSD is organized as a 108 x 30 character map that can be positioned anywhere on the screen. 384 characters can be created at 12 x 24 pixels per character or 192 characters at 24 x 24 pixels per character. The OSD can support transparency and a maximum of 64 pairs of foreground and background colors. The maximum resolution of the OSD is 1296 x 720 pixels.

The OSD supports a split mode that allows it to be overlaid onto some 3D video formats. The OSD can be split vertically or horizontally. When split vertically, the OSD can be overlaid onto Frame Packed 3D formats or Top-and-Bottom 3D formats. When split horizontally, the OSD can be overlaid onto Side-by-Side 3D formats. However, 3D processing downstream from the SiI9616 device of Side-by-Side (Half) and Top-and-Bottom formats will distort the characters, as they will be expanded by 2x horizontally in a Side-by-Side (Half) format, or they will be expanded by 2x vertically in a Top-and-Bottom format.

2x, 3x and 4x pixel and line replication are supported for increasing the size of the OSD characters. Pixel replication is independent for horizontal and vertical. Pixel and line replication may be used to increase the legibility of the OSD for 4K x 2K output. The OSD is rendered in YCbCr 4:4:4 or RGB color space.

2.11. Video Overlay

The SiI9616 video processor can overlay video from one input port onto the main output. The main video is the one that goes through the processing path of the SiI9616 device. Its source is either the HDMI receiver or the Parallel Video Input (PVI). If the HDMI receiver is selected as the source of the main video, then the PVI is the input port for the overlay video. If the main video is supplied by the PVI port, then the HDMI receiver is the input port for the overlay video.

Overlay works only if the main video and the overlay video are synchronous and have the same timing. In other words, the VSYNC and HSYNC pulses must line up, and the DE areas must also line up. To achieve this the SiI9616 device provides a set of programmable genlock output signals that the external overlay source uses to synchronize to the output timing of the SiI9616 device.

Figure 2.5 on the next page illustrates an example of overlay. The desert scene represents the main video image while the ellipse represents the overlay image from an external source superimposed on top of the main video image. The active video region of the overlay input must be equal to the main output. The actual overlay is done over a programmable rectangle. The overlay rectangle can cover the entire screen or a smaller area, in which case it can be positioned anywhere within the background image.

Within the overlay rectangle, a chroma key may be used to select which portions of the overlay video area are not superimposed over the main image. A chroma key consists of a low and high value. If an overlay pixel value is within the low and high values, then overlay is not done and the main video is shown instead. If an overlay pixel value is outside the range of values defined by the low and high values, then the overlay image is shown instead of the main image. Chroma keying allows the overlay image to have a non-rectangular shape. An alpha bend value can be applied to adjust the transparency of the overlay image.

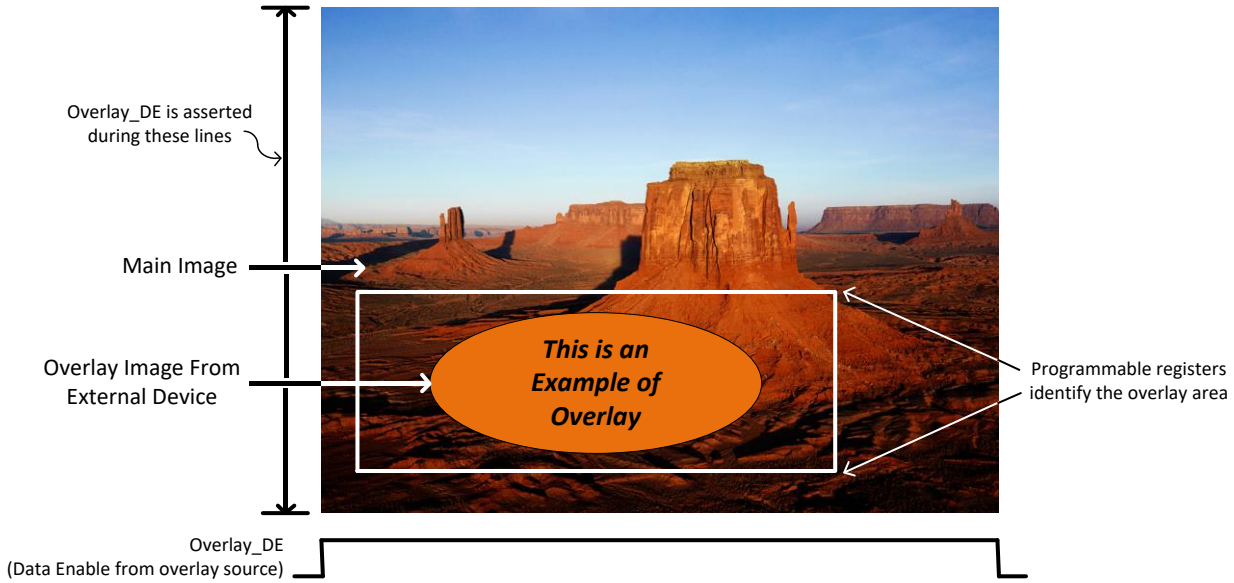


Figure 2.5. Video Overlay

2.12. Genlock Timing Signals

The video overlay function works only if the external video source is synchronized to the output timing of the SiI9616 device. The SiI9616 device provides a genlock signal for the external video source that it can use for synchronization. The genlock signal is comprised of four signals: Clock, VSYNC, HSYNC, and Data Enable (DE). The DE output can be reconfigured to send the field polarity (even/odd) signal instead of data enable. The reference signal for the genlock logic is the processed video output.

The timing of the genlock signal is programmable (except the clock) and must be programmed to match the timing of the main output of the video processor. The genlock module also supports programmable line and cycle delays, which can be positive or negative. The programmable delays are used to adjust the delay between the external overlay signal and the main video signal so that they are lined up properly before mixing. The overlay mixer module contains measurement logic to determine the delay between both signals.

2.13. Output Post Processing

Additional processing can be performed on the output data after the scaling/enhancement data path before it is sent to the HDMI transmitter or parallel output port. These functions are color space conversion, chroma upsampling/subsampling, dither/round, and range clip. All processing is done in 36 bits. Not all functions are available for the data path to the HDMI transmitter (see Figure 2.3 on page 13). The missing functions are supported by similar logic blocks in the HDMI transmitter.

2.13.1. Chroma Upsampler/Subsampler

The chroma upsampler and chroma subsampler modules are the same as those used in the input path.

2.13.2. 3 x 3 Matrix (Multicolor Space Converter)

There are two 3 x 3 matrix modules in the video output path. These are the same 3 x 3 matrix modules that are available in the input path. Like their counterpart in the video input path, these modules perform color space conversion using a user-programmed coefficient and offset values, or 64 predefined sets of coefficients for all standard color space conversions.

2.13.3. Dither/Round

This module performs dithering or rounding of the video data when reducing color depth.

The following rounding modes are supported:

- Round 12-bit to 10-bit
- Round 12-bit to 8-bit
- Round 10-bit to 8-bit
- No rounding

The following dithering modes are supported:

- Dither 12-bit to 10-bit
- Dither 12-bit to 10-bit
- Dither 10-bit to 8-bit
- No dithering

Dithering is performed by adding pseudo random noise to the video data before truncating it to a reduced color depth.

2.13.4. Range Clip

This module performs dynamic range clipping for video levels. The clipping levels are fully programmable. Clipping is defined by four parameters:

- Minimum clip level for Y channel
- Maximum clip level for Y channel
- Minimum clip level for Cb and Cr channels
- Maximum clip level for Cb and Cr channels

In RGB mode, the Y parameters are used for all three color components.

2.14. 4:2:0 Output

The SiI9616 video processor supports YCbCr 4:2:0 ready displays. The primary purpose of this pixel encoding format is to support the transmission of 4K x 2K 50/60 Hz formats using a link clock rate that is half the pixel clock rate, or 297 MHz, by reducing the bandwidth through chroma subsampling.

In YCbCr 4:2:0 format, the chroma components, Cb and Cr, are subsampled both horizontally and vertically with respect to the Y component by a factor of two. This produces a Y-to-Cb/Cr ratio of 4:1, which results in half the bandwidth of YCbCr 4:4:4 format. As shown in Figure 2.6, the subsampled Cb and Cr components are co-sited and aligned with Y horizontally, but are shifted by half a line vertically.

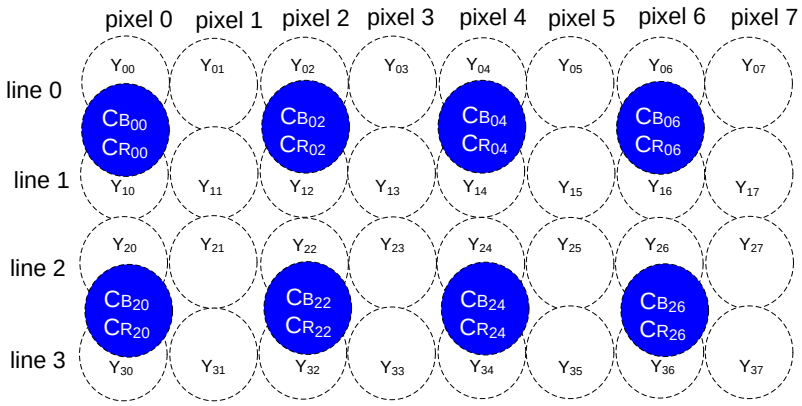


Figure 2.6. Location of Cb/Cr with Respect to Y in YCbCr 4:2:0

Figure 2.7 illustrates the organization and timing of the Y, Cb and Cr samples when transported across the HDMI link in YCbCr 4:2:0 format. Two horizontally successive Y samples are transmitted in TMDS channel 1 and 2 in order, respectively. The Cb and Cr samples are transmitted on alternate lines in TMDS channel 0, with Cb being transferred first.

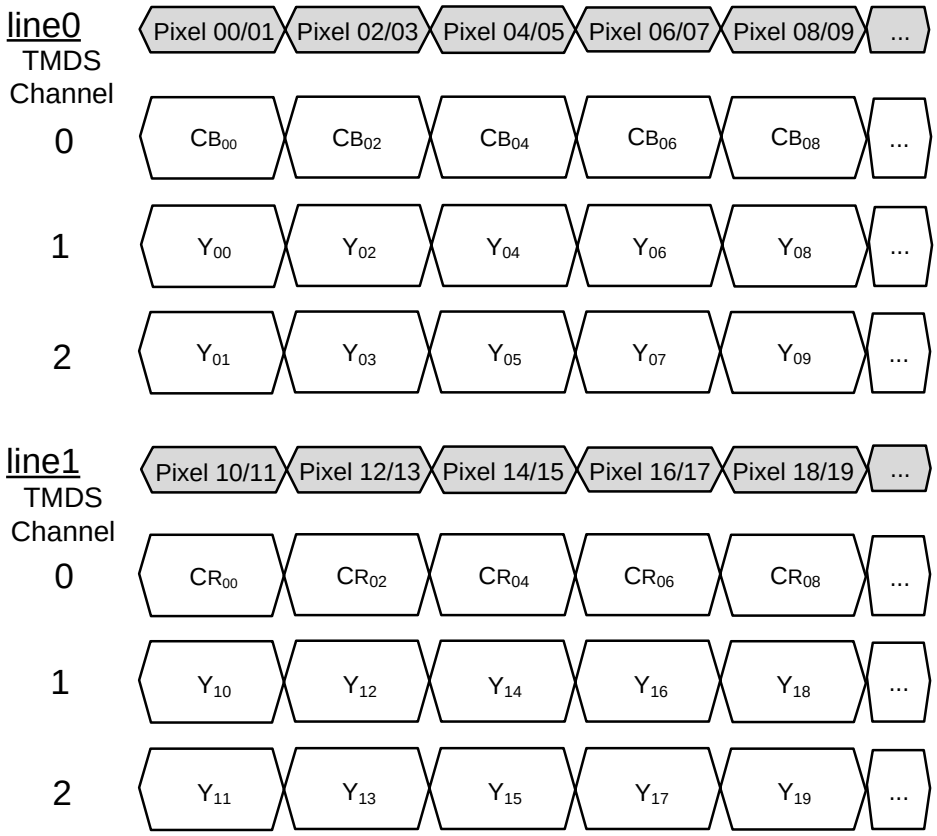


Figure 2.7. YCbCr 4:2:0 Signal Mapping and Timing Diagram

The SiI9616 video processor provides a special mode for scaling any input format with 50/60 Hz frame rate to 4K x 2K 50/60 Hz in 4:2:0 output format. In this mode, the scaler is configured to scale the input vertically to the full 4K x 2K vertical resolution of 2160 lines and horizontally to half the horizontal resolution, either 1920 or 2048 pixels. A half line vertical shift is then applied to the chroma component of the generated signal before being upsampled by a factor of two. The resultant 4:4:4 signal then goes to a luma upsampler module where the luma component is upsampled to create two times the number of samples. In the final stage, the luma component is sent out in two pixels per clock, while the chroma components Cb and Cr are clocked out on alternating lines. All processing is done with an output clock of 297 MHz.

2.15. Parallel Video Data Input

2.15.1. Common Video Input Formats

The Parallel Video Input (PVI) data capture block receives uncompressed 8- to 12-bit color depth (bits per color component) digital video.

Table 2.3 shows several common input pixel encoding schemes that the SiI9616 device supports on the parallel video input pins. A description of each format is provided in the Pixel Encoding Description section on page 24.

Table 2.3. Input Formats

Format	Syncs	Pixel Clocks					Figure Reference
		480i/576i (MHz)	480p/576p (MHz)	720p (MHz)	1080i (MHz)	1080p (MHz)	
24/30/36 bit dual clock edge YCbCr 4:4:4 or RGB (Note 4)	External	13.5	27	74	74	—	Figure 2.16 Figure 2.17
16/20/24 bit YCbCr 4:2:2	External	13.5	27	74	74	148	Figure 2.8
16/20/24 bit YCbCr 4:2:2	Embedded	13.5	27	74	74	148	Figure 2.9 Figure 2.10
8/10/12 bit YCbCr 4:2:2	External	13.5 (double clock edge) or 27	27 (double clock edge) or 54	—	—	—	Figure 2.11
8/10/12 bit YCbCr 4:2:2	Embedded	13.5 (double clock edge) or 27	27 (double clock edge) or 54	—	—	—	Figure 2.12 Figure 2.13
24/30/36 bit YCbCr 4:4:4	External	13.5, 27 (Note 3)	27	74	74	148	Figure 2.14
24/30/36 bit RGB	External	13.5, 27 (Note 3)	27	74	74	148	Figure 2.15

Notes:

1. Formats without DE are supported using the SiI9616 internal DE generator.
2. Embedded syncs must be input on the internal Y bus.
3. 27 MHz pixel clock for pixel-replicated or multiplexed 480i or 576i inputs.
4. Data is latched on both the rising and falling edges of the clock.

2.15.2. Input Connections

Table 2.4 below, and Table 2.5 and Table 2.6 on the next page show how the various video input formats should be connected. However, for ease of layout, pin and bus swapping can be used.

Table 2.4. Input Video Connections

SiI9616 Pins	Input Format									
	16-bit YCbCr 4:2:2	20-bit YCbCr 4:2:2	24-bit YCbCr 4:2:2	24-bit YCbCr 4:4:4	30-bit YCbCr 4:4:4	36-bit YCbCr 4:4:4	24-bit RGB	30-bit RGB	36-bit RGB	24/30/36 bit YCbCr 4:4:4 or RGB (Dual Edge)
PVI_DATA23	Y[7]	Y[9]	Y[11]	Y[7]	Y[9]	Y[11]	G[7]	G[9]	G[11]	Refer to Table 2.5
PVI_DATA22	Y[6]	Y[8]	Y[10]	Y[6]	Y[8]	Y[10]	G[6]	G[8]	G[10]	
PVI_DATA21	Y[5]	Y[7]	Y[9]	Y[5]	Y[7]	Y[9]	G[5]	G[7]	G[9]	
PVI_DATA20	Y[4]	Y[6]	Y[8]	Y[4]	Y[6]	Y[8]	G[4]	G[6]	G[8]	
PVI_DATA19	Y[3]	Y[5]	Y[7]	Y[3]	Y[5]	Y[7]	G[3]	G[5]	G[7]	
PVI_DATA18	Y[2]	Y[4]	Y[6]	Y[2]	Y[4]	Y[6]	G[2]	G[4]	G[6]	
PVI_DATA17	Y[1]	Y[3]	Y[5]	Y[1]	Y[3]	Y[5]	G[1]	G[3]	G[5]	
PVI_DATA16	Y[0]	Y[2]	Y[4]	Y[0]	Y[2]	Y[4]	G[0]	G[2]	G[4]	
PVI_DATA15	—	Y[1]	Y[3]	—	Y[1]	Y[3]	—	G[1]	G[3]	
PVI_DATA14	—	Y[0]	Y[2]	—	Y[0]	Y[2]	—	G[0]	G[2]	
PVI_DATA13	—	—	Y[1]	—	—	Y[1]	—	—	G[1]	
PVI_DATA12	—	—	Y[0]	—	—	Y[0]	—	—	G[0]	
PVI_DATA11	C[7]	C[9]	C[11]	CB[7]	CB[9]	CB[11]	B[7]	B[9]	B[11]	
PVI_DATA10	C[6]	C[8]	C[10]	CB[6]	CB[8]	CB[10]	B[6]	B[8]	B[10]	
PVI_DATA9	C[5]	C[7]	C[9]	CB[5]	CB[7]	CB[9]	B[5]	B[7]	B[9]	
PVI_DATA8	C[4]	C[6]	C[8]	CB[4]	CB[6]	CB[8]	B[4]	B[6]	B[8]	
PVI_DATA7	C[3]	C[5]	C[7]	CB[3]	CB[5]	CB[7]	B[3]	B[5]	B[7]	
PVI_DATA6	C[2]	C[4]	C[6]	CB[2]	CB[4]	CB[6]	B[2]	B[4]	B[6]	
PVI_DATA5	C[1]	C[3]	C[5]	CB[1]	CB[3]	CB[5]	B[1]	B[3]	B[5]	
PVI_DATA4	C[0]	C[2]	C[4]	CB[0]	CB[2]	CB[4]	B[0]	B[2]	B[4]	
PVI_DATA3	—	C[1]	C[3]	—	CB[1]	CB[3]	—	B[1]	B[3]	
PVI_DATA2	—	C[0]	C[2]	—	CB[0]	CB[2]	—	B[0]	B[2]	
PVI_DATA1	—	—	C[1]	—	—	CB[1]	—	—	B[1]	
PVI_DATA0	—	—	C[0]	—	—	CB[0]	—	—	B[0]	
PVI_DATA35	—	—	—	CR[7]	CR[9]	CR[11]	R[7]	R[9]	R[11]	
PVI_DATA34	—	—	—	CR[6]	CR[8]	CR[10]	R[6]	R[8]	R[10]	
PVI_DATA33	—	—	—	CR[5]	CR[7]	CR[9]	R[5]	R[7]	R[9]	
PVI_DATA32	—	—	—	CR[4]	CR[6]	CR[8]	R[4]	R[6]	R[8]	
PVI_DATA31	—	—	—	CR[3]	CR[5]	CR[7]	R[3]	R[5]	R[7]	
PVI_DATA30	—	—	—	CR[2]	CR[4]	CR[6]	R[2]	R[4]	R[6]	
PVI_DATA29	—	—	—	CR[1]	CR[3]	CR[5]	R[1]	R[3]	R[5]	
PVI_DATA28	—	—	—	CR[0]	CR[2]	CR[4]	R[0]	R[2]	R[4]	
PVI_DATA27	—	—	—	—	CR[1]	CR[3]	—	R[1]	R[3]	
PVI_DATA26	—	—	—	—	CR[0]	CR[2]	—	R[0]	R[2]	
PVI_DATA25	—	—	—	—	—	CR[1]	—	—	R[1]	
PVI_DATA24	—	—	—	—	—	CR[0]	—	—	R[0]	

Table 2.5. Dual Clock Edge RGB and YCbCr 4:4:4 Formats Input Connections

Pin Name	24-bit				30-bit				36-bit			
	RGB		YCbCr		RGB		YCbCr		RGB		YCbCr	
	1st Edge	2nd Edge	1st Edge	2nd Edge	1st Edge	2nd Edge	1st Edge	2nd Edge	1st Edge	2nd Edge	1st Edge	2nd Edge
PVI_DATA0	—	—	—	—	—	—	—	—	B0	G6	Cb0	Y6
PVI_DATA1	—	—	—	—	—	—	—	—	B1	G7	Cb1	Y7
PVI_DATA2	—	—	—	—	—	—	—	—	B2	G8	Cb2	Y8
PVI_DATA3	—	—	—	—	B0	G5	Cb0	Y5	B3	G9	Cb3	Y9
PVI_DATA4	—	—	—	—	B1	G6	Cb1	Y6	B4	G10	Cb4	Y10
PVI_DATA5	—	—	—	—	B2	G7	Cb2	Y7	B5	G11	Cb5	Y11
PVI_DATA6	B0	G4	Cb0	Y4	B3	G8	Cb3	Y8	B6	R0	Cb6	Cr0
PVI_DATA7	B1	G5	Cb1	Y5	B4	G9	Cb4	Y9	B7	R1	Cb7	Cr1
PVI_DATA8	B2	G6	Cb2	Y6	B5	R0	Cb5	Cr0	B8	R2	Cb8	Cr2
PVI_DATA9	B3	G7	Cb3	Y7	B6	R1	Cb6	Cr1	B9	R3	Cb9	Cr3
PVI_DATA10	B4	R0	Cb4	Cr0	B7	R2	Cb7	Cr2	B10	R4	Cb10	Cr4
PVI_DATA11	B5	R1	Cb5	Cr1	B8	R3	Cb8	Cr3	B11	R5	Cb11	Cr5
PVI_DATA12	B6	R2	Cb6	Cr2	B9	R4	Cb9	Cr4	G0	R6	Y0	Cr6
PVI_DATA13	B7	R3	Cb7	Cr3	G0	R5	Y0	Cr5	G1	R7	Y1	Cr7
PVI_DATA14	G0	R4	Y0	Cr4	G1	R6	Y1	Cr6	G2	R8	Y2	Cr8
PVI_DATA15	G1	R5	Y1	Cr5	G2	R7	Y2	Cr7	G3	R9	Y3	Cr9
PVI_DATA16	G2	R6	Y2	Cr6	G3	R8	Y3	Cr8	G4	R10	Y4	Cr10
PVI_DATA17	G3	R7	Y3	Cr7	G4	R9	Y4	Cr9	G5	R11	Y5	Cr11
PVI_HSYNC	HSync	HSync	HSync	HSync	HSync	HSync	HSync	HSync	HSync	HSync	HSync	HSync
PVI_VSYNC	VSync	VSync	VSync	VSync	VSync	VSync	VSync	VSync	VSync	VSync	VSync	VSync
PVI_DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE

Note: Bit reversal (changing the pin mapping from 11:0 to 0:11) is supported in this mode; however, the input channels cannot be swapped. For example, the Y input bus cannot be mapped to the internal Cb bus.

Table 2.6. Multiplexed YCbCr 4:2:2 Formats Input Connections

Pin Name	8-bit	10-bit	12-bit
PVI_DATA23	Y[7]/C[7]	Y[9]/C[9]	Y[11]/C[11]
PVI_DATA22	Y[6]/C[6]	Y[8]/C[8]	Y[10]/ C[10]
PVI_DATA21	Y[5]/C[5]	Y[7]/C[7]	Y[9]/C[9]
PVI_DATA20	Y[4]/C[4]	Y[6]/C[6]	Y[8]/C[8]
PVI_DATA19	Y[3]/C[3]	Y[5]/C[5]	Y[7]/C[7]
PVI_DATA18	Y[2]/C[2]	Y[4]/C[4]	Y[6]/C[6]
PVI_DATA17	Y[1]/C[1]	Y[3]/C[3]	Y[5]/C[5]
PVI_DATA16	Y[0]/C[0]	Y[2]/C[2]	Y[4]/C[4]
PVI_DATA15	—	Y[1]/C[1]	Y[3]/C[3]
PVI_DATA14	—	Y[0]/C[0]	Y[2]/C[2]
PVI_DATA13	—	—	Y[1]/C[1]
PVI_DATA12	—	—	Y[0]/C[0]

2.15.3. Pixel Encoding Description

2.15.3.1. YCbCr 4:2:2 with External Syncs

Figure 2.8 shows the input waveforms for separate Y and C with horizontal sync, vertical sync, and data enable inputs. Data is sampled on the rising edge of the input clock. The combined bus width for Y and C can be 16, 20, or 24 bits.

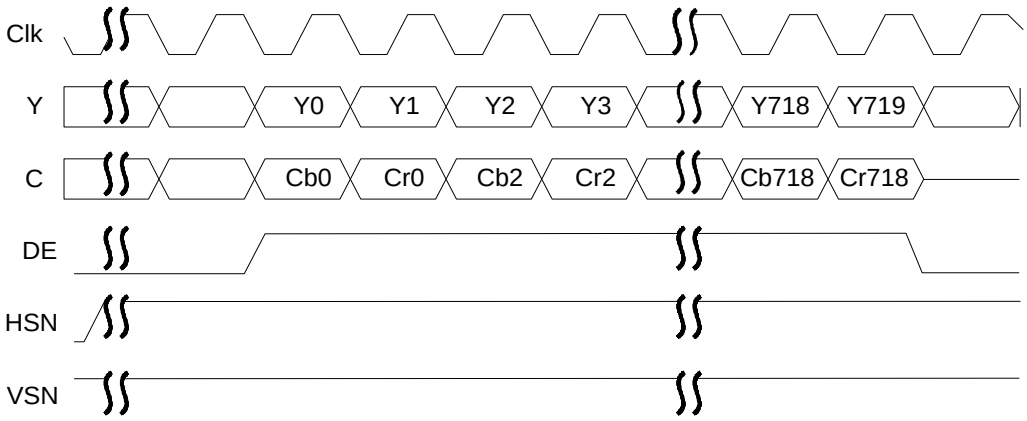


Figure 2.8. Inputs Description of YCbCr 4:2:2 with External Syncs

2.15.3.2. YCbCr 4:2:2 with Embedded Syncs

Figure 2.9 and Figure 2.10 show the input waveforms for the input format that features separate Y and C inputs with embedded syncs. Figure 2.9 shows the Start Active Video (SAV) code for 10-bit inputs on the Y input followed by the input video data. Figure 2.10 shows the input video data followed by the End Active Video (EAV) code for 10-bit inputs. For 8-bit inputs, the two least significant bits of the SAV and EAV should be dropped. In the figures below, the data is sampled on the rising edge of the clock. The clock rate is 27 MHz. Refer to the ITU.656 Specification for more detailed information regarding the format of the embedded syncs.

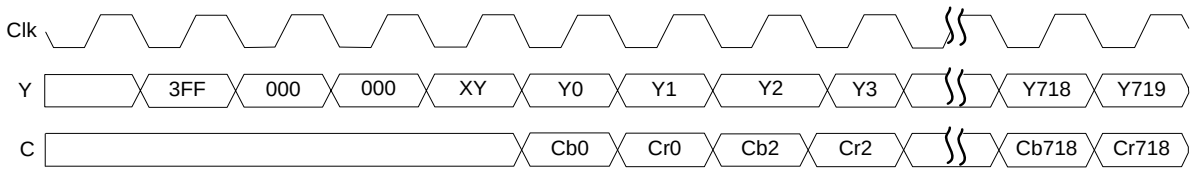


Figure 2.9. Input Description of YCbCr 4:2:2 with Embedded Syncs, SAV

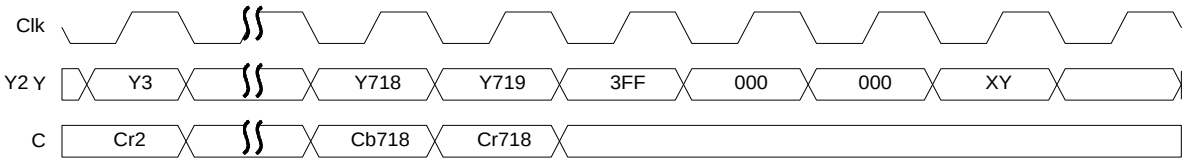


Figure 2.10. Input Description of YCbCr 4:2:2 with Embedded Syncs, EAV

The format can also be input using both clock edges.

2.15.3.3. Multiplexed YCbCr 4:2:2 with External Syncs (27 MHz or 54 MHz)

Figure 2.11 shows the input waveform for the input format that features multiplexed Y and C inputs and separate vertical sync, horizontal sync, and data enable.

If the input resolution is 480p or 576p, the clock runs at 54 MHz and the data is sampled on the rising edge of the clock. Alternatively, the clock can run at 27 MHz and the device can be programmed to read data on both the rising and falling edges of the clock.

If the input resolution is 480i or 576i, the clock runs at 27 MHz and the data is sampled on the rising edge of the clock. If the input clock is 13.5 MHz, the device should be configured to read data on both the rising and falling edges of the clock.

For 12-bit multiplexed YCbCr data, use the Y(11:0) inputs. For 10-bit multiplexed YCbCr data, use the Y(11:2) inputs. For 8-bit multiplexed YCbCr data, use the Y(11:4) inputs.

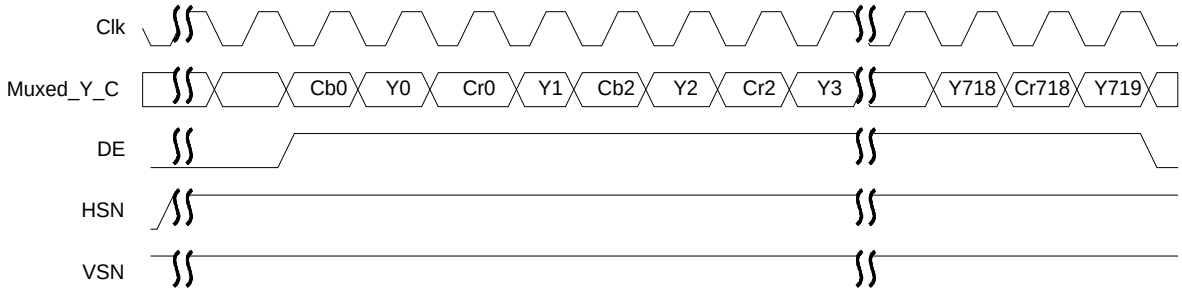


Figure 2.11. Input Description of Multiplexed YCbCr 4:2:2 with External Syncs (27 MHz or 54 MHz)

2.15.3.4. Multiplexed YCbCr 4:2:2 with Embedded Syncs

Figure 2.12 and Figure 2.13 show the input waveforms for the input format that features multiplexed Y and C inputs along with embedded syncs.

If the input resolution is 480p or 576p, the clock runs at 54 MHz and the data is sampled on the rising edge of the clock. Alternatively, the clock can run at 27 MHz and the device can be programmed to read data on both the rising and falling edges of the clock.

If the input resolution is 480i or 576i, the clock runs at 27 MHz and the data is sampled on the rising edge of the clock.

High-definition resolutions are also supported. However, 1080p inputs must be clocked-in using both the rising and falling edges.

Figure 2.12 shows the Start Active Video (SAV) code followed by the video data. Figure 2.13 shows active data followed by the End Active Video (EAV) code. For 12-bit multiplexed YCbCr data, use the Y (11:0) inputs. For 10-bit multiplexed YCbCr data, use the Y (11:2) inputs. For 8-bit multiplexed YCbCr data, use the Y (11:4) inputs. Refer to the ITU.656 Specification for more detailed information about this format.

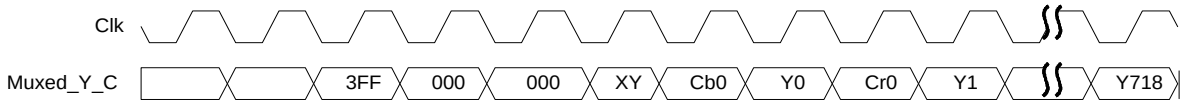


Figure 2.12. Input Description of Multiplexed YCbCr 4:2:2 with Embedded Syncs, SAV

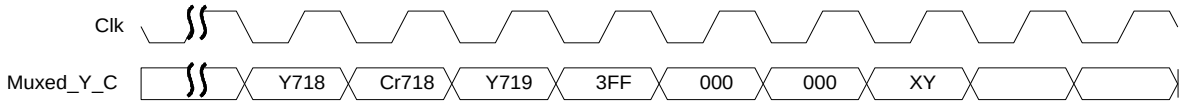


Figure 2.13. Input Description of Multiplexed YCbCr 4:2:2 with Embedded Syncs, EAV

2.15.3.5. YCbCr 4:4:4

Figure 2.14 shows the input waveforms for the 24-, 30-, or 36-bit YCbCr 4:4:4 format. This input format requires external VSYNC and HSYNC. A DE can be generated using the SiI9616 internal DE generator.

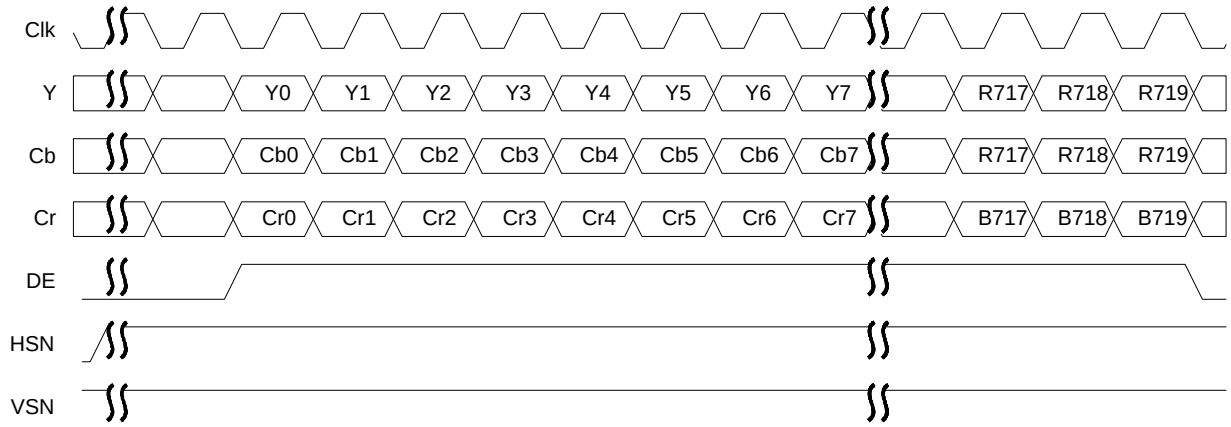


Figure 2.14. Input Description for YCbCr 4:4:4

2.15.3.6. RGB

Figure 2.15 shows the input waveforms for the 24, 30, or 36 bit or RGB input format. This input format requires external VSYNC and HSYNC. A DE can be generated using the SiI9616 internal DE generator.

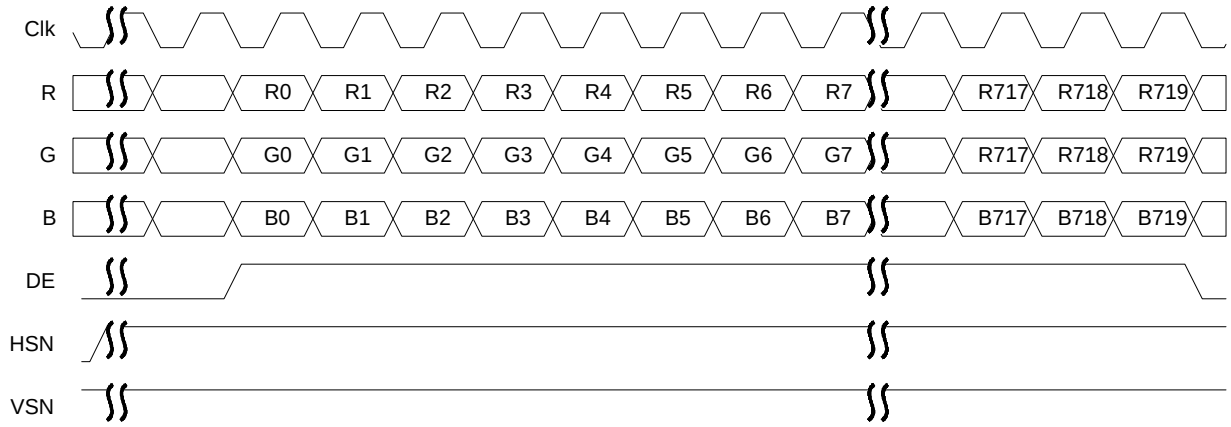


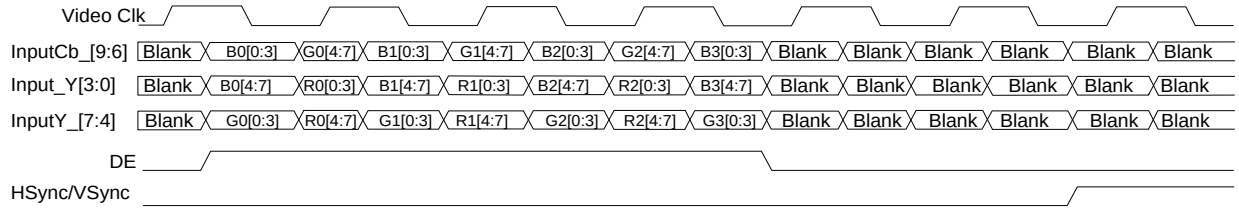
Figure 2.15. Input Description of RGB

2.15.3.7. Dual Edge Clock RGB and YCbCr 4:4:4 Formats with External Syncs

This format requires that the data be clocked-in on both edges of the input video clock. The video input clock must run at its typical rate for the resolution. For example, for 480p inputs, the video input clock must be 27 MHz. Because this format requires external syncs, the SiI9616 internal DE generator can be used if an external DE is not available.

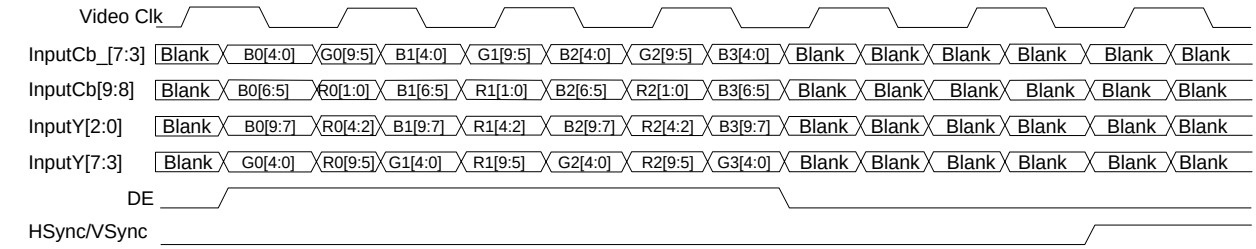
Bit reversal (changing the input pin mapping from 11:0 to 0:11) is permitted; however, in this mode, the external inputs cannot be mapped to different internal inputs. For example, the Y input bus cannot be mapped to the internal Cb bus.

Figure 2.16 and Figure 2.17 show two examples of waveforms illustrating the 24- and 30-bit versions of this format. Other waveforms are possible and are listed in Table 2.5 on page 23.



*The polarity for the video clock shown above can be reversed.

Figure 2.16. 24-bit RGB Format with External Syncs



*The polarity for the video clock shown above can be reversed.

Figure 2.17. 30-bit RGB Format with External Syncs

2.16. Parallel Video Data Output

The Parallel Video Output (PVO) block of the SiI9616 video processor can output a video stream in one of many different formats. Table 2.7 shows a list of common supported video formats.

Not all formats in Table 2.7 can be supported when both the PVO and HDMI output are connected in the system. See the Output Connections section on the next page for details.

Table 2.7. Output Formats

Bit Depth	Encoding	Resolutions Supported	Color Space	Syncs	Clock Rate MHz
8/10/12	Multiplexed 4:2:2 YCbCr	480i, 576i	BT.601	Separate or Embedded	27
8/10/12	Multiplexed 4:2:2 YCbCr	480p, 576p	BT.601	Separate or Embedded	54
16/20/24	4:2:2 YCbCr	480i, 576i	BT.601	Separate	13.5
16/20/24	4:2:2 YCbCr	480p, 576p	BT.601	Separate	27
16/20/24	4:2:2 YCbCr	720p, 1080i	BT.709	Separate	74
16/20/24	4:2:2 YCbCr	1080p	BT.709	Separate	148
24/30/36	4:4:4 YCbCr	480p, 576p	BT.601	Separate	27
24/30/36	4:4:4 YCbCr	720p, 1080i	BT.709	Separate	74
24/30/36	4:4:4 YCbCr	1080p	BT.709	Separate	148
24/30/36	RGB	480p, 576p	—	Separate	27
24/30/36	RGB	720p, 1080i	—	Separate	74
24/30/36	RGB	1080p	—	Separate	148
24/30/36	RGB	VGA, SVGA, XGA, SXGA, UXGA	—	Separate	< 162

2.16.1. Output Connections

The parallel video output is a 36-bit data bus that can be programmed to support multiple RGB, YCbCr 4:4:4 and YCbCr 4:2:2 bus formats, as shown in Table 2.7. Not all of these output formats can be selected if the system supports both the PVO and HDMI output at the same time.

2.16.1.1. Supported Output Formats and Signal Connections when HDMI Output is Not Connected

Figure 2.18 shows a system where only the PVO output is enabled while the HDMI output is disabled.

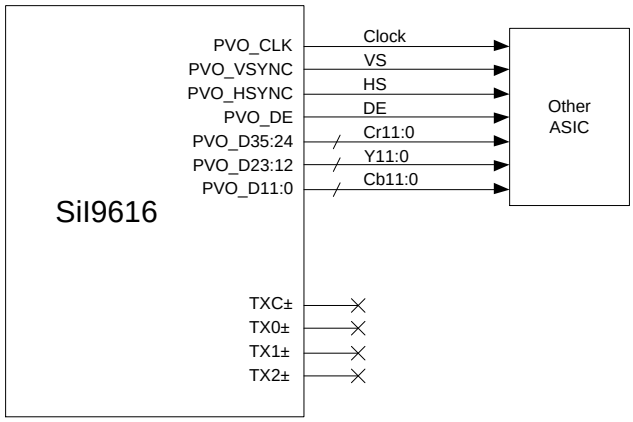


Figure 2.18. SiI9616 Video Processor with PVO Enabled and HDMI Output Not Connected

In this output configuration, all 36 bits of the PVO data bus are available to transmit the video data and all output formats are supported. Table 2.8 on the next page shows the signal connections available on the PVO in this case.

Table 2.8. PVO Signal Connections when HDMI Output is Not Connected

Sil9616 Pins	Output Format											
	8-bit YCbCr 4:2:2	10-bit YCbCr 4:2:2	12-bit YCbCr 4:2:2	16-bit YCbr 4:2:2	20-bit YCbr 4:2:2	24-bit YCbr 4:2:2	24-bit YCbr 4:4:4	30-bit YCbr 4:4:4	36-bit YCbr 4:4:4	24-bit RGB	30-bit RGB	36-bit RGB
PVO_DATA23	Y[7]/C[7]	Y[9]/C[9]	Y[11]/C[11]	Y[7]	Y[9]	Y[11]	Y[7]	Y[9]	Y[11]	G[7]	G[9]	G[11]
PVO_DATA22	Y[6]/C[6]	Y[8]/C[8]	Y[10]/C[10]	Y[6]	Y[8]	Y[10]	Y[6]	Y[8]	Y[10]	G[6]	G[8]	G[10]
PVO_DATA21	Y[5]/C[5]	Y[7]/C[7]	Y[9]/C[9]	Y[5]	Y[7]	Y[9]	Y[5]	Y[7]	Y[9]	G[5]	G[7]	G[9]
PVO_DATA20	Y[4]/C[4]	Y[6]/C[6]	Y[8]/C[8]	Y[4]	Y[6]	Y[8]	Y[4]	Y[6]	Y[8]	G[4]	G[6]	G[8]
PVO_DATA19	Y[3]/C[3]	Y[5]/C[5]	Y[7]/C[7]	Y[3]	Y[5]	Y[7]	Y[3]	Y[5]	Y[7]	G[3]	G[5]	G[7]
PVO_DATA18	Y[2]/C[2]	Y[4]/C[4]	Y[6]/C[6]	Y[2]	Y[4]	Y[6]	Y[2]	Y[4]	Y[6]	G[2]	G[4]	G[6]
PVO_DATA17	Y[1]/C[1]	Y[3]/C[3]	Y[5]/C[5]	Y[1]	Y[3]	Y[5]	Y[1]	Y[3]	Y[5]	G[1]	G[3]	G[5]
PVO_DATA16	Y[0]/C[0]	Y[2]/C[2]	Y[4]/C[4]	Y[0]	Y[2]	Y[4]	Y[0]	Y[2]	Y[4]	G[0]	G[2]	G[4]
PVO_DATA15	—	Y[1]/C[1]	Y[3]/C[3]	—	Y[1]	Y[3]	—	Y[1]	Y[3]	—	G[1]	G[3]
PVO_DATA14	—	Y[0]/C[0]	Y[2]/C[2]	—	Y[0]	Y[2]	—	Y[0]	Y[2]	—	G[0]	G[2]
PVO_DATA13	—	—	Y[1]/C[1]	—	—	Y[1]	—	—	Y[1]	—	—	G[1]
PVO_DATA12	—	—	Y[0]/C[0]	—	—	Y[0]	—	—	Y[0]	—	—	G[0]
PVO_DATA11	—	—	—	—	—	—	CB[7]	CB[9]	CB[11]	B[7]	B[9]	B[11]
PVO_DATA10	—	—	—	—	—	—	CB[6]	CB[8]	CB[10]	B[6]	B[8]	B[10]
PVO_DATA9	—	—	—	—	—	—	CB[5]	CB[7]	CB[9]	B[5]	B[7]	B[9]
PVO_DATA8	—	—	—	—	—	—	CB[4]	CB[6]	CB[8]	B[4]	B[6]	B[8]
PVO_DATA7	—	—	—	—	—	—	CB[3]	CB[5]	CB[7]	B[3]	B[5]	B[7]
PVO_DATA6	—	—	—	—	—	—	CB[2]	CB[4]	CB[6]	B[2]	B[4]	B[6]
PVO_DATA5	—	—	—	—	—	—	CB[1]	CB[3]	CB[5]	B[1]	B[3]	B[5]
PVO_DATA4	—	—	—	—	—	—	CB[0]	CB[2]	CB[4]	B[0]	B[2]	B[4]
PVO_DATA3	—	—	—	—	—	—	—	CB[1]	CB[3]	—	B[1]	B[3]
PVO_DATA2	—	—	—	—	—	—	—	CB[0]	CB[2]	—	B[0]	B[2]
PVO_DATA1	—	—	—	—	—	—	—	—	CB[1]	—	—	B[1]
PVO_DATA0	—	—	—	—	—	—	—	—	CB[0]	—	—	B[0]
PVO_DATA35	—	—	—	C[7]	C[9]	C[11]	CR[7]	CR[9]	CR[11]	R[7]	R[9]	R[11]
PVO_DATA34	—	—	—	C[6]	C[8]	C[10]	CR[6]	CR[8]	CR[10]	R[6]	R[8]	R[10]
PVO_DATA33	—	—	—	C[5]	C[7]	C[9]	CR[5]	CR[7]	CR[9]	R[5]	R[7]	R[9]
PVO_DATA32	—	—	—	C[4]	C[6]	C[8]	CR[4]	CR[6]	CR[8]	R[4]	R[6]	R[8]
PVO_DATA31	—	—	—	C[3]	C[5]	C[7]	CR[3]	CR[5]	CR[7]	R[3]	R[5]	R[7]
PVO_DATA30	—	—	—	C[2]	C[4]	C[6]	CR[2]	CR[4]	CR[6]	R[2]	R[4]	R[6]
PVO_DATA29	—	—	—	C[1]	C[3]	C[5]	CR[1]	CR[3]	CR[5]	R[1]	R[3]	R[5]
PVO_DATA28	—	—	—	C[0]	C[2]	C[4]	CR[0]	CR[2]	CR[4]	R[0]	R[2]	R[4]
PVO_DATA27	—	—	—	—	C[1]	C[3]	—	CR[1]	CR[3]	—	R[1]	R[3]
PVO_DATA26	—	—	—	—	C[0]	C[2]	—	CR[0]	CR[2]	—	R[0]	R[2]
PVO_DATA25	—	—	—	—	—	C[1]	—	—	CR[1]	—	—	R[1]
PVO_DATA24	—	—	—	—	—	C[0]	—	—	CR[0]	—	—	R[0]

2.16.1.2. Supported Output Formats and Signal Connections when HDMI Output is Connected

In a system where both the PVO and HDMI output of the Sil9616 video processor are enabled at the same time, the only supported bus formats on the PVO are the following:

- 16/20-bit YCbCr4:2:2
- 8/10-bit Multiplexed YCbCr 4:2:2

Figure 2.19 shows an example of a SiI9616 video processor in which both its PVO and HDMI output are wired to transmit video. The PVO is programmed for 20-bit YCbCr 4:2:2 format in this example.

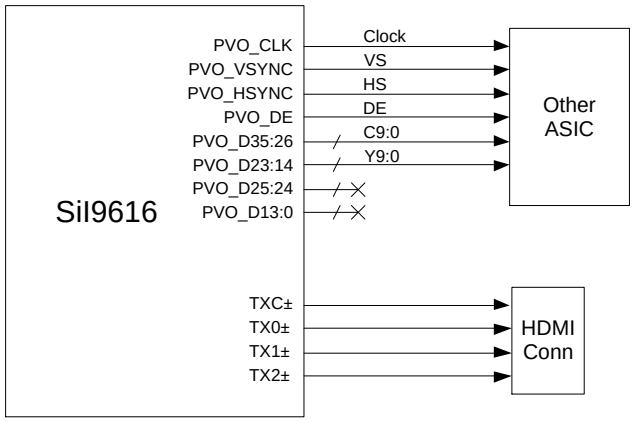


Figure 2.19. SiI9616 Video Processor with PVO and HDMI Output Connected

Table 2.9 shows the signal connections that are supported on the PVO when the HDMI output is connected. If needed, the multicolor space converter and chroma subsampler modules in the PVO data path can be used to convert any input format to the YCbCr 4:2:2 format while the Output Rate Converter module can be used to multiplex the Y and C data onto a single channel.

Table 2.9. PVO Signal Connections when HDMI Output is Connected

SiI9616 Pins	Output Format			
	8-bit YCbCr 4:2:2	10-bit YCbCr 4:2:2	16-bit YCbCr 4:2:2	20-bit YCbCr 4:2:2
PVO_DATA23	Y[7]/C[7]	Y[9]/C[9]	Y[7]	Y[9]
PVO_DATA22	Y[6]/C[6]	Y[8]/C[8]	Y[6]	Y[8]
PVO_DATA21	Y[5]/C[5]	Y[7]/C[7]	Y[5]	Y[7]
PVO_DATA20	Y[4]/C[4]	Y[6]/C[6]	Y[4]	Y[6]
PVO_DATA19	Y[3]/C[3]	Y[5]/C[5]	Y[3]	Y[5]
PVO_DATA18	Y[2]/C[2]	Y[4]/C[4]	Y[2]	Y[4]
PVO_DATA17	Y[1]/C[1]	Y[3]/C[3]	Y[1]	Y[3]
PVO_DATA16	Y[0]/C[0]	Y[2]/C[2]	Y[0]	Y[2]
PVO_DATA15	—	Y[1]/C[1]	—	Y[1]
PVO_DATA14	—	Y[0]/C[0]	—	Y[0]
PVO_DATA35	—	—	C[7]	C[9]
PVO_DATA34	—	—	C[6]	C[8]
PVO_DATA33	—	—	C[5]	C[7]
PVO_DATA32	—	—	C[4]	C[6]
PVO_DATA31	—	—	C[3]	C[5]
PVO_DATA30	—	—	C[2]	C[4]
PVO_DATA29	—	—	C[1]	C[3]
PVO_DATA28	—	—	C[0]	C[2]
PVO_DATA27	—	—	—	C[1]
PVO_DATA26	—	—	—	C[0]

2.16.2. Output Pin Configuration

The PVO pins can be reconfigured in a number of ways by register programming. Each of the three output pin groups (Y/G, Cb/B, and Cr/R) can be disabled independently. All pins can be disabled at once or only the 2, 4, or 6 least significant bits. The output clock and sync signals, including DE, can also be disabled individually. Disabling unused/unconnected pins ensures that they do not toggle unnecessarily. The polarity of the output clock, VSYNC, HSYNC, and DE signals can be inverted.

2.16.3. PVO Clock Duty Cycle

The parallel video output clock has a number of different duty cycles depending on where it is sourced from.

The duty cycle of the PVO clock is nominally 50% when generated from the video PLLs, either in independent mode or in cascaded mode.

When the PVO clock is sourced from the HDMI receiver, its duty cycle is determined by the zone the PLL of the HDMI receiver is operating in and the color depth of the input video. The PLL has three operating zones – 1x, 2x and 4x. The PLL zone is automatically selected by the receiver for the current link frequency. Table 2.10 below shows the PVO clock duty cycle for different receiver PLL zones and input color depths.

If the PVI clock is selected as the source for the PVO clock, the duty cycle of the PVO clock is the same as the input clock.

From Table 2.10, the duty cycle of the PVO clock is not always 50% when it comes from the HDMI receiver. If a clock with a 50% duty cycle is desired, the clock can be sent to one of the video PLLs, which then generates a clock signal of the same frequency but with 50% duty cycle.

Table 2.10. PVO Clock Duty Cycle Specifications

Clock Source	PLL Zone	Deep Color Mode	Duty Cycle[1] (nominal)
Video PLL0/1	Not Applicable	Not Applicable	50%
HDMI Receiver	1x (< 38 MHz)[2]	8-bit	50%
		10-bit	60%
		12-bit	66.67%
	2x (35 MHz to 82 MHz)[2]	8-bit	75%
		10-bit	50%
		12-bit	50%
	4x (> 74 MHz)[2]	8-bit	87.5%
		10-bit	50%
		12-bit	50%
PVI	Not Applicable	Not Applicable	Same as input clock

Notes:
1. The duty cycle is the percentage of time the clock signal is High in one clock period.
2. Typical operating range of link frequency for given zone. Note the frequency overlap between zones.

2.17. HDMI Output

The SiI9616 video processor features an HDMI transmitter with 300 MHz TMDS core for 1080p 60 Hz 3D and 4K x 2K outputs, full digital video and audio pipelines, integrated HDCP keys and encryption engine, and Audio Return Channel (ARC) input.

2.17.1. TMDS Transmitter Core

The TMDS transmitter core performs 8-bit to 10-bit TMDS encoding on the data received from the HDCP XOR mask and is then sent over three TMDS data and one TMDS clock differential lines. See the HDCP Encryption Engine/XOR Mask section on the next page for more details. The transmitter core supports link clocks from 25 MHz to 300 MHz. The internal PLL has the option to multiply the pixel clock to implement deep color or pixel repetition modes.

2.17.2. Deep Color Support

The SiI9616 video processor provides support for deep color video data up to the maximum specified link speed of 3 Gb/s (300 MHz internal clock rate for the deep color packetized data). It supports 30-bit and 36-bit video input formats, and converts the data to 8-bit packets for encryption and encoding for transferring across the TMDS link.

When the input data width is wider than desired, the device can be programmed to dither or truncate the video data to the desired size. For example, if the input data width is a 12 bits per pixel component, but the sink device only supports 10 bits, the HDMI transmitter can be programmed to dither or truncate the 12-bit input data to the desired 10-bit output data.

2.17.3. Source Termination

TMDS transmitters use a current source to develop the low-voltage differential signal at the receiver end of the DC-coupled TMDS transmission line, and constitute open termination for reflected waveforms. As a result, signal reflections created by traces, packaging, connectors, and the cable can arrive at the transmitter with increased amplitude. To reduce these reflections, the HDMI transmitter port has an internal termination option of 150 Ω for single-ended termination, and 300 Ω for differential termination. This termination reduces the amplitude of the reflected signal, but it also lowers the common mode input voltage at the sink. Lattice Semiconductor recommends turning internal source termination off when the transmitter operates less than or equal to 165 MHz, and turning it on for frequencies above 165 MHz.

2.17.4. HDCP Encryption Engine/XOR Mask

The HDMI transmitter provides an HDCP encryption engine that contains the logic necessary to encrypt the incoming audio and video data, and includes support for HDCP authentication and repeater checks. The system microcontroller controls the encryption process by using a set sequence of register reads and writes. An algorithm uses HDCP keys and a Key Selection Vector (KSV), stored in the HDCP key, ROM to calculate a number that is then applied to an XOR mask. This process encrypts the audio and video data on a pixel-by-pixel basis during each clock cycle.

2.17.5. HDCP Key ROM

The SiI9616 video processor comes preprogrammed with a set of production HDCP keys for the HDMI transmitter. The keys are stored in an internal ROM. System manufacturers do not need to purchase key sets from the Digital Content Protection LLC. Lattice Semiconductor handles all purchasing, programming, and security for the HDCP keys. The preprogrammed HDCP keys provide the highest level of security because there is no way to read the keys once the device is programmed.

Customers must sign the HDCP license agreement (www.digital-cp.com) or be under a specific NDA with Lattice Semiconductor before receiving SiI9616 samples.

2.17.6. Audio Return Channel

The SiI9616 video processor provides an Audio Return Channel (ARC) input to receive an IEC60958-1 or IEC61937 audio stream from the connected sink device through the utility pin of the HDMI cable.

The SiI9616 device supports only single mode ARC. The SiI9616 ARC input can be made compatible for common mode ARC by using an AC-coupling network between the HPD and utility pins of the HDMI connector of the HDMI output port and the SiI9616 ARC pin.

2.17.7. DDC Master I^2C Interface

The SiI9616 HDMI transmitter includes a DDC master I^2C interface for direct connection to the HDMI cable. The DDC master I^2C interface is used for two purposes:

- To read the EDID of the connected downstream device,
- To perform HDCP authentication of the connected downstream device.

The host uses the DDC master logic to read the EDID by programming the target address, offset, and number of bytes. When completed, or when the DDC master FIFO becomes full, an interrupt signal is sent to the host so that the host can read data out of the FIFO.

The TPI hardware uses the DDC master to carry out HDCP authentication tasks. The request to perform HDCP authentication is initiated by the host, but it does not access the DDC master directly.

2.17.8. Receiver Sense and Hot Plug Detection

The HDMI transmitter can detect a connected device through the Hot Plug Detect (HPD) input signal or the internal Receiver Sense (RSEN) logic. When HIGH, the HPD signal indicates to the transmitter that the EDID of the connected receiver is readable. The RSEN can be used to detect whether the attached device is powered by sensing the termination in the attached device. An interrupt can be generated whenever there is a change in the state of the HPD or RSEN signal.

2.17.9. Interrupts

The Interrupt logic in the HDMI transmitter buffers interrupt events from different sources. Receiver Sense and Hot Plug Interrupts are also available in power-down mode. The logic for handling these interrupts when all clocks are disabled is also part of this block. The INT pin provides an interrupt signal to the system microcontroller when any of the following occur:

- Monitor Detect (either from the HPD input level or from the receiver sense feature) changes
- VSYNC (useful for synchronizing a microcontroller to the vertical timing interval)
- Error in the audio format
- DDC FIFO status change
- HDCP authentication error

2.18. HDMI Input

The SiI9616 video processor integrates an HDMI receiver that accepts 300 MHz inputs such as 1080p 60 Hz 3D and 4K x 2K video formats. It offers a full video and audio processing pipeline, integrated HDCP keys, and a decryption engine. MHL mode is available with support for PackedPixel mode.

2.18.1. TMDS Receiver Core

The HDMI receiver core is the latest generation core and can receive TMDS data up to 300 MHz. The core performs

10- to 8-bit TMDS decoding on the video data, and 10- to 4-bit TMDS decoding on the audio data received from the three TMDS differential data lines, along with a TMDS differential clock. The TMDS core can sense a stopped clock or stopped video and software can put the video processor into power-down mode.

Adaptive equalization is applied to the input signal to counter high-frequency attenuation resulting from long cables, thus ensuring reliable data recovery.

The receiver core operates in either HDMI or MHL mode. In MHL mode, the receiver core de-multiplexes a single TMDS data channel into its three component logical channels (two for PackedPixel mode) of 8 bits each, using a common mode clock signal carried on the same TMDS channel.

2.18.2. Deep Color Support

The SiI9616 video processor detects deep color packets in the HDMI data stream and automatically decodes the proper pixel clock setting and output bus width. The deep color mode can be read from registers as 24-bits, 30-bits, or 36-bits per pixel, up to 1080p 60 Hz. An interrupt can be generated whenever the deep color mode changes.

2.18.3. MHL Receiver

The HDMI input of the SiI9616 video processor can be configured as a Mobile High-definition Link (MHL) receiver. When an MHL source is connected, an MHL cable detect sense signal from the cable is asserted and sent to the SiI9616 device, and also to the host microcontroller as an interrupt to configure the receiver port as an MHL port, and to prepare for the CBUS discovery process.

The MHL receiver supports PackedPixel mode, which encodes YCbCr 4:2:2 pixel data using 16 bits per pixel rather than 24 bits per pixel as in the other pixel encoding modes. The incoming pixel clock rate may be as high as 150 MHz in this

mode, with a link clock rate of half of the pixel clock, which allows MHL to support 1080p 60 Hz video. The maximum link clock rate remains 75 MHz in PackedPixel mode.

2.18.4. HDCP Decryption Engine/XOR Mask

The HDMI receiver provides an HDCP decryption engine to decrypt protected audio and video data transmitted by the source device. Decryption is enabled only after the successful completion of an authentication protocol between the source device and the HDMI receiver. This process is driven by the source device through a set sequence of read and writes through the DDC channel. A resulting calculated value is applied to an XOR mask during each clock cycle to decrypt the audio-visual data.

The HDMI receiver also contains all the necessary logic to support full HDCP repeaters. The KSV FIFO can store a KSV list consisting of up to 16 devices.

2.18.5. HDCP Embedded Keys

The SiI9616 device is preprogrammed with a set of production HDCP keys for the HDMI receiver. The keys are stored on the chip in non-volatile memory. Lattice Semiconductor handles all purchasing, programming, and security for the HDCP keys. Before receiving samples of the SiI9616 video processor, customers must sign the HDCP license agreement (available from Digital Content Protection LLC) or a special NDA with Lattice Semiconductor.

2.18.6. EDID RAM Block

An EDID block is supported on the HDMI receiver port. The EDID block consists of 256 bytes of RAM to contain the EDID data structure. This memory, comprised of SRAM, is volatile and must be initialized by software during power up.

2.19. Audio Input Processing

The SiI9616 video processor provides multiple ways to accept digital audio signals for insertion onto the HDMI output stream. The HDMI transmitter receives the audio stream through an I^2S or S/PDIF port. Audio data can come from one of many sources for each interface, controlled by a multiplexer. This is illustrated in Figure 2.2 on page 10.

All major audio encoding formats are supported, including LPCM audio, one-bit audio, and bitstream audio formats including high-bitrate audio.

2.19.1. I^2S Audio Input

There are two external I^2S ports on the SiI9616 device. The first I^2S port is comprised of three signal pins: AI_SCK, AI_WS, and AI_SD. The signal pins are dedicated inputs intended to support two-channel linear pulse code modulation (LPCM) audio. This I^2S input port accepts audio sample frequencies of 32, 44.1, 48, 88.2, 96, 176.4, and 192 kHz.

The second I^2S port has seven signal pins: AO_MCLK, AO_SCK, AO_WS, and AO_SD[3:0]. All pins except AO_MCLK are bidirectional. The direction of these pins is controlled by a software programmable register. These pins default to outputs. When the pins are configured as inputs, they enable an input of up to eight channels of LPCM audio for insertion onto the HDMI output. The I^2S input supports sampling frequencies from 32 to 192 kHz.

The multichannel I^2S input also supports high-bitrate audio formats like Dolby® TrueHD and DTS-HD Master Audio™.

Only one of the I^2S ports can be selected to send audio data to the HDMI transmitter at any given time.

2.19.2. Direct Stream Digital Input

Seven pins are used for the Direct Stream Digital interface that provides six-channel one-bit audio data (DSD). This interface is for SACD applications. The DSD interface shares the multichannel I^2S and S/PDIF pins of the SiI9616 device.

The one-bit audio inputs are sampled on the positive edge of the DSD clock, assembled into 56-bit packets, and mapped to the appropriate FIFO. The Audio InfoFrame, instead of the Channel Status bits, carries the sampling information for one-bit audio. The one-bit audio interface supports an input clock frequency of 2.882 MHz (64 • 44.1 kHz).

Table 2.11. DSD Pin Mapping

DSD Signal	Pin #	Pin Name
DCLK	73	AO_SCK
DR0	74	AO_WS
DL0	72	AO_SD0
DR1	71	AO_SD1
DL1	70	AO_SD2
DR2	69	AO_SD3
DL2	77	AO_SPDIF

2.19.3. S/PDIF Input

The SiI9616 device can accept digital audio from a S/PDIF input pin. The Sony/Philips Digital Interface Format (S/PDIF) interface is usually associated with compressed audio formats such as Dolby® Digital (AC-3), DTS, and the more advanced variants of these formats.

The S/PDIF interface also supports the LPCM format at sampling frequencies of 32 kHz, 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, 176.4 kHz, and 192 kHz.

2.19.4. Requirement for an MCLK

The video processor includes an integrated MCLK generator for operation without requiring an external clock PLL. This removes the requirement for an MCLK input on the device for creating the time stamp value used in audio clock recovery.

2.19.5. Audio Downsampler

The SiI9616 device has an audio downsampler function that downsamples the incoming two-channel audio data and sends the result over the HDMI link. The audio data can be downsampled by one-half or one-fourth with register control. Conversions from 192 kHz to 48 kHz, 176.4 kHz to 44.1 kHz, 96 kHz to 48 kHz, and 88.2 kHz to 44.1 kHz are supported. Some limitations in the audio sample word length, when using this feature, may need special consideration in a real application.

When enabling the audio downsampler, the Channel Status registers for the audio sample word lengths sent over the HDMI link always indicate the maximum possible length. For example, if the input S/PDIF stream was in 20-bit mode with 16 bits valid after enabling the downsampler, the Channel Status indicates 20-bit mode with 20 bits valid.

Audio sample word length is carried in bits 33 through 35 of the Channel Status register over the HDMI link, as shown in Table 2.12 on the next page. These bits are always set to 0b101 when enabling the downsampler feature. Audio data is not affected because zeros are placed into the LSBs of the data, and the wider word length is sent across the HDMI link.

Table 2.12. Channel Status Bits Used for Word Length

Bit				Sample Word Length (bits)	Note
Audio Sample Word Length			Maximum Word Length[1]		
35	34	33	32		
0	0	0	0	Not Indicated	—
0	0	1	0	16	2
0	1	0	0	18	2
1	0	0	0	19	2
1	0	1	0	20	2, 4
1	1	0	0	17	2
0	0	0	1	Not Indicated	3
0	0	1	1	20	3
0	1	0	1	22	3
1	0	0	1	23	3
1	0	1	1	24	3, 4
1	1	0	1	21	3

Notes:
1. Maximum audio sample word length (MAXLEN) is 20 bits if MAXLEN = 0 and 24 bits if MAXLEN = 1.
2. Maximum audio sample word length is 20.
3. Maximum audio sample word length is 24.
4. Bits [35:33] are always 0b101 when the downsampler is enabled.

2.19.6. High-bitrate Audio on HDMI

The high-bitrate compression standards, such as Dolby® TrueHD and DTS-HD Master Audio™, transmit data at bitrates as high as 18 Mb/s or 24 Mb/s. Because these bit rates are so high, Blu-ray decoders, HDMI transmitters (as source devices), and DSPs and HDMI receivers (as sink devices) must carry the data using four I^2S lines rather than using a single very-high-speed S/PDIF interface or I^2S bus (see Figure 2.20).

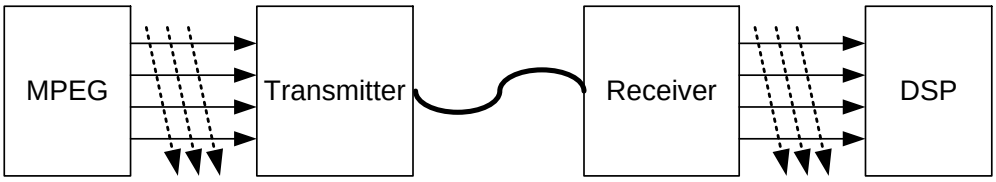


Figure 2.20. High-speed Data Transmission

The high-bitrate audio stream is originally encoded as a single stream. To send the stream over four I^2S lines, the DVD decoder splits it into four streams. Figure 2.21 shows the high-bitrate stream before it has been split into four I^2S lines, and Figure 2.22 on the next page shows the same audio stream after being split. Each sample requires 16 cycles of the I^2S clock (SCK).

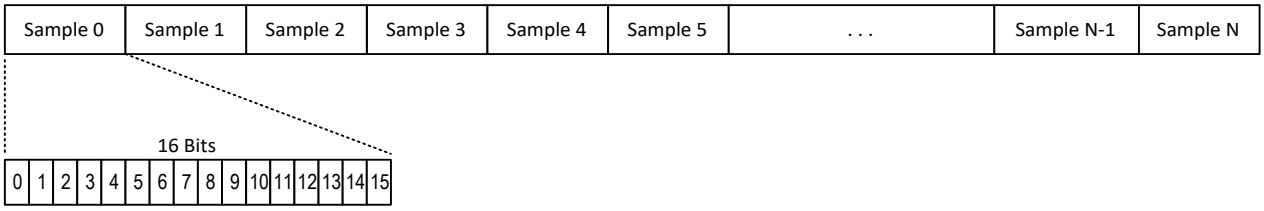


Figure 2.21. High-bitrate Stream before and after Reassembly and Splitting

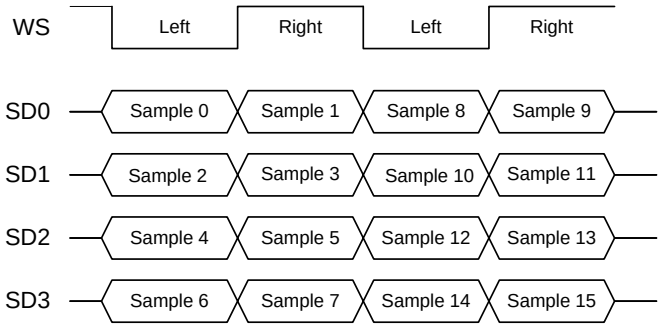


Figure 2.22. High-bitrate Stream after Splitting

2.19.7. I²S-to-S/PDIF Conversion

The SiI9616 video processor includes audio processing to convert LPCM audio from the two-channel I²S input, or from the I²S output of the HDMI receiver, to an IEC 60958 formatted audio stream. The converted audio stream is sent to the S/PDIF output pin. The conversion works only for two-channel audio.

2.20. Audio Output Processing

The SiI9616 video processor supports audio extraction from the received HDMI/MHL streams. It can send the digital audio to a S/PDIF output, four I²S outputs (SD[3:0]), or six one-bit audio outputs. In addition, the audio output signals can be routed directly to the audio input ports of the HDMI transmitter using an internal audio data path. Internal routing, multiplexing and processing of I²S and SPDIF audio signals are illustrated in Figure 2.2 on page 10.

2.20.1. S/PDIF Output

The S/PDIF output transmits two-channel uncompressed LPCM data (IEC 60958) or a compressed bitstream for multichannel (IEC 61937) formats. The audio data output logic forms the audio data output stream from the HDMI audio packets. The S/PDIF output supports audio sampling rates from 32 to 192 kHz. A separate master clock output (MCLK), coherent with the S/PDIF output, is provided for time-stamping purposes.

2.20.2. I²S Audio Output

An I²S output port with four data lines on the SiI9616 device enables eight-channel digital audio output at sample rates from 32 to 192 kHz. The I²S interface is highly programmable through registers to allow interfacing with a wide range of audio DACs or audio DSPs with I²S inputs. The I²S output port consists of signal pins AO_MCLK, AO_SCK, AO_WS, and AO_SD[3:0].

Additionally, an MCLK output signal is provided with a frequency that is programmable as an integer multiple of the audio sample rate f_S. MCLK frequencies support various audio sample rates as shown in Table 2.13.

Table 2.13. Supported MCLK Frequencies

Multiple of f_S	Audio Sample Rate, f_S: I²S and S/PDIF Supported Rates						
	32 kHz	44.1 kHz	48 kHz	88.2 kHz	96 kHz	176.4 kHz	192 kHz
128	4.096 MHz	5.645 MHz	6.144 MHz	11.290 MHz	12.288 MHz	22.579 MHz	24.576 MHz
256	8.192 MHz	11.290 MHz	12.288 MHz	22.579 MHz	24.576 MHz	45.158 MHz	49.152 MHz
384	12.288 MHz	16.934 MHz	18.432 MHz	33.864 MHz	36.864 MHz	—	—
512	16.384 MHz	22.579 MHz	24.576 MHz	45.158 MHz	49.152 MHz	—	—

The I²S output pins can be reconfigured as inputs for source-specific applications, such as a Blu-ray player where the SoC supplies the multichannel audio to the SiI9616 device directly through the I²S bus.

2.20.3. One-bit Audio Output (DSD/SACD)

The SiI9616 device can output six DSD streams and a clock for up to six-channel support. The DSD streams are output on the I²S and S/PDIF pins. One-bit audio supports 64 • f_S, with f_S being 44.1 kHz or 88.2 kHz. DSD output pin mapping is the same as for DSD input, as shown in Table 2.11 on page 35.

The one-bit audio outputs are synchronous to the positive edge of the DSD Clock. For one-bit audio, the sampling information is carried in the Audio InfoFrame, instead of the Channel Status bits.

2.20.4. High-bitrate Audio Support

The SiI9616 video processor supports the extraction of high-bitrate audio packets from the HDMI input. The extracted data is streamed out through the I²S output port on four I²S data lines at 192 kHz packet rate each.

Figure 2.23 shows the layout of the high-bitrate audio samples on four I²S lines.

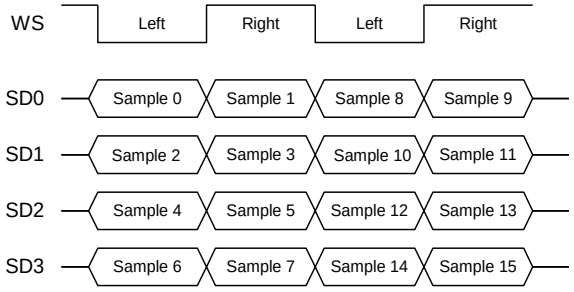


Figure 2.23. Layout of High-bitrate Audio Samples on I²S

2.20.5. Auto Audio Configuration

The SiI9616 video processor can control the audio output based on the current states of CablePlug, FIFO, Video, ECC, ACR, PLL, InfoFrame and HDMI. Audio output is only enabled when all necessary conditions are met. If any critical condition is missing, the audio output is disabled automatically. Each of these events, which the logic monitors, can be turned on or off separately through a set of programmable registers.

2.20.6. Soft Mute

On command from a register bit or when automatically triggered with Automatic Audio Control (AAC), the video processor progressively reduces the audio data amplitude to mute the sound in a controlled manner. This is useful when there is an interruption to the HDMI audio stream (or an error) to prevent any audio pop from being sent to the I²S or S/PDIF outputs.

2.21. CEC Interface

The Consumer Electronics Control (CEC) Interface block provides CEC electrically compliant signals between CEC devices and a CEC master. A CEC controller compatible with the Lattice Semiconductor CEC Programming Interface (CPI) is included on the chip. This CEC controller has a high-level register interface accessible through the I²C or SPI interface and can send and receive CEC commands. This controller makes CEC control very easy and straightforward, and removes the burden of having a host CPU perform these low-level transactions on the CEC bus.

2.22. GPIO

The SiI9616 video processor has four General Purpose I/O (GPIO) pins. Each GPIO pin supports the following functions:

- Input mode: The value can be read through a register.
- Output mode: The value can be set through a programmable register.

The GPIO pins can be reconfigured as a Serial Pheripheral Interface (SPI) for programming the chip. Refer to the Pin Strapping section on page 39 for more information.

2.23. Control and Configuration

2.23.1. Register/Configuration Logic

The register/configuration logic block incorporates all the registers required for configuring and managing the features of the SiI9616 video processor. These registers are used to perform HDCP authentication, audio/video/auxiliary format processing, CEA-861B InfoFrame packet format, and power-down control.

The registers are accessible from one of two I^2C serial ports. The first is the DDC port located on the HDMI receiver port, and is connected through the HDMI cable to the upstream HDMI transmitter. It is used to exchange values between the transmitter and the SiI9616 video processor for HDCP operation. The second port is the local I^2C port that controls the SiI9616 device from the display system. The local device registers controlled by the display system can also be accessed through a Serial Peripheral Interface (SPI) bus.

The local device registers are accessed using a 16-bit addressing scheme. Refer to the Feature Information section on page 66 for details.

2.23.2. I^2C Serial Ports

The SiI9616 video processor provides three I^2C serial interfaces:

- DDC receiver port to communicate back to the upstream HDMI or DVI host,
- DDC master port to read the EDID or perform HDCP authentication of the downstream device,
- I^2C port for initialization and control by a local microcontroller in the display.

Refer to the Feature Information section on page 66 for a more detailed description of these serial ports.

The device address for the local I^2C interface can be set as 0x30 or 0x32 through a strapping pin (see Table 2.14 below).

2.23.3. SPI Serial Bus

The SiI9616 SPI serial interface employs a simple four-wire synchronous serial interface with unidirectional data lines. The SPI interface allows the local microcontroller to access the SiI9616 device registers at up to 10 MHz bitrate. This is a more efficient method of configuring the device when compared to I^2C mode. Refer to the Feature Information section on page 66 for a more detailed description of SPI.

2.23.4. Delay from Reset Deactivation to Register Access

Once the Reset pin of the SiI9616 device is deactivated, the software must wait 100 ns before accessing the device registers through either the local I^2C or SPI bus.

2.24. Pin Strapping

The SiI9616 device supports pin strapping configuration to select the default device I^2C address and the mode of the SPI pins. These settings are shown in Table 2.14. The logical value on these pins are latched by the SiI9616 device on the rising edge of RESET. See the Digital Audio Output Pins table on page 62 for more information.

Table 2.14. Pin Strapping Options

Pin Name	Mode Name	Description
AO_MUTE	I2C_ADDRSEL	Select I^2C Address (0x30/0x32). 0 – Address 0x30 1 – Address 0x32
AO_SPDIF/DL2	GPIO_MODE	Select GPIO Mode. 0 – SPI pins used as SPI 1 – SPI pins used as GPIO

2.25. Power Supply Sequencing

There are no power supply sequencing requirements for the SiI9616 device.

2.26. Audio PLL Reset

Once the SiI9616 device is powered on and all the power supplies of the device have reached their normal operating voltages, the audio PLL must be reset to ensure normal operation. The audio PLL is reset by asserting its Power Down bit for at least 1 ms.

3. Electrical Specifications

3.1. Absolute Maximum Conditions

Table 3.1. Absolute Maximum Conditions

Symbol	Parameter	Min	Typ	Max	Units	Notes
IO_VDD33	I/O Pin Supply Voltage	–0.3	—	4.0	V	1, 2, 3
IO_APVDD33	Audio PLL I/O Supply Voltage	–0.3	—	4.0	V	1, 2, 3
RX_AVDD10	TMDS RX Analog 1.0 V Supply Voltage	–0.3	—	1.5	V	1, 2
RX_AVDD33	TMDS RX Analog 3.3 V Supply Voltage	–0.3	—	4.0	V	1, 2
TX_AVDD10	TMDS TX Analog Supply Voltage	–0.3	—	1.5	V	1, 2
TX_PVDD10	TMDS TX PLL Supply Voltage	–0.3	—	1.5	V	1, 2
VP_AVDD10	Video PLL Supply Voltage	–0.3	—	1.5	V	1, 2
AP_AVDD10	Audio PLL Supply Voltage	–0.3	—	1.5	V	1, 2
DVDD10	Digital Logic Supply Voltage	–0.3	—	1.5	V	1, 2
IO_VDD5	I/O Pin 5 V Supply Voltage	–0.3	—	5.7	V	1, 2
V_I	Input Voltage	–0.3	—	IO_VDD33 + 0.3	V	1, 2
$V_{5V\text{-}Tolerant}$	Input Voltage on 5 V tolerant Pins	–0.3	—	5.7	V	—
T_J	Junction Temperature	—	—	125	°C	—
T_{STG}	Storage Temperature	–65	—	150	°C	—

Notes:
1. Permanent device damage can occur if absolute maximum conditions are exceeded.
2. Functional operation should be restricted to the conditions described under normal operating conditions.
3. Voltage undershoot or overshoot cannot exceed absolute maximum conditions.
4. Refer to the SiI9616 Qualification Report for information on ESD performance.

3.2. Normal Operating Conditions

Table 3.2. Normal Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units	Notes
IO_VDD33	I/O Pin Supply Voltage	3.14	3.3	3.47	V	—
IO_APVDD33	Audio PLL I/O Supply Voltage	3.14	3.3	3.47	V	—
RX_AVDD10	TMDS RX Analog 1.0 V Supply Voltage	0.95	1.0	1.05	V	—
RX_AVDD33	TMDS RX Analog 3.3 V Supply Voltage	3.14	3.3	3.47	V	—
TX_AVDD10	TMDS TX Analog Supply Voltage	0.95	1.0	1.05	V	—
TX_PVDD10	TMDS TX PLL Supply Voltage	0.95	1.0	1.05	V	—
VP_AVDD10	Video PLL Supply Voltage	0.95	1.0	1.05	V	—
AP_AVDD10	Audio PLL Supply Voltage	0.95	1.0	1.05	V	—
DVDD10	Digital Logic Supply Voltage	0.95	1.0	1.05	V	—
IO_VDD5	I/O Pin 5 V Supply Voltage	4.75	5.0	5.25	V	1
T_A	Ambient Temperature (with power applied)	0	—	70	°C	—
Θ_{ja}	Ambient Thermal Resistance (Theta JA)	—	—	27	°C/W	2

Notes:
1. The IO_VDD5 pin is the supply voltage for the CSCL, CSDA, CEC, CDSENSE, TX_DSCL, TX_DSDA, RX_DSDA, RX_DSCL, and RX_HPD/CBUS pins. It must be connected to a 5 V power supply.
2. Airflow at 0 m/s.

3.3. DC Specifications

Table 3.3. Digital I/O Specifications

Symbol	Parameter	Pin Type[1]	Conditions	Min	Typ	Max	Units	Notes
V_{IH}	HIGH-level Input Voltage	LVTTL Schmitt	—	2.0	—	—	V	—
V_{IL}	LOW-level Input Voltage	LVTTL Schmitt	—	—	—	0.8	V	—
DDC V_{TH+}	LOW-to-HIGH Threshold, DDC Bus	Schmitt	—	3.0	—	—	V	2
DDC V_{TH-}	HIGH-to-LOW Threshold, DDC Bus	Schmitt	—	—	—	1.5	V	2
V_{OH}	HIGH-level Output Voltage	LVTTL	—	2.4	—	—	V	—
V_{OL}	LOW-level Output Voltage	LVTTL	—	—	—	0.4	V	—
$V_{OL\ DDC}$	LOW-level Output Voltage	Open-drain	I_{OL} = –3 mA	—	—	0.4	V	—
$V_{OL\ I2C}$	LOW-level Output Voltage	Open-drain	I_{OL} = –3 mA	—	—	0.4	V	—
I_{OL}	Output Leakage Current	—	High-impedance	–10	—	100	µA	3
I_{IL}	Input Leakage Current	—	High-impedance	–10	—	100	µA	4
I_{OD6}	6 mA Digital Output Drive	Output	V_{OUT} = 2.4 V	6	—	—	mA	—
			V_{OUT} = 0.4 V	6	—	—	mA	—
I_{OD8}	8 mA Digital Output Drive	Output	V_{OUT} = 2.4 V	8	—	—	mA	—
			V_{OUT} = 0.4 V	8	—	—	mA	—
I_{OD16}	16 mA Digital Output Drive	Output	V_{OUT} = 2.4 V	16	—	—	mA	—
			V_{OUT} = 0.4 V	16	—	—	mA	—
R_{PD}	Internal Pull Down Resistor	Outputs	—	—	46	—	kΩ	—
I_{OPD}	Output Pull Down Current	Outputs	IO_VDD33 = 3.47 V	—	—	100	µA	3
I_{IPD}	Input Pull Down Current	Input	IO_VDD33 = 3.47 V	—	—	100	µA	4

Notes:

1. Refer to the Pin Diagram and Pin Descriptions section on page 57 for pin type designations for all package pins.
2. Schmitt trigger input pin thresholds V_{TH+} and V_{TH-} correspond to V_{IH} and V_{IL}, respectively.
3. The chip includes an internal pull-down resistor on many of the output pins. When in the high-impedance state, these pins draw a pull-down current according to this specification when the signal is driven HIGH by another source device.
4. The chip includes an internal pull-down resistor on many of the input pins. These pins draw a pull-down current according to this specification when the signal is driven HIGH by another device.

Table 3.4. TMDS Input DC Specifications – HDMI Mode

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IDFH}	Differential Mode Input Voltage	—	150	—	1200	mV
V_{ICMH}	Common Mode Input Voltage	—	RX_AVDD33 – 400	—	RX_AVDD33 – 37.5	mV

Table 3.5. TMDS Input DC Specifications – MHL Mode

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IDC}	Single-ended Input DC Voltage	—	RX_AVDD33 – 1200	—	RX_AVDD33 – 300	mV
V_{IDFM}	Differential Mode Input Swing Voltage	—	200	—	1000	mV
V_{ICMM}	Common Mode Input Swing Voltage	—	170	—	Min (720, 0.85 V_{IDF})	mV

Table 3.6. TMDS Output DC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VSWING	Single-ended Output Swing Voltage	R_{LOAD} = 50 Ω	400	—	600	mV
VH	Single-ended HIGH-level Output Voltage	≤ 165 MHz TMDS clock	TX_AVDD33 – 10	—	TX_AVDD33 + 10	mV
		> 165 MHz TMDS clock	TX_AVDD33 – 200	—	TX_AVDD33 + 10	mV
VL	Single-ended LOW-level Output Voltage	≤ 165 MHz TMDS clock	AVDD33 – 600	—	AVDD33 – 400	mV
		> 165 MHz TMDS clock	AVDD33 – 700	—	AVDD33 – 400	mV

Table 3.7. Single Mode Audio Return Channel DC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IS_ARC}	Input Swing Amplitude	—	160	—	600	mV

Table 3.8. CEC DC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{TH+CEC}	LOW-to-HIGH Threshold	—	2.0	—	—	V
V_{TH-CEC}	HIGH-to-LOW Threshold	—	—	—	0.8	V
V_{OH_CEC}	HIGH-level Output Voltage	—	2.5	—	—	V
V_{OL_CEC}	LOW-level Output Voltage	—	—	—	0.6	V
I_{IL_CEC}	Input Leakage Current	Power Off	—	—	1.8	µA

Table 3.9. CBUS DC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH_CBUS}	High-level Input Voltage	—	1.0	—	—	V
V_{IL_CBUS}	Low-level Input Voltage	—	—	—	0.6	V
V_{OH_CBUS}	High-level Output Voltage	I_{OH} = 100 µA	1.5	—	1.9	V
V_{OL_CBUS}	Low-level Output Voltage	I_{OL} = –100 µA	—	—	0.2	V
Z_{DSC_CBUS}	Pull-down Resistance – Discovery	—	800	1000	1200	Ω
Z_{ON_CBUS}	Pull-down Resistance – Active	—	90	100	110	kΩ
I_{IL_CBUS}	Input Leakage Current	High-impedance	—	—	1	µA
C_{CBUS}	Capacitance	Power On	—	—	80	pF

3.3.1. DC Power Supply Pin Specifications

Table 3.10. Total Power Dissipation

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{IO_VDD33}	Supply Current for IO_VDD33	—	—	—	80	mA
$I_{IO\_APVDD33}$	Supply Current for IO_APVDD33	—	—	—	5	mA
I_{RX_AVDD10}	Supply Current for RX_AVDD10	—	—	—	80	mA
I_{RX_AVDD33}	Supply Current for RX_AVDD33	—	—	—	57	mA
I_{TX_AVDD10}	Supply Current for TX_AVDD10	—	—	—	38	mA
I_{TX_PVDD10}	Supply Current for TX_PVDD10	—	—	—	9	mA
I_{VP_AVDD10}	Supply Current for VP_AVDD10	—	—	—	12	mA
I_{AP_AVDD10}	Supply Current for AP_AVDD10	—	—	—	3	mA
I_{DVDD10}	Supply Current for DVDD10	—	—	—	1017	mA
I_{IO_VDD5}	Supply Current for IO_VDD5	—	—	—	8	mA
Total	Total Power	—	—	—	1.75	W

Notes: Maximum power dissipation has been measured under the following operating conditions:

- 70 °C ambient temperature with device power supplies set to 5% over normal operating values.
- Scaling 480p 60 Hz input from PVI to 1080p 60 Hz output to PVO with a pseudo random pattern and video processing enabled. PVO bus format has been configured as 20-bit YCbCr 4:2:2.
- Pass through of 4K 24 Hz video from HDMI input to HDMI output with a pseudo random pattern.

Table 3.11. Maximum IO_VDD33 Power Dissipation in 36-bit RGB Format

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{IO_VDD33}	Supply Current for IO_VDD33	—	—	—	184	mA

Notes: Maximum power dissipation has been measured under the following operating conditions:

- 70 °C ambient temperature with device power supplies set to 5% over normal operating values.
- PVO output one-pixel black and white checkerboard pattern at 165 MHz clock rate.

Table 3.12. Power-down Mode Power Dissipation

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{PD_1V}	1 V Power Supply Current	—	—	—	280	mA
$I_{PD\_3.3V}$	3.3 V Power Supply Current	—	—	—	7	mA
I_{PD_5V}	5 V Power Supply Current	—	—	—	8	mA
Total	Total Power	—	—	—	360	mW

Note: Maximum power dissipation has been measured at 70 °C ambient temperature with supplies set to 5% over normal operating values, and no switching applied on the input and output ports.

3.4. AC Specifications

Table 3.13. TMDS Input AC Timing Specifications – HDMI Mode

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure
T_{DPS}	Intra Pair Differential Input Skew	@300 MHz	—	—	$0.15T_{bit}$ + 112	ps	—
T_{CCS}	Channel-to-Channel Differential Input Skew	—	—	—	$0.2T_{PIXEL}$ + 1.78	ns	Figure 4.1
F_{RXC}	Differential Input Clock Frequency	—	25	—	300	MHz	—
T_{RXC}	Differential Input Clock Period	—	3.33	—	40	ns	—
T_{DIJIT}	Differential Input Clock Jitter Tolerance	@300 MHz	—	—	0.3	T_{BIT}	—

Table 3.14. TMDS Input AC Timing Specifications – MHL Mode

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{SKEW_DF}	Input Differential Intra Pair Skew	—	—	—	93	ps
T_{SKEW_CM}	Input Common Mode Intra Pair Skew	—	—	—	93	ps
F_{RXC}	Differential Input Clock Frequency	—	25	—	300	MHz
T_{RXC}	Differential Input Clock Period	—	3.33	—	40	ns
T_{CLOCK_JIT}	Common Mode Clock Jitter Tolerance	@300 MHz	—	—	$0.8T_{BIT}$	ps
T_{DATA_JIT}	Differential Data Jitter Tolerance	@300 MHz	—	—	$0.6T_{BIT}$	ps

Table 3.15. TMDS Output AC Timing Specifications Mode

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{TXDPS}	Intra Pair Differential Output Skew	—	—	—	0.15	T_{BIT}
T_{TXRT}	Data/Clock Rise Time	20% – 80%	75	—	—	ps
T_{TXFT}	Data/Clock Fall Time	20% – 80%	75	—	—	ps
F_{TXC}	Differential Output Clock Frequency	—	25	—	300	MHz
T_{TXC}	Differential Output Clock Period	—	3.33	—	40	ns
T_{DCDUTY}	Differential Output Clock Duty Cycle	—	40%	—	60%	T_{TXC}
T_{DOJIT}	Differential Output Clock Jitter	—	—	—	0.25	T_{BIT}

Table 3.16. CEC AC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{R_CEC}	Rise Time	10% – 90%	—	—	250	µs
T_{F_CEC}	Fall Time	10% – 90%	—	—	50	µs

Table 3.17. CBUS AC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{BIT_CBUS}	Bit Time	1 MHz clock	0.8	—	1.2	µs
T_{BJIT_CBUS}	Bit-to-Bit Jitter	—	–1%	—	+1%	T_{BIT_CBUS}
T_{DUTY_CBUS}	Duty Cycle of 1 Bit	—	40%	—	60%	T_{BIT_CBUS}
T_{R_CBUS}	Rise Time	0.2 V – 1.5 V	5	—	200	ns
T_{F_CBUS}	Fall Time	0.2 V – 1.5 V	5	—	200	ns
ΔT_{RF}	Rise-to-Fall Time Difference	—	—	—	100	ns

Table 3.18. Video Input Timing Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Notes
T_{ICIP}	PVI_CLK period, one pixel per clock	—	6.06	—	74.07	ns	Figure 4.2	1
F_{ICIP}	PVI_CLK frequency, one pixel per clock	—	13.5	—	165	MHz	—	1
T_{CIP12}	PVI_CLK period, dual edge clock	—	13.47	—	74.07	ns	Figure 4.2	2
F_{CIP12}	PVI_CLK frequency, dual edge clock	—	13.5	—	74.25	MHz	—	2
T_{IDUTY}	PVI_CLK duty cycle	—	40%	—	60%	T_{CIP}	Figure 4.2	—
T_{SIDF}	Setup Time to PVI_CLK falling edge	Falling edge clocking	0.53	—	—	ns	Figure 4.4	3, 4
T_{HIDF}	Hold Time to PVI_CLK falling edge		0.74	—	—	ns		
T_{SIDR}	Setup Time to PVI_CLK rising edge	Rising edge clocking	0.53	—	—	ns	Figure 4.3	3, 5
T_{HIDR}	Hold Time to PVI_CLK rising edge		0.74	—	—	ns		
T_{SIDD}	Setup Time to PVI_CLK rising or falling edge	Dual edge clocking	0.53	—	—	ns	Figure 4.5	3
T_{HIDD}	Hold Time to PVI_CLK rising or falling edge		0.74	—	—	ns		

Notes:

1. T_{ICIP} and F_{ICIP} apply in single edge clocking modes. T_{ICIP} is the inverse of F_{ICIP} and is not a controlling specification.
2. T_{CIP12} and F_{CIP12} apply in dual edge mode. T_{CIP12} is the inverse of F_{CIP12} and is not a controlling specification.
3. Setup and hold time specifications apply to PVI_DATA, PVI_DE, PVI_VSYNC, and PVI_HSYNC input pins, relative to PVI_CLK input clock.
4. Data is clocked in on the falling edge of PVI_CLK.
5. Data is clocked in on the rising edge of PVI_CLK.

Table 3.19. Video Output Timing Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Notes
D_{LHT_C}	LOW-to-HIGH Rise Time Transition, PVO_CLOCK pin	$R_{S,CLK}$ = 33 Ω C_L = 10 pF	—	—	0.60	ns	Figure 4.6	1
D_{HLT_C}	HIGH-to-LOW Fall Time Transition, PVO_CLOCK pin	$R_{S,CLK}$ = 33 Ω C_L = 10 pF	—	—	0.69	ns	Figure 4.6	1
D_{LHT_D}	LOW-to-HIGH Rise Time Transition, data and control pins	$R_{S,D}$ = 68 Ω C_L = 10 pF	—	—	2.1	ns	Figure 4.6	1, 2
D_{HLT_D}	HIGH-to-LOW Fall Time Transition, data and control pins	$R_{S,D}$ = 68 Ω C_L = 10 pF	—	—	2.2	ns	Figure 4.6	1, 2
R_{OCIP}	PVO_CLOCK Cycle Time	—	6.06	—	74.07	ns	Figure 4.7	3, 4
F_{OCIP}	PVO_CLOCK Frequency	—	13.5	—	165	MHz	—	3
T_{ODUTY}	PVO_CLOCK Duty Cycle (clock source: Video PLL)	$R_{S,CLK}$ = 33 Ω C_L = 10 pF	42%	—	51%	R_{CIP}	Figure 4.7	1, 5, 6
	PVO_CLOCK Duty Cycle (clock source: HDMI receiver clock)	$R_{S,CLK}$ = 33 Ω C_L = 10 pF	42%	—	92%	R_{CIP}	Figure 4.7	1, 5, 7
	PVO_CLOCK Duty Cycle (clock source: PVI clock)	$R_{S,CLK}$ = 33 Ω C_L = 10 pF	33%	—	67%	R_{CIP}	Figure 4.7	1, 5, 8
T_{CK2OUT}	PVO_CLOCK-to-Output Delay	$R_{S,CLK}$ = 33 Ω $R_{S,D}$ = 68 Ω C_L = 10 pF	1.5	—	3.9	ns	Figure 4.7	1

Notes:

1. Video output timing has been measured with a test circuit consisting of a 33 Ω series resistor and a 10 pF load capacitor on the clock pin, and a 68 Ω series resistor and a 10 pF load capacitor on the data and control pins (see Figure 3.1 below).
2. Applies to PVO_HSYNC, PVO_VSYNC, PVO_DE, and PVO_DATA[35:0].
3. All output timings are defined at the maximum operating clock frequency, F_{OCIP}, unless otherwise specified.
4. R_{OCIP} is the inverse of F_{OCIP} and is not a controlling specification.
5. The duty cycle of the PVO clock varies depending on the source of the clock. Refer to PVO Clock Duty Cycle section on page 31 for more information.
6. Measured at 27 MHz and 148.5 MHz output clock frequencies.
7. Measured at 27 MHz and 165 MHz output clock frequencies.
8. Measured at PVI clock duty cycles of 40% and 60%.
9. See Table 4.1 on page 55 for calculations of worst case output setup and hold times.
10. All timing parameters are applicable to the Genlock output as well, consisting of GL_CLK, GL_VSYNC, GL_HSYNC and GL_EVNODD signals.

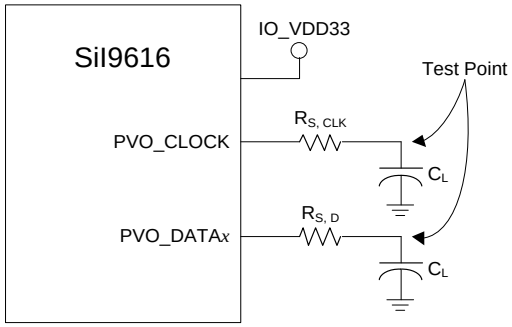


Figure 3.1. Video Output Timing Test Circuit

Table 3.20. I²S Audio Input Port Timing Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Notes
F_{S_I2S}	Sample Rate	—	32	—	192	kHz	—	—
T_{SCKCYC}	I²S Cycle Time	—	—	—	1.0	UI	Figure 4.8	1
$T_{SCKIDUTY}$	I²S Duty Cycle	—	90%	—	110%	UI	Figure 4.8	1
T_{I2SSU}	I²S Setup Time	—	15	—	—	ns	Figure 4.8	2
T_{I2SHD}	I²S Hold Time	—	5	—	—	ns	Figure 4.8	2

Notes:
1. Proportional to unit time (UI) according to sample rate. Refer to the I²S Specification.
2. Setup and hold minimum times are based on 13.388 MHz sampling, which is adapted from Figure 3 of the Philips I²S Specification.
3. All parameters are applicable to the I²S output port signals when reconfigured as inputs.

Table 3.21. S/PDIF Input Port Timing Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure
F_{S_SPDIF}	Sample Rate	—	32	—	192	kHz	—
T_{SPICYC}	AI_SPDIF Cycle Time*	—	—	—	1.0	UI	Figure 4.9
$T_{SPIDUTY}$	AI_SPDIF Duty Cycle*	—	90%	—	110%	UI	Figure 4.9

***Note:** Proportional to unit time (UI) according to sample rate. Refer to the IEC60958 Specification.

Table 3.22. I²S Audio Output Port Timing Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Notes
T_{TR}	AO_SCK Clock Period	C_L = 10 pF	1.00	—	—	T_{tr}	Figure 4.10	1, 2
T_{HC}	AO_SCK Clock HIGH Time	C_L = 10 pF	0.35	—	—	T_{tr}		1, 2
T_{LC}	AO_SCK Clock LOW Time	C_L = 10 pF	0.35	—	—	T_{tr}		1, 2
T_{SU}	Setup Time, AO_SCK to AO_SD/WS	C_L = 10 pF	$0.4T_{tr} - 5$	—	—	ns		1, 2
T_{HD}	Hold Time, AO_SCK to AO_SD/WS	C_L = 10 pF	$0.4T_{tr} - 5$	—	—	ns		1, 2
$T_{SCKODUTY}$	AO_SCK Duty Cycle	C_L = 10 pF	40%	—	60%	T_{tr}		1, 2
T_{SCK2SD}	AO_SCK-to-AO_SD or AO_WS Delay	C_L = 10 pF	–5	—	+5	ns		1, 3

Notes:
1. Guaranteed by design.
2. Refer to Figure 4.10 on page 53. Meets timings in the Philips I²S Specification.
3. Applies also to SDC-to-WS delay.

Table 3.23. S/PDIF Output Port Timing Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Notes
T_{SPOCYC}	AO_SPDIF Cycle Time	C_L = 10 pF	—	1.0	—	UI	Figure 4.11	1, 2
F_{SPDIF}	AO_SPDIF Frequency	—	4	—	24	MHz		3
$T_{SPODUTY}$	AO_SPDIF Duty Cycle	C_L = 10 pF	90%	—	110%	UI		2
$T_{MCLKCYC}$	AO_MCLK Cycle Time	C_L = 10 pF	20	—	250	ns	Figure 4.12	1
F_{MCLK}	AO_MCLK Frequency	C_L = 10 pF	4	—	50	MHz		1
$T_{MCLKDUTY}$	AO_MCLK Duty Cycle	C_L = 10 pF	40%	—	60%	$T_{MCLKCYC}$		—

Notes:
1. Guaranteed by design.
2. Proportional to unit time (UI), according to sample rate.
3. S/PDIF is not a true clock, but is generated from the internal 128 f_S clock, for f_S from 32 to 192 kHz.

Table 3.24. Crystal Clock Timings

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure
F_{XTAL}*	External Crystal Freq.	—	26	27	28.5	MHz	Figure 3.2

***Note:** The XTALIN/XTALOUT pin pair must be driven with a clock in all applications.

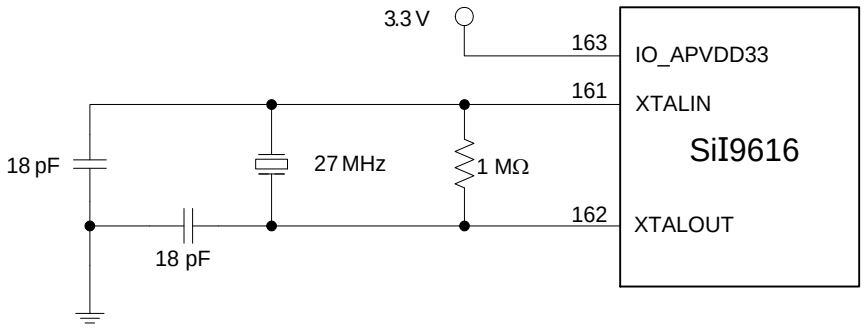


Figure 3.2. Crystal Clock Schematic

3.5. Control Timing Specifications

Table 3.25. Reset Timings

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure
T_{RESET}	RESET# Signal LOW Time for Valid Reset	—	10	—	—	µs	Figure 4.16

Table 3.26. I²C Control Signal Timings

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Notes
T_{I2CDVD}	SDA Data Valid Delay from SCL Falling Edge	C_L = 400 pF	—	—	700	ns	Figure 4.13	—
F_{RXDDC}	Clock Rate on Rx DDC Port	C_L = 400 pF	—	—	100	kHz	—	1
F_{TXDDC}	Clock Rate on Tx DDC Port	C_L = 400 pF	—	—	100	kHz	—	1, 2
F_{I^2C}	Clock Rate on Local I²C Port	C_L = 400 pF	—	—	400	kHz	—	3

Notes:
1. DDC ports are limited to 100 kHz by the HDMI Specification, and meet I²C standard mode timings.
2. The operating frequency of the HDMI transmitter DDC port is programmable.
3. Local I²C port (CSCL/CSDA) meets standard mode I²C timing requirements to 400 kHz.

Table 3.27. SPI Control Signal Timings

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure
tCSs	SPI_CS# Setup Time to SPI_CLK	—	6	—	—	ns	Figure 4.14, Figure 4.15
tCSh	SPI_CS# Hold Time to SPI_CLK	—	6	—	—	ns	Figure 4.14, Figure 4.15
tTXs	SPI_TX Setup Time to SPI_CLK	—	6	—	—	ns	Figure 4.14, Figure 4.15
tTXh	SPI_TX Hold Time to SPI_CLK	—	6	—	—	ns	Figure 4.14, Figure 4.15
tRXp	SPI_RX Output Time from SPI_CLK Falling Edge	—	1	—	7	ns	Figure 4.15

Note: Signal names are from the host's perspective.

4. Timing Diagrams

4.1. TMDS Input Timing Diagrams

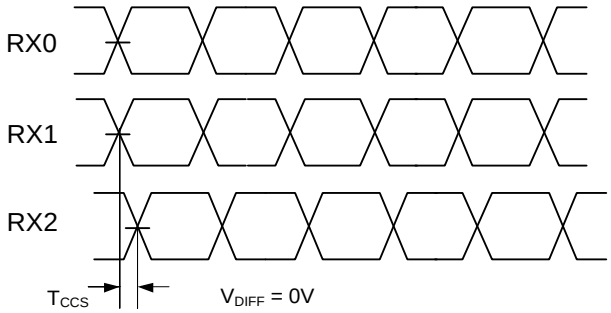


Figure 4.1. TMDS Channel-to-Channel Skew Timing

4.2. Digital Video Input Timing Diagrams

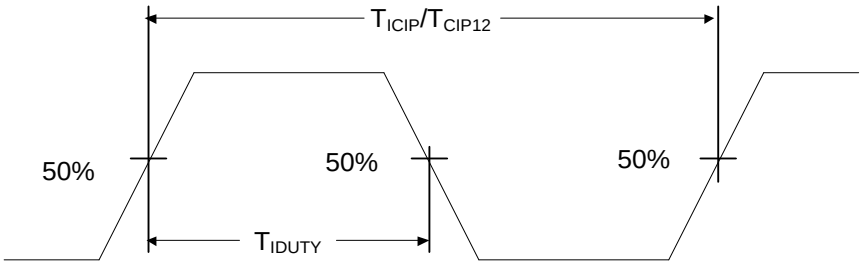
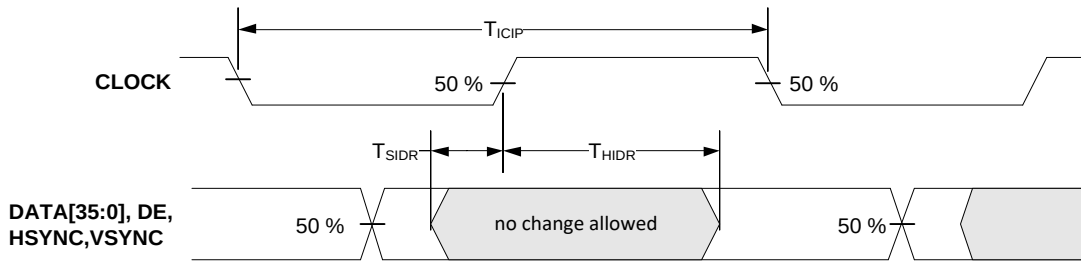
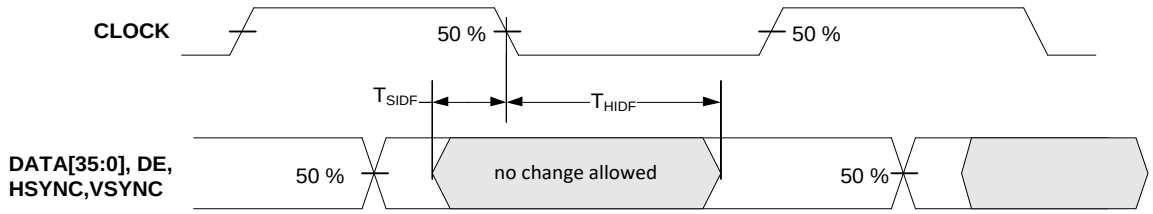


Figure 4.2. PVI_CLK Clock Duty Cycle



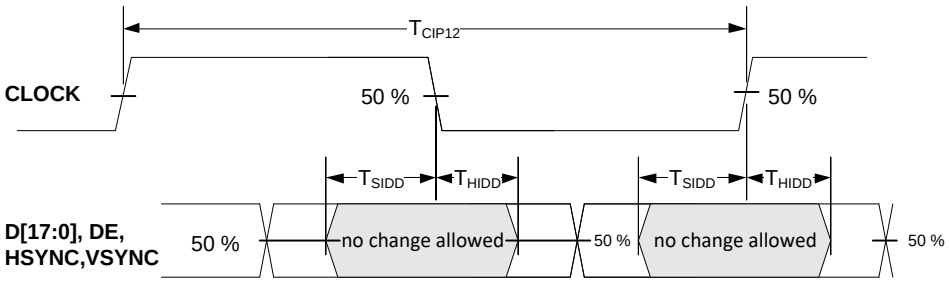
Signals may change only in the unshaded portion of the waveform, to meet both the minimum setup and minimum hold time specifications.

Figure 4.3. Control and Data Single-edge Setup and Hold Times – Rising Edge Clocking



Signals may change only in the unshaded portion of the waveform, to meet both the minimum setup and minimum hold time specifications.

Figure 4.4. Control and Data Single-edge Setup and Hold Times – Falling Edge Clocking



Signals may change only in the unshaded portion of the waveform, to meet both the minimum setup and minimum hold time specifications.

Figure 4.5. Control and Data Dual-edge Setup and Hold Times

4.3. Digital Video Output Timing Diagrams

4.3.1. Output Transition Times

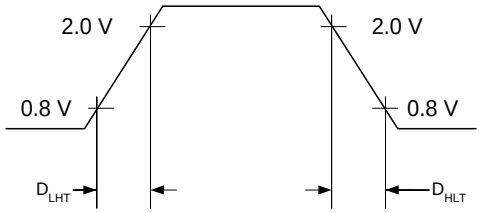


Figure 4.6. Video Digital Output Transition Times

4.3.2. Output Clock to Output Data Delay

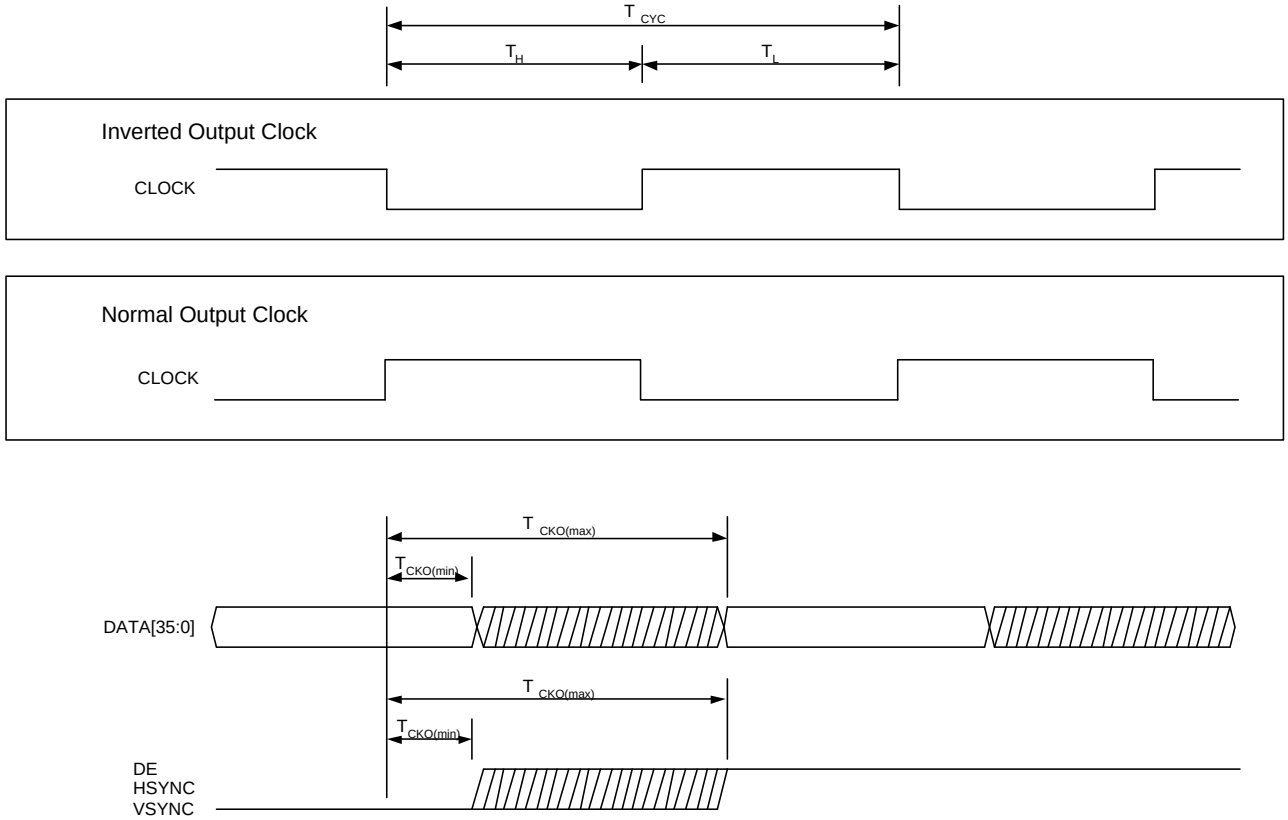


Figure 4.7. Clock-to-Output Delay and Duty Cycle Limits

4.4. Digital Audio Input Timing Diagrams

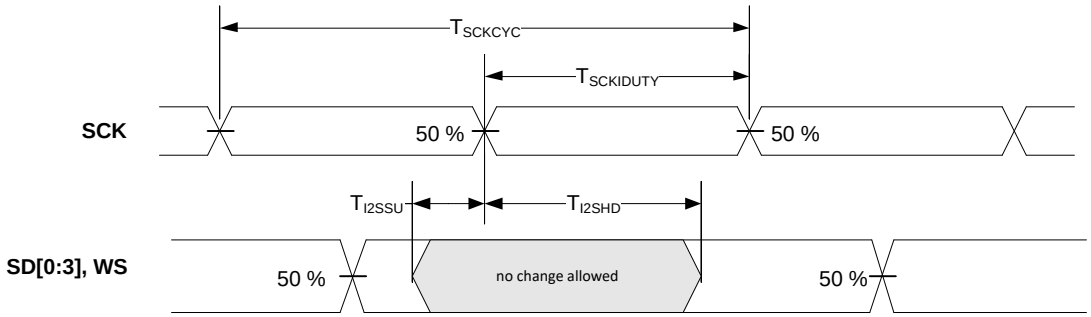


Figure 4.8. I²S Input Timings

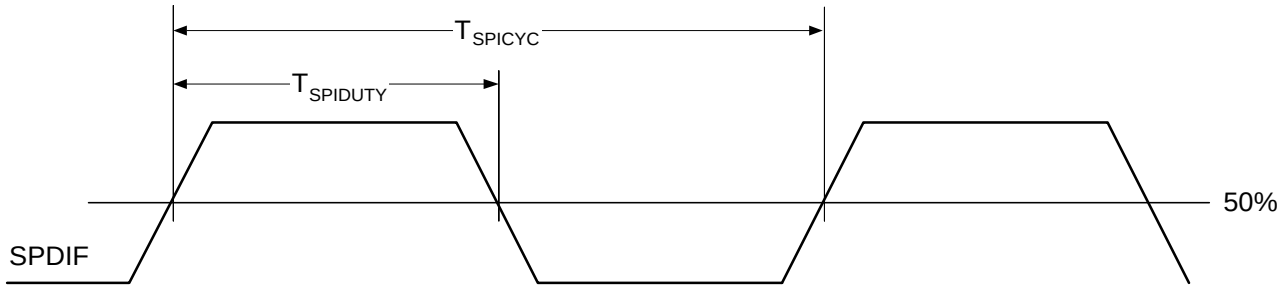


Figure 4.9. S/PDIF Input Timings

4.5. Digital Audio Output Timing Diagrams

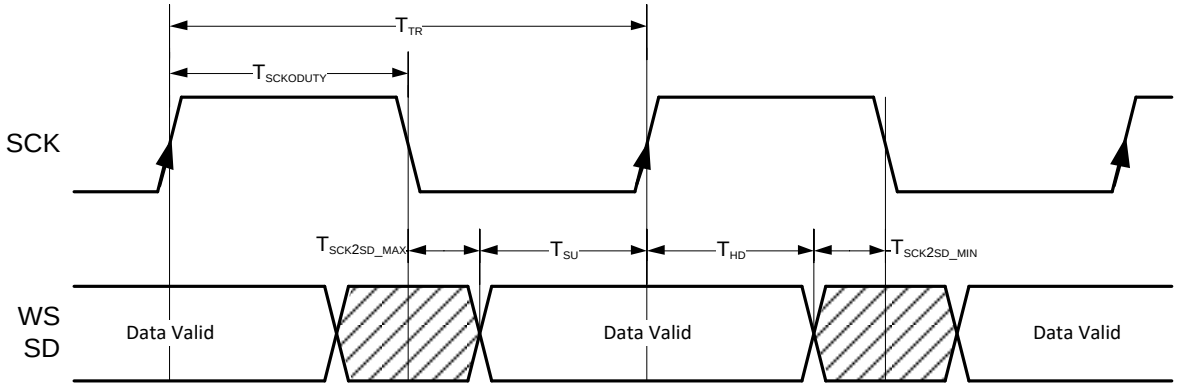


Figure 4.10. I²S Output Timings

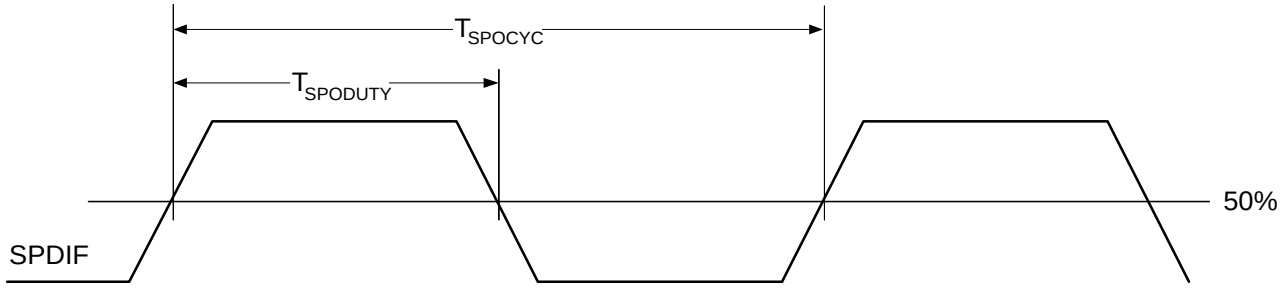


Figure 4.11. S/PDIF Output Timings

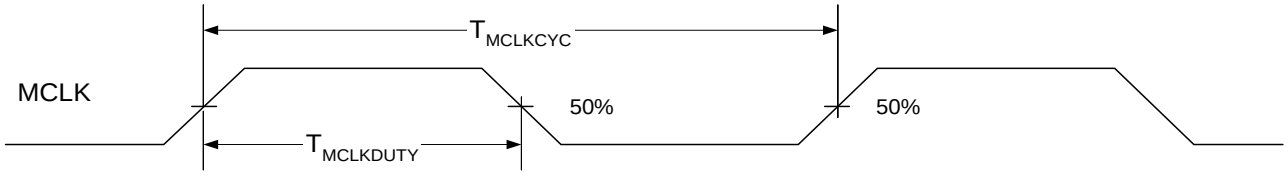


Figure 4.12. MCLK Timings

4.6. Control Signal Timing Diagrams

4.6.1. I²C Timing Diagram

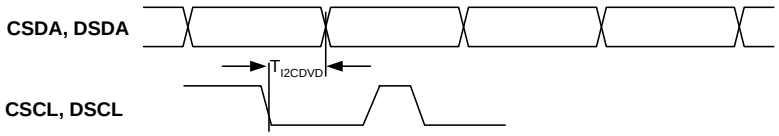


Figure 4.13. I²C Data Valid Delay

4.6.2. SPI Timing Diagrams

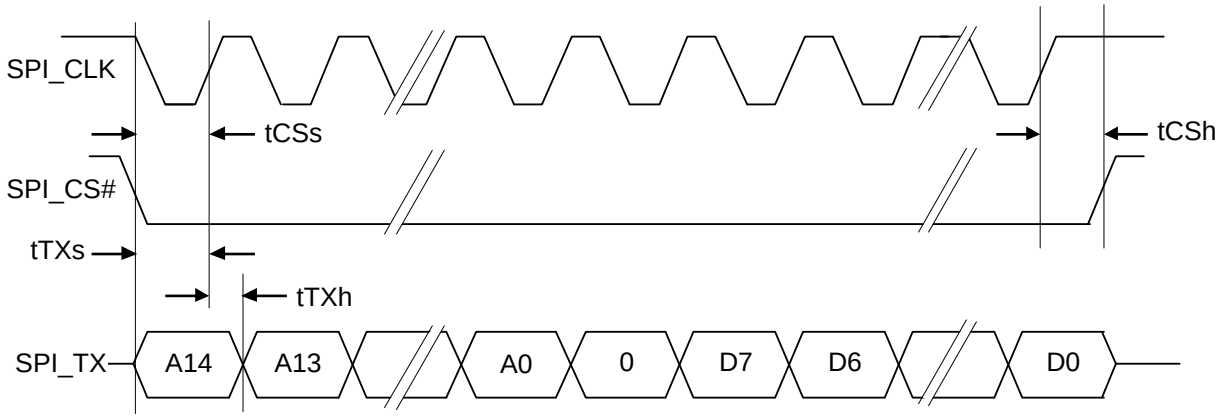


Figure 4.14. SPI Write Setup and Hold Times

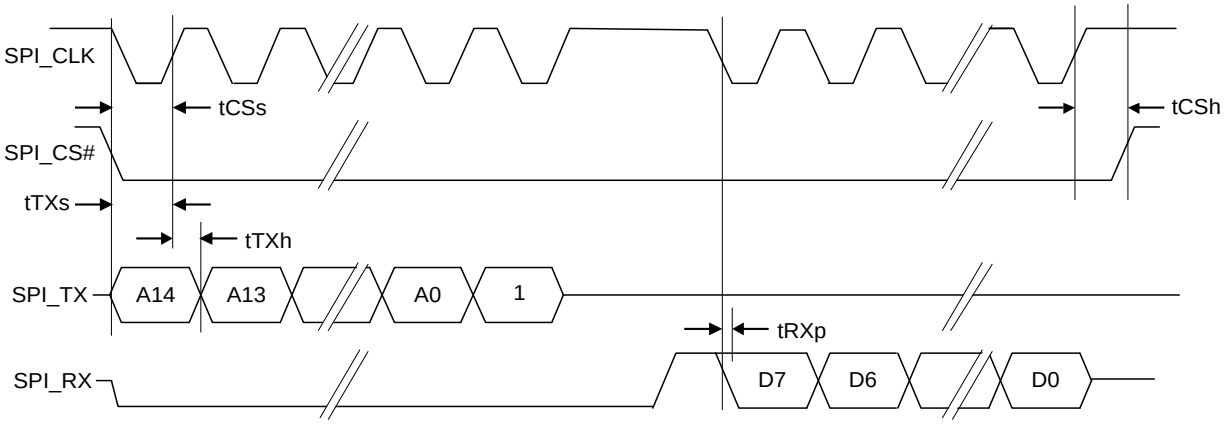
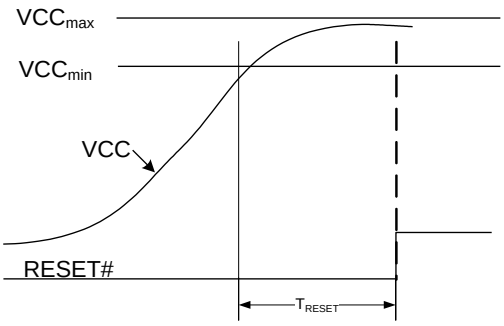
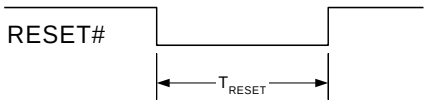


Figure 4.15. SPI Read Setup and Hold Times

4.7. Reset Timings



Note that VCC must be stable between its limits for Normal Operating Conditions for T_{RESET} before RESET# is HIGH.



RESET# must be pulled LOW for T_{RESET} before accessing registers. This can be done by holding RESET# LOW until T_{RESET} after stable power (at left); OR by pulling RESET# LOW from a HIGH state (at right) for at least T_{RESET}.

Figure 4.16. RESET# Minimum Timings

4.8. Calculating Setup and Hold Times for Parallel Video Output Bus

Output data is clocked out on one rising (or falling) edge of PVO_CLK, and is then captured downstream using the same polarity PVO_CLK edge one clock period later. The setup time of data to PVO_CLK and hold time of PVO_CLK-to-data are a function of the worst case PVO_CLK-to-output delay, as shown in Figure 4.17. The active rising PVO_CLK edge is shown with an arrowhead. For an inverted output clock, reverse the logic.

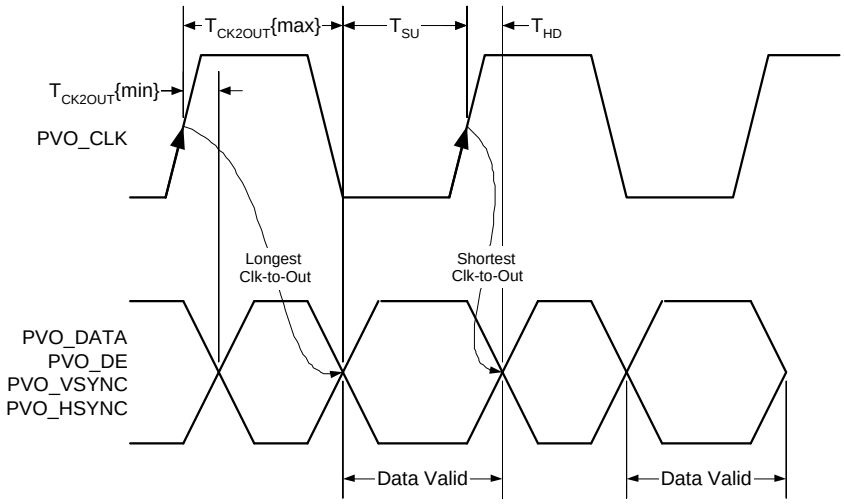


Figure 4.17. Parallel Video Output Setup and Hold Times

Table 4.1 shows the minimum calculated setup and hold times for commonly used PVO_CLK frequencies. The setup and hold times apply to PVO_DE, PVO_VSYNC, PVO_HSYNC, and PVO_Data output pins, with an output load of 10 pF. These are approximations. Hold time is not related to PVO_CLK frequency.

Table 4.1. Calculation of Parallel Video Output Setup and Hold Times

Symbol	Parameter	T_{PVO_CLK}		Min
T_{SU}	Setup Time to PVO_CLK = $T_{PVO\_CLK} - T_{CK2OUT}$\{max\}	27 MHz	37.0 ns	33.1 ns
		74.25 MHz	13.5 ns	9.6 ns
		148.5 MHz	6.73 ns	2.83 ns
T_{HD}	Hold Time from PVO_CLK = T_{CK2OUT}\{min\}	27 MHz	37.0 ns	2.1 ns

4.9. Calculating Setup and Hold Times for I²S Audio Output Bus

Valid serial data is available at T_{SCK2SD} after the falling edge of the first AO_SCK cycle, and then captured downstream using the active rising edge of AO_SCK one clock period later. The setup time of data-to-AO_SCK (T_{SU}) and hold time of AO_SCK-to-data (T_{HD}) are a function of the worst case AO_SCK-to-output data delay (T_{SCK2SD}). Figure 4.10 on page 53 illustrates this timing relationship. Note that the active AO_SCK edge (rising edge) is shown with an arrowhead. For a falling edge sampling clock, the logic is reversed.

Table 4.2 shows the setup and hold time calculation examples for various audio sample frequencies. The setup and hold times for other audio sampling frequencies can also be calculated with the formula used in these examples.

Table 4.2. I²S Setup and Hold Time Calculations

Symbol	Parameter	FWS (kHz)	FSCK (MHz)	T_{TR}(ns)	Min (ns)
T_{SU}	Setup Time, SCK to SD/WS $= T_{TR} - (T_{SCKDUTY\_WORST} + T_{SCK2SD\_MAX})$ $= T_{TR} - (0.6T_{TR} + 5ns)$ $= 0.4T_{TR} - 5ns$	32	2.048	488	190
		44.1	2.822	354	136
		48	3.072	326	125
		96	6.144	163	60
		192	12.288	81	27
T_{HD}	Hold Time, SCK to SD/WS $= (T_{SCKDUTY\_WORST} - T_{SCK2SD\_MIN})$ $= 0.4T_{TR} - 5ns$	32	2.048	488	190
		44.1	2.822	354	136
		48	3.072	326	125
		96	6.144	163	60
		192	12.288	81	27

Note: The sample calculations shown are based on WS = 64 SCK rising edges.

5. Pin Diagram and Pin Descriptions

5.1. Pin Diagram

Figure 5.1 shows the pin assignments of the SiI9616 video processor. Individual pin functions are described in the Pin Descriptions on the next page. The package is a 20 mm x 20 mm 176 pin TQFP, 0.4 mm pitch, with an ePad that must be connected to ground.

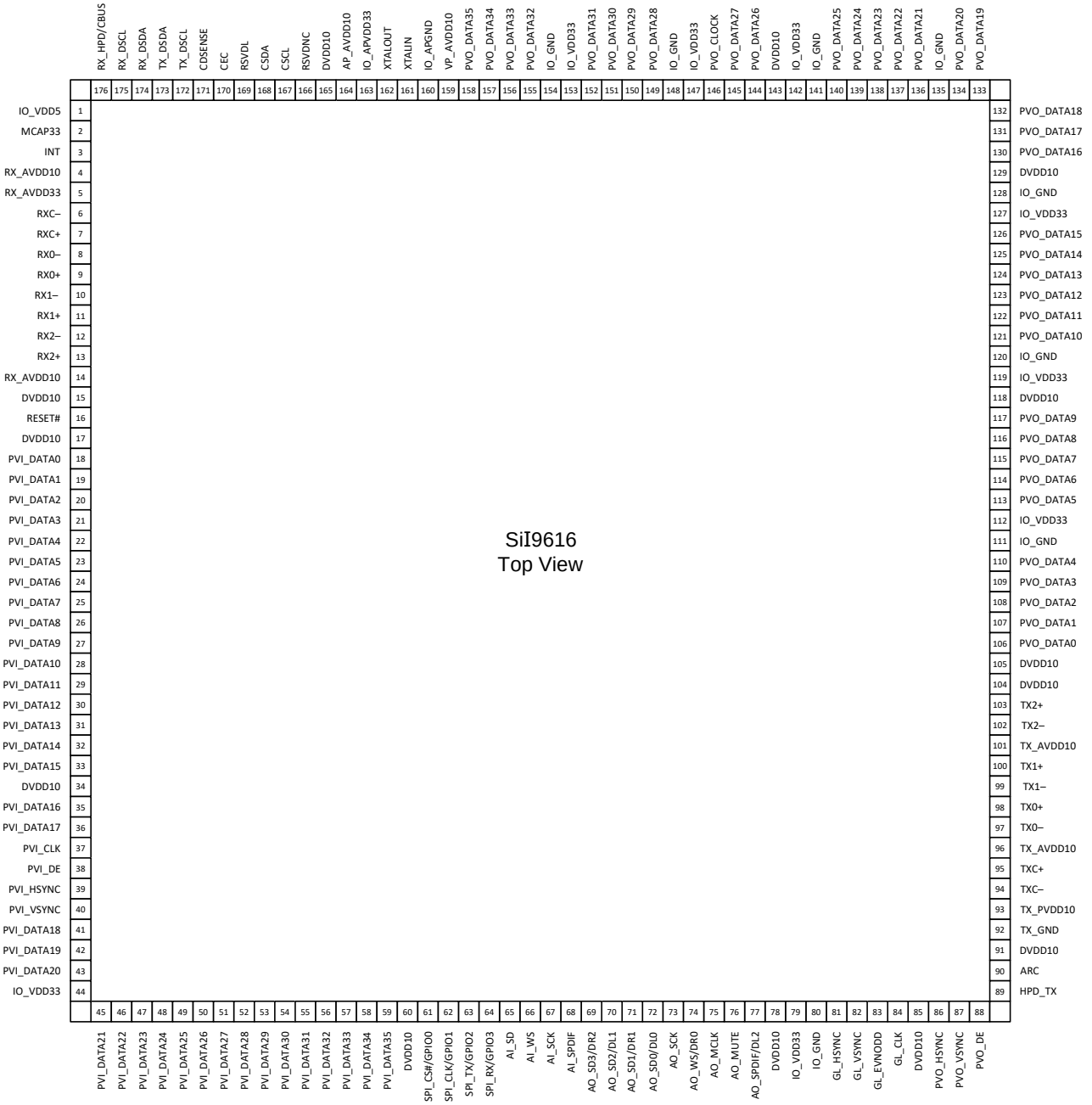


Figure 5.1. Pin Diagram

5.2. Pin Descriptions

5.2.1. Digital Video Input Data Pins

Pin Name	Pin	Type	Dir	Description
PVI_DATA0	18	LVTTL Schmitt 5 V tolerant	Input	36-bit Input Pixel Data Bus. PVI_DATA[35:0] is highly configurable using the various video configuration registers. It supports a wide array of input formats, including multiple RGB and YCbCr bus formats. These pins have a weak internal pull-down resistor.
PVI_DATA1	19			
PVI_DATA2	20			
PVI_DATA3	21			
PVI_DATA4	22			
PVI_DATA5	23			
PVI_DATA6	24			
PVI_DATA7	25			
PVI_DATA8	26			
PVI_DATA9	27			
PVI_DATA10	28			
PVI_DATA11	29			
PVI_DATA12	30			
PVI_DATA13	31			
PVI_DATA14	32			
PVI_DATA15	33			
PVI_DATA16	35			
PVI_DATA17	36			
PVI_DATA18	41			
PVI_DATA19	42			
PVI_DATA20	43			
PVI_DATA21	45			
PVI_DATA22	46			
PVI_DATA23	47			
PVI_DATA24	48			
PVI_DATA25	49			
PVI_DATA26	50			
PVI_DATA27	51			
PVI_DATA28	52			
PVI_DATA29	53			
PVI_DATA30	54			
PVI_DATA31	55			
PVI_DATA32	56			
PVI_DATA33	57			
PVI_DATA34	58			
PVI_DATA35	59			

5.2.2. Digital Video Input Control Pins

Pin Name	Pin	Type	Dir	Description
PVI_CLK	37	LVTTL Schmitt 5 V tolerant	Input	Input Data Clock. This pin has a weak internal pull-down resistor.
PVI_DE	38	LVTTL Schmitt 5 V tolerant	Input	Input Data Enable. This pin has a weak internal pull-down resistor.
PVI_HSYNC	39	LVTTL Schmitt 5 V tolerant	Input	Input Horizontal Sync. This pin has a weak internal pull-down resistor.
PVI_VSYNC	40	LVTTL Schmitt 5 V tolerant	Input	Input Vertical Sync. This pin has a weak internal pull-down resistor.

5.2.3. Digital Video Output Data Pins

Pin Name	Pin	Type	Dir	Description
PVO_DATA0	106	LVTTL 5 V tolerant 8 mA	Output	36-bit Output Pixel Data Bus. PVO_DATA[35:0] is highly configurable using the various video configuration registers. It supports a wide array of output formats, including multiple RGB and YCbCr bus formats. These pins can be floated by register programming. These pins have a weak internal pull-down resistor.
PVO_DATA1	107			
PVO_DATA2	108			
PVO_DATA3	109			
PVO_DATA4	110			
PVO_DATA5	113			
PVO_DATA6	114			
PVO_DATA7	115			
PVO_DATA8	116			
PVO_DATA9	117			
PVO_DATA10	121			
PVO_DATA11	122			
PVO_DATA12	123			
PVO_DATA13	124			
PVO_DATA14	125			
PVO_DATA15	126			
PVO_DATA16	130			
PVO_DATA17	131			
PVO_DATA18	132			
PVO_DATA19	133			
PVO_DATA20	134			
PVO_DATA21	136			
PVO_DATA22	137			
PVO_DATA23	138			
PVO_DATA24	139			
PVO_DATA25	140			
PVO_DATA26	144			
PVO_DATA27	145			
PVO_DATA28	149			
PVO_DATA29	150			
PVO_DATA30	151			
PVO_DATA31	152			
PVO_DATA32	155			
PVO_DATA33	156			
PVO_DATA34	157			
PVO_DATA35	158			

5.2.4. Digital Video Output Control Pins

Pin Name	Pin	Type	Dir	Description
PVO_DE	88	LVTTL 5 V tolerant 8 mA	Output	Data Enable. This pin can be floated by register programming. This pin has a weak internal pull-down resistor.
PVO_HSYNC	86	LVTTL 5 V tolerant 8 mA	Output	Horizontal Sync Output. This pin can be floated by register programming. |This pin has a weak internal pull-down resistor.
PVO_VSYNC	87	LVTTL 5 V tolerant 8 mA	Output	Vertical Sync Output. This pin can be floated by register programming. This pin has a weak internal pull-down resistor.
PVO_CLK	146	LVTTL 5 V tolerant 16 mA	Output	Output Data Clock.

5.2.5. Genlock Pins

Pin Name	Pin	Type	Dir	Description
GL_HSYNC	81	LVTTL 5 V tolerant 8 mA	Output	Genlock HSYNC. This pin has a weak internal pull-down resistor.
GL_VSYNC	82	LVTTL 5 V tolerant 8 mA	Output	Genlock VSYNC. This pin has a weak internal pull-down resistor.
GL_EVNODD	83	LVTTL 5 V tolerant 8 mA	Output	Software configurable as Genlock DE or Genlock Even or Odd Field Indicator for interlaced formats. This pin has a weak internal pull-down resistor.
GL_CLK	84	LVTTL 5 V tolerant 8 mA	Output	Genlock Clock. This pin has a weak internal pull-down resistor.

5.2.6. HDMI Receiver Control Signal Pins

Pin Name	Pin	Type	Dir	Description
RX_DSCL	175	Schmitt Open-drain 5 V tolerant	Input	DDC I^2C Clock for HDMI Receiver Port. HDCP KSV, An, and Ri values are exchanged over an I^2C port during authentication. This pin does not present a current path to GND when the device is not powered. This pin requires an external 47 kΩ pull-up resistor as defined in the HDMI Specification.
RX_DSDA	174	Schmitt Open-drain 5 V tolerant	Input Output	DDC I^2C Data for HDMI Receiver Port. HDCP KSV, An, and Ri values are exchanged over an I^2C port during authentication. This pin does not present a current path to GND when the device is not powered.
RX_HPD/CBUS	176	LVTTL/ CBUS 5 V tolerant	Input Output	Hotplug Output Signal-to-HDMI Connector. In HDMI mode, this is a 5 V signal with 1 kΩ output impedance. It indicates that EDID is readable. In MHL mode, this pin serves as the CBUS signal.
CEC	170	CEC compliant 5 V tolerant	Input Output	HDMI Compliant CEC I/O used to interface to CEC devices. This pin connects to the CEC signal of all HDMI connectors in the system. This pin has an internal pull-up resistor.
CDSENSE	171	LVTTL Schmitt 5 V tolerant	Input	MHL Cable Detect Sense.

5.2.7. HDMI Receiver Differential Signal Data Pins

Pin Name	Pin	Type	Dir	Description
RX0+	9	TMDS Analog	Input	HDMI Port TMDS Input Data Pairs.
RX0–	8			
RX1+	11			
RX1–	10			
RX2+	13			
RX2–	12			
RXC+	7	TMDS Analog	Input	HDMI Port TMDS Input Clock Pair.
RCX–	6			

5.2.8. Digital Audio Output Pins

Pin Name	Pin	Type	Dir	Description
AO_MCLK	75	LVTTL 5 V tolerant 6 mA	Output	Audio Master Clock Output. This pin has a weak internal pull-down resistor.
AO_SCK*	73	LVTTL Schmitt 5 V tolerant 6 mA	Output Input	I²S Serial Clock Output or DSD Clock Output. This pin has a weak internal pull-down resistor.
AO_SD3/DR2*	69	LVTTL Schmitt 5 V tolerant 6 mA	Output Input	I²S Serial Ch3 Data Output/DSD Serial Right Ch2 Data Output.
AO_SD2/DL1*	70			I²S Serial Ch2 Data Output/DSD Serial Left Ch1 Data Output.
AO_SD1/DR1*	71			I²S Serial Ch1 Data Output/DSD Serial Right Ch1 Data Output.
AO_SD0/DL0*	72			I²S Serial Ch0 Data Output/DSD Serial Left Ch0 Data Output. AO_SD[3:0] pins have a weak internal pull-down resistor.
AO_WS/DR0*	74	LVTTL Schmitt 5 V tolerant 6 mA	Output Input	I²S Word Select Output/DSD Serial Right Ch0 Data Output. This pin has weak internal pull-down resistor.
AO_SPDIF/DL2	77	LVTTL Schmitt 5 V tolerant 6 mA	Input	SPI/GPIO Mode Strapping. This pin is an input when the RESET# pin is asserted. On the rising edge of RESET#, the level on this pin is latched and sets the operational mode of the SPI/GPIO pins. LOW – SPI/GPIO pins are used as SPI signals. HIGH – SPI/GPIO pins are used as GPIO signals. This pin has a weak internal pull-down resistor.
			Output	S/PDIF audio output when the device is not in reset.
				DSD Serial Left Channel 2 data output when device is not in reset.
AO_MUTE	76	LVTTL Schmitt 5 V tolerant 6 mA	Input	Local I²C Slave Address Strapping. This pin is an input when the RESET# pin is asserted. On the rising edge of RESET#, the level on this pin is latched and used to set the address of the local I²C interface. LOW – Address 0x30 HIGH – Address 0x32 This pin has a weak internal pull-down resistor.
			Output	Mute Audio Output. This pin becomes the audio mute output when RESET# is inactive. It is used as a signal to the external downstream audio device, audio DAC, etc. to mute audio output.

***Note**: These I²S audio output signals can be reconfigured by software as inputs to support multichannel audio input.

5.2.9. HDMI Transmitter TMDS Output Pins

Pin Name	Pin	Type	Dir	Description
TX0+	98	TMDS Analog	Output	HDMI Transmitter Output Port Data. TMDS LOW voltage differential signal output data pairs.
TX0–	97			
TX1+	100			
TX1–	99			
TX2+	103			
TX2–	102			
TXC+	95	TMDS Analog	Output	HDMI Transmitter Output Port Clock. TMDS LOW voltage differential signal output clock pair.
TXC–	94			

5.2.10. HDMI Transmitter Control Signal Pins

Pin Name	Pin	Type	Dir	Description
HPD_TX	89	LVTTL Schmitt 5 V tolerant	Input	Hot Plug Detect. This pin has a weak internal pull-down resistor.
TX_DSCL	172	Schmitt Open-drain 5 V tolerant	Input Output	DDC I^2C Clock for HDMI Transmitter Port. HDCP KSV, An, and Ri values are exchanged over this I^2C port during authentication. This is a true open-drain, so it does not pull to GND if power is not applied. This pin requires an external pull-up resistor between 1.5 to 2.0 kΩ as defined in the HDMI Specification.
TX_DSDA	173	Schmitt Open-drain 5 V tolerant	Input Output	DDC I^2C Data for HDMI Transmitter Port. HDCP KSV, An, and Ri values are exchanged over this I^2C port during authentication. This is a true open-drain, so it does not pull to GND if power is not applied. This pin requires an external pull-up resistor between 1.5 to 2.0 kΩ as defined in the HDMI Specification.

5.2.11. Audio Input Pins

Pin Name	Pin	Type	Dir	Description
AI_SCK	67	LVTTL Schmitt 5 V tolerant	Input	I^2S Serial Clock Input. This pin has a weak internal pull-down resistor.
AI_WS	66	LVTTL Schmitt 5 V tolerant	Input	I^2S Word Select Input. This pin has a weak internal pull-down resistor.
AI_SD	65	LVTTL Schmitt 5 V tolerant	Input	I^2S Data Input. This pin has a weak internal pull-down resistor.
AI_SPDIF	68	LVTTL Schmitt 5 V tolerant	Input	S/PDIF Input. This pin has a weak internal pull-down resistor.
ARC	90	Analog	Input	Audio Return Channel Input from HDMI. This pin can be left unconnected when not used.

5.2.12. Configuration/Programming Pins

Pin Name	Pin	Type	Dir	Description
INT	3	LVTTL 5 V tolerant 8 mA	Output	Interrupt Output. The INT pin can be programmed to be an open-drain output (default) or a push-pull LVTTL output. The polarity of the INT pin can be set to negative (default) or positive asserted.
RESET#	16	LVTTL Schmitt 5 V tolerant	Input	Reset Pin. Active LOW. This pin has a weak internal pull-down resistor.
CSCL	167	LVTTL Schmitt Open-drain 5 V tolerant	Input	Configuration/Status I^2C Clock. Chip configuration and status are accessed using this I^2C port. This pin requires an external pull-up resistor. A suggested value is 4.7 kΩ or stronger. This pin has a weak internal pull-down resistor.
CSDA	168	LVTTL Schmitt Open-drain 5 V tolerant 8 mA	Input Output	Configuration/Status I^2C Data. Chip configuration and status are accessed using this I^2C port. This pin requires an external pull-up resistor. A suggested value is 4.7 kΩ or stronger. This pin has a weak internal pull-down resistor.
SPI_CS#/GPIO0	61	LVTTL Schmitt 5 V tolerant 8mA	Input	SPI Chip Select. Selected when the AO_SPDIF/DL2 pin is LOW during reset.
			Input Output	GPIO0. Selected when the AO_SPDIF/DL2 pin is HIGH during reset. This pin has a weak internal pull-down resistor.
SPI_CLK/ GPIO1	62	LVTTL Schmitt 5 V tolerant 8mA	Input	SPI Clock. Selected when the AO_SPDIF/DL2 pin is LOW during reset.
			Input Output	GPIO1. Selected when the AO_SPDIF/DL2 pin is HIGH during reset. This pin has a weak internal pull-down resistor.
SPI_TX/GPIO2	63	LVTTL Schmitt 5 V tolerant 8mA	Output	SPI Data Output. Selected when the AO_SPDIF/DL2 pin is LOW during reset.
			Input Output	GPIO2. Selected when the AO_SPDIF/DL2 pin is HIGH during reset. This pin has a weak internal pull-down resistor.
SPI_RX/GPIO3	64	LVTTL Schmitt 5 V tolerant 8mA	Input	SPI Data Input. Selected when the AO_SPDIF/DL2 pin is LOW during reset.
			Input Output	GPIO3. Selected when the AO_SPDIF/DL2 pin is HIGH during reset. This pin has a weak internal pull-down resistor.

5.2.13. Crystal Clock Pins

Pin Name	Pin	Type	Dir	Description
XTALIN	161	5 V tolerant LVTTL	Input	Crystal Clock Input. Generates internal system clock and allows LVTTL input. Frequency required is 26 MHz through 28.5 MHz. 27 MHz frequency is recommended. The system clock is used as the reference clock for the audio PLL and scaler PLL. It is also used for register access and interrupt processing.
XTALOUT	162	LVTTL	Output	Crystal Clock Output.

Note: The XTALIN pin can be driven at LVTTL levels by a clock (leaving XTALOUT unconnected) or connected through a crystal to XTALOUT.

5.2.14. Power and Ground Pins

Pin Name	Pin	Type	Description	Supply
IO_VDD5	1	Power	Power supply for CSCL, CSDA, CEC, CDSENSE, TX_DSCL, TX_DSDA, RX_DSDA, RX_DSCL and RX_HPD/CBUS pins.	5.0 V
MCAP33	2	Power	Capacitor for Internal Regulator.	3.3 V
RX_AVDD10	4, 14	Power	TMDS Rx Analog 1.0 V Power Supply.	1.0 V
RX_AVDD33	5	Power	TMDS Rx Analog 3.3 V Power Supply.	3.3 V
TX_PVDD10	93	Power	TMDS Tx PLL Analog 1.0 V Power Supply.	1.0 V
TX_AVDD10	96, 101	Power	TMDS Tx Analog 1.0 V Power Supply.	1.0 V
DVDD10	15, 17, 34, 60, 78, 85, 91, 104, 105, 118, 129, 143, 165	Power	Digital Logic Power Supply.	1.0 V
VP_AVDD10	159	Power	Video PLL Power Supply.	1.0 V
AP_AVDD10	164	Power	Audio PLL Power Supply.	1.0 V
IO_VDD33	44, 79, 112, 119, 127, 142, 147, 153	Power	I/O Power Supply.	3.3 V
IO_APVDD33	163	Power	Audio PLL I/O Power Supply.	3.3 V
TX_GND	92	Ground	TMDS Tx Ground.	Ground
IO_APGND	160	Ground	Audio PLL I/O Ground.	Ground
IO_GND	80, 111, 120, 128, 135, 141, 148, 154	Ground	I/O Ground.	Ground
GND	ePad (bottom of package)	Ground	Ground. The ePad ***must*** be soldered to ground.	Ground

5.2.15. Reserved Pins

Pin Name	Pin	Type	Description	Supply
RSVDNC	166	Reserved	Do not connect.	—
RSVDL	169	Reserved	Reserved. Must be tied to ground.	Ground

6. Feature Information

6.1. I²C and SPI Interfaces

6.1.1. E-DDC/I²C Interface

The HDCP protocol requires the video transmitter and video receiver to exchange values. The transmitter reads the EDID data in the receiver to ascertain its capabilities. These values are exchanged over the DDC channel of the HDMI interface. The E-DDC channel follows the I²C serial protocol. Both the HDMI receiver and transmitter ports of the SiI9616 device feature their own separate E-DDC buses.

6.1.1.1. HDMI Receiver E-DDC Interface

The HDMI receiver port of the SiI9616 device has a connection to the E-DDC bus with the slave address of 0x74 for HDCP authentication, and 0xA0 for EDID data retrieval by the upstream transmitter. The I²C read operation is shown in Figure 6.1, and the write operation in Figure 6.2.

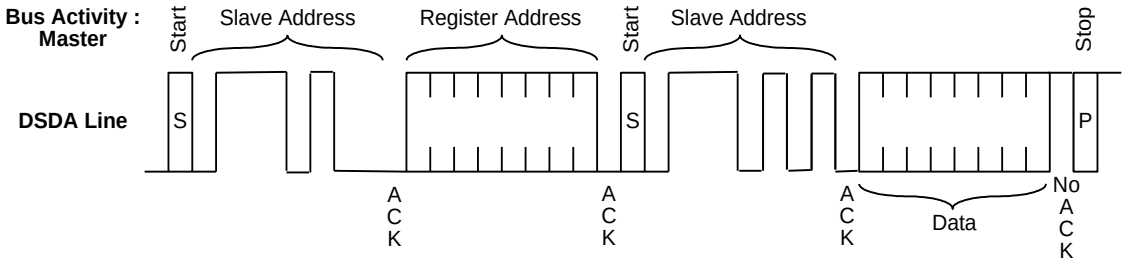


Figure 6.1. DDC Byte Read

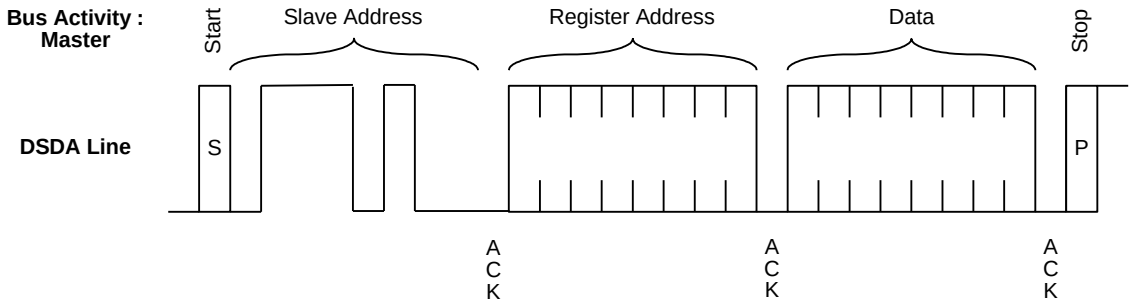


Figure 6.2. DDC Byte Write

Multiple bytes can be transferred in each transaction, regardless of whether they are reads or writes. The operations are similar to those in the two figures above, except that there is more than one data phase. An ACK follows each byte except the last byte in a read operation. Byte addresses increase with the least-significant byte transferred first, and the most-significant byte last. See the I²C Specification for more information.

There is also a Short Read format that can be performed during the third phase of HDCP authentication. It is designed to improve the efficiency of Ri register reads that must be done every two seconds while encryption is enabled. Figure 6.3 on the next page shows this transaction. There is no register address phase (only the slave address phase), because the register address is reset to 0x08 (Ri) after a hardware or software reset, and after the STOP condition on any preceding I²C transaction.

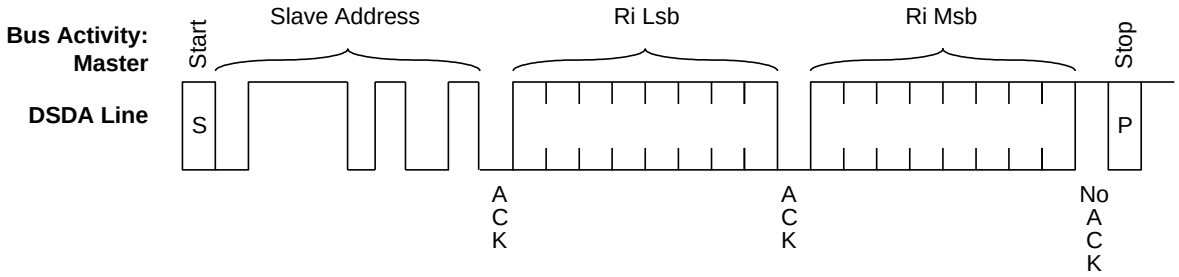


Figure 6.3. Short Read Sequence

6.1.1.2. HDMI Transmitter E-DDC Interface

The SiI9616 HDMI transmitter port interfaces with the E-DDC bus through an I²C master controller. The DDC master supports the I²C transactions specified by the VESA Enhanced Display Data Channel Standard. The DDC master complies with the 100 kHz standard mode timing of the I²C Specification and supports slave clock stretching, as required by E-DDC. Figure 6.4 shows the supported transactions and timing sequences.

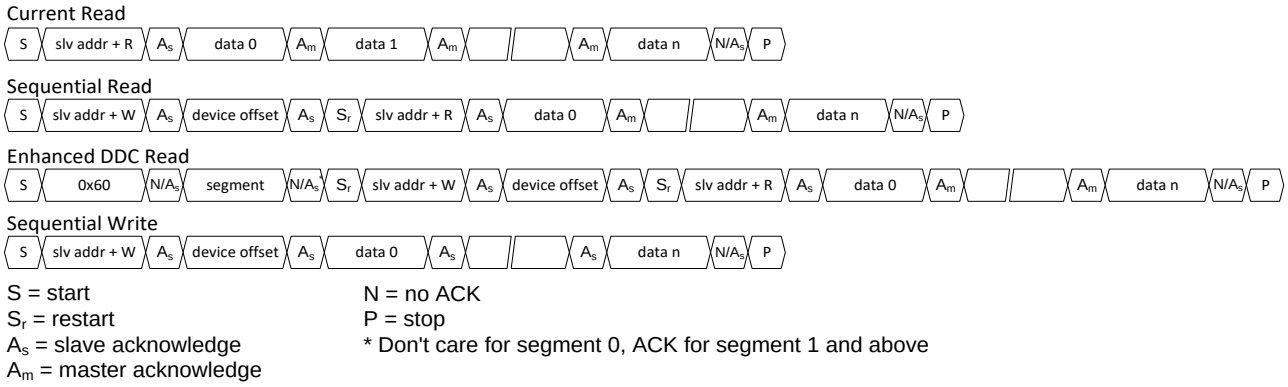


Figure 6.4. DDC Master I²C Supported Transactions

6.1.2. Local I²C Interface

The SiI9616 video processor has a third I²C port accessible only to the controller in the display device. It is separate from the E-DDC bus and is a slave device. The local I²C interface on SiI9616 pins CSCL and CSDA is a slave interface that can run up to 400 kHz. This bus is used to configure and control the video processor by reading and writing to necessary registers.

The device registers are accessed using 16-bit addresses. Figure 6.5 on the next page illustrates the bus activity on the CSDA line when writing to a device register, and Figure 6.6 on the next page illustrates the same when reading a device register. In both read and write cycles, after the master transmits the device address and receives an acknowledgment from the slave, it sends two bytes, which represent the address of the register it wants to read or write. These two bytes make up the high and low bytes of the register address. The rest of the bus cycle follows the same format as transactions using an 8-bit register address.

For example, to write to register 0x1008 of the HDMI receiver, the master would transmit 0x10 for the high address byte and 0x08 for the low address byte.

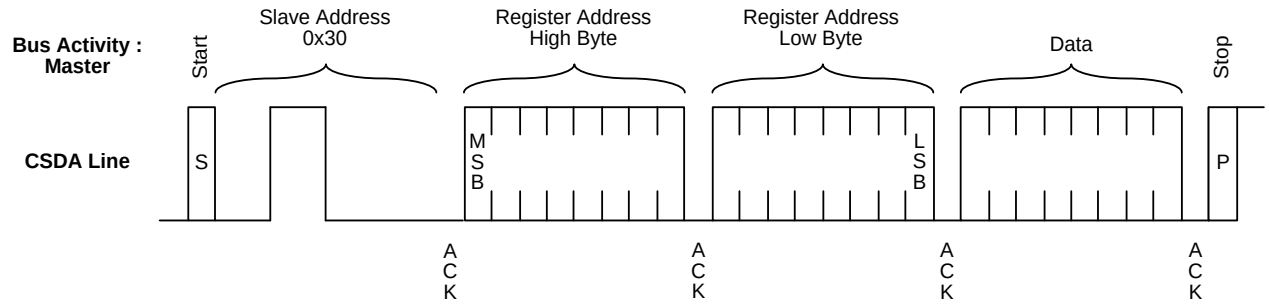


Figure 6.5. Register Write Cycle on Local I²C

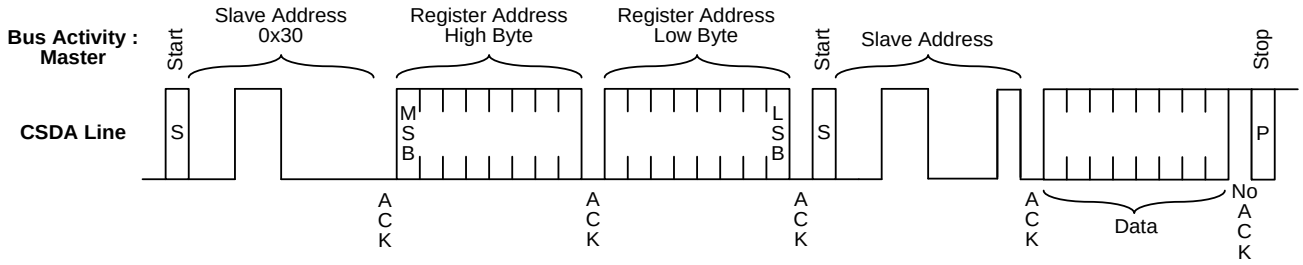


Figure 6.6. Register Read Cycle on Local I²C

Multibyte transfers are supported. The operations are similar to those described above. The internal address pointer is advanced automatically after every transfer of a byte.

The device address of the local I²C interface can be set to one of two values by strapping the AO_MUTE pin LOW or HIGH at reset. Table 6.1 shows the device address selected for each state of the AO_MUTE pin at reset.

Table 6.1. Control of Local I²C Device Address with AO_MUTE Pin

Device Address	AO_MUTE = LOW	AO_MUTE = HIGH
Local I²C	0x30	0x32

6.1.3. Video Requirement for I²C Access

The SiI9616 video processor does not require an active video clock to access its registers from either the E-DDC port or the local I²C port. Read/Write registers can be written and then read back. Read-only registers that provide values for an active video or audio stream return indeterminate values if there is no video clock and no active sync. Use the SCDT and CKDT register bits to determine when active video is being received by the chip.

6.1.4. Local SPI Serial Interface

The SPI serial interface is a simple four-wire synchronous serial interface with unidirectional data lines. The host CPU drives clock, chip select, and serial transmit data to the SPI slave device. It also receives serial data from the SPI slave device. By using multiple chip-enables and tying the receive data lines together, it is possible to connect multiple SPI slave devices to a single host CPU as shown in Figure 6.7 and Figure 6.8 on the next page.

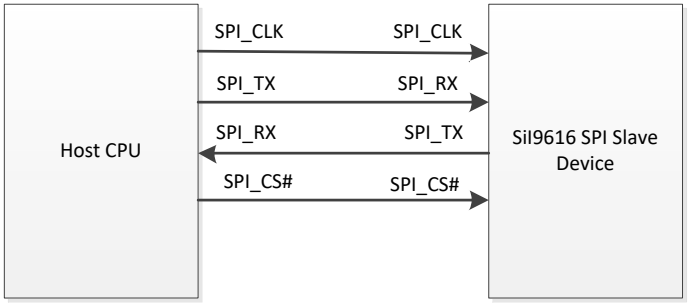


Figure 6.7. SPI Serial Connection Example: Host ↔ Single SPI Slave Device

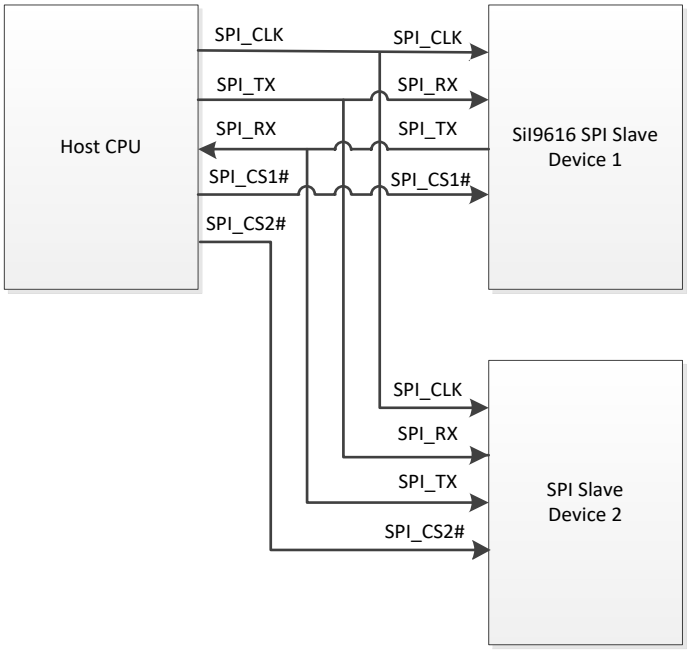


Figure 6.8. SPI Serial Connection Example: Host ↔ Dual SPI Slave Devices

Note: The maximum clock frequency is 10 MHz.

6.1.4.1. Write Operation

The following description of a write operation is from the perspective of the host controller as shown in Figure 6.9 on the next page.

First, the host CPU asserts the SPI_CS# line LOW to indicate the start of a transfer. Then it sends 15 address bits (MSB first) on the SPI_TX line, followed by a single R/W bit (0 = write). For a write operation, the host CPU sends *N* bytes of write data one byte at a time (MSB first). The order of bits on the SPI_TX line is 7…0, 15…8, 23…16, and so on. When more than one byte is written, the address is incremented automatically in the SPI slave device. The maximum number of bytes that may be written in a single transaction is not limited by the bus protocol, but may be limited by the slave device.

At the end of the transaction, SPI_CS# is deasserted to indicate the end of the transfer. If SPI_CS# is deasserted too early, the slave device aborts the transfer and the results may be undefined.

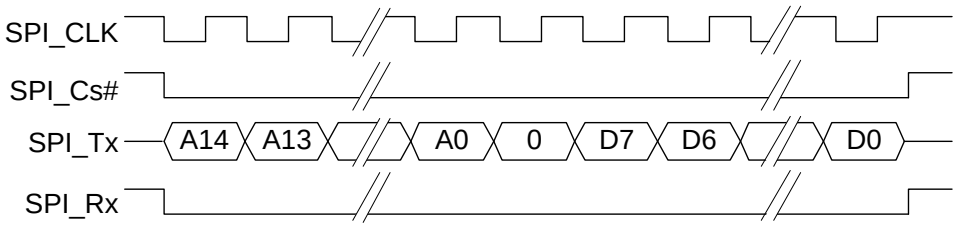


Figure 6.9. SPI Serial Write Operation

Note: Signal names as seen at the host side of the interface.

6.1.5. Read Operation

The following description of a read operation is from the perspective of the host controller as shown in Figure 6.10 below.

First, the host CPU asserts the SPI_CS# line LOW to indicate the start of a transfer. Then it sends 15 address bits (MSB first) on the SPI_TX line, followed by a single R/W bit (1 = read). For a read operation, the host CPU must poll the SPI_RX line while holding the clock pin HIGH, until the slave device drives the SPI_RX line HIGH to indicate data is ready. The host may then start reading *N* bytes of data one byte at a time (MSB first). The order of bits on the serial line is 7…0, 15…8, 23…16, and so on.

Similar to the write operation, when more than one byte is read, the address is incremented automatically in the SPI slave device. The maximum number of bytes that may be read in a single transaction is not limited by the bus protocol, but may be limited by the slave device. Note that the serial clock does not toggle in the pause between sending the address and receiving read data. At the end of the transaction, SPI_CS# is deasserted to indicate the end of the transfer. If SPI_CS# is deasserted too early, the slave device aborts the transfer, and the results may be undefined.

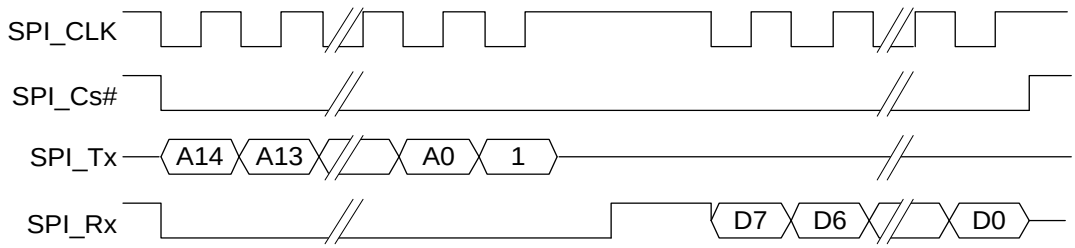


Figure 6.10. SPI Serial Read Operation

Note: Signal names as seen at the host side of the interface.

7. Package Information

7.1. ePad Requirements

The SiI9616 video processor is packaged in a 176-pin, 20 mm x 20 mm TQFP package with an exposed pad (ePad) that is used for the electrical ground of the device and for improved thermal transfer characteristics. The ePad dimensions are 6 mm x 6 mm ± 0.15 mm. Soldering the ePad to the ground plane of the PCB is required to meet package power dissipation requirements at full-speed operation, and to correctly connect the chip circuitry to electrical ground. To avoid the possibility of electrical shorts, a clearance of at least 0.25 mm should be designed on the PCB between the edge of the ePad and the inner edges of the lead pads.

The thermal land area on the PCB may use thermal vias to improve heat removal from the package. These thermal vias also double as the ground connections of the chip and must attach internally in the PCB to the ground plane. An array of vias should be designed into the PCB beneath the package. For optimum thermal performance, the via diameter should be 12 mils to 13 mils (0.30 mm to 0.33 mm) and the via barrel should be plated with 1-ounce copper to plug the via. This design helps to avoid any solder wicking inside the via during the soldering process, which may result in voids in solder between the pad and the thermal land. If the copper plating does not plug the vias, the thermal vias can be tented with solder mask on the top surface of the PCB to avoid solder wicking inside the via during assembly. The solder mask diameter should be at least 4 mils (0.1 mm) larger than the via diameter.

Package standoff when mounting the device also needs to be considered. For a nominal standoff of approximately 0.1 mm, the stencil thickness of 5 mils to 8 mils should provide a good solder joint between the ePad and the thermal land.

Figure 7.1 on the next page shows the package dimensions of the SiI9616 video processor.

7.2. PCB Layout Guidelines

Refer to Lattice Semiconductor document *PCB Layout Guidelines: Designing with Exposed Pads* (refer to Lattice Semiconductor Documents on page 75) for basic PCB design guidelines when designing with thermally enhanced packages using the exposed pad. This application note is intended for use by PCB layout designers.

7.3. Package Dimensions

This figure is not to scale.

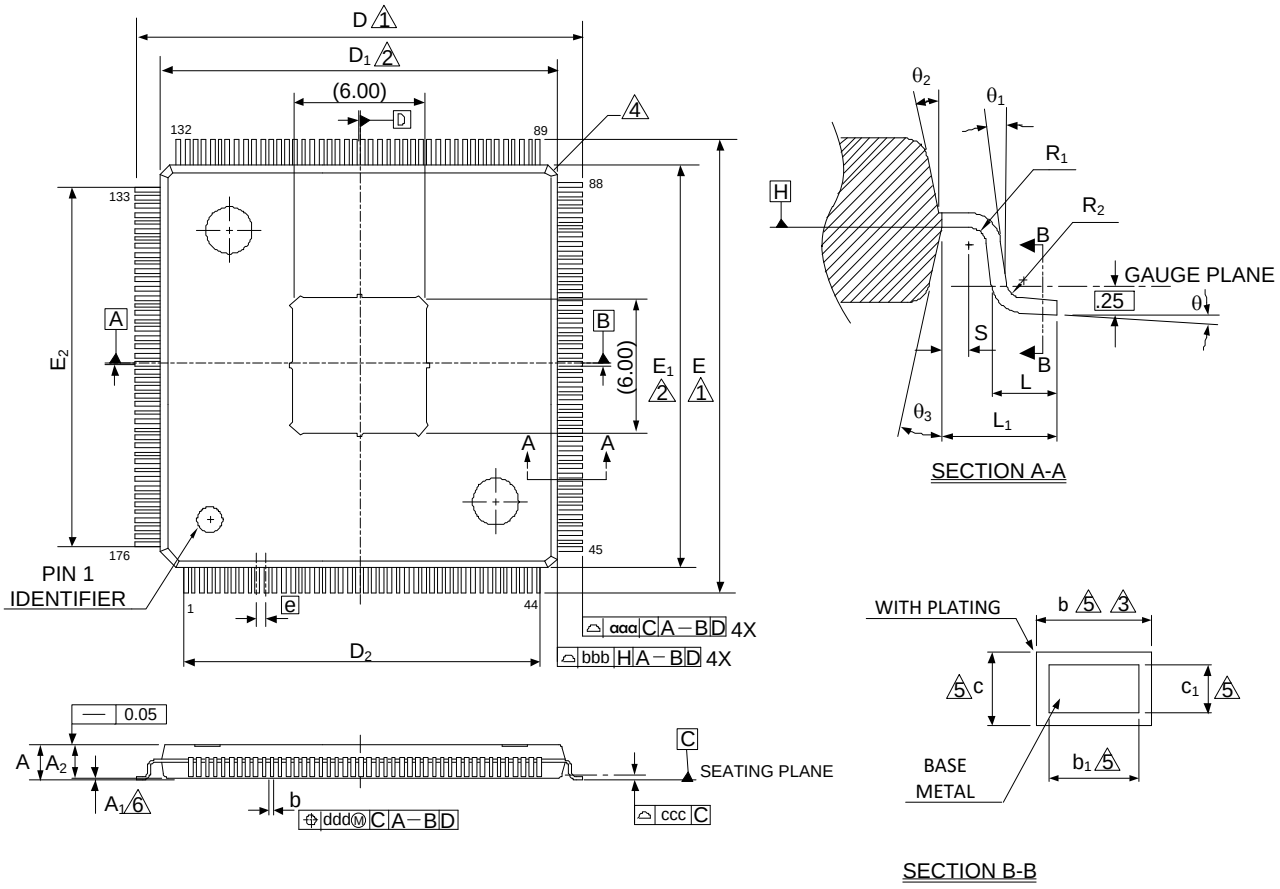


Figure 7.1. Package Diagram

Notes:

1. To be determined at seating plane C.
2. Dimensions D_1 and E_1 do not include mold protrusion D_1 and E_1 are maximum plastic body size dimensions including mold mismatch.
3. Dimension b does not include Dambar protrusion. cannot be located on the lower radius or the foot.
4. Exact shape of each corner is optional.
5. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
6. A_1 is defined as the distance from the seating plane to the lowest point of the package body.

JEDEC Package Code MS-026

Item	Description	Dimension in mm			Item	Description	Dimension in mm		
		Min	Typ	Max			Min	Typ	Max
A	Thickness	1.00	1.10	1.20	L	Lead foot length	0.45	0.60	0.75
A_1	Stand-off	0.05	0.10	0.15	L_1	Total lead length	1.00 REF		
A_2	Body thickness	0.95	1.00	1.05	R_1	Lead radius, inside	0.08	—	—
b	Lead width (with plating)	0.13	0.18	0.23	R_2	Lead radius, outside	0.08	—	0.20
b_1	Lead width (base metal)	0.13	0.16	0.19	S	Lead horizontal run	0.20	—	—
c	Lead thickness (with plating)	0.09	—	0.20	Θ		0°	3.5°	7°
c_1	Lead thickness (base metal)	0.09	—	0.16	$Θ_1$		0°	—	—
D	Footprint	22.00 BSC			$Θ_2$		11°	12°	13°
D_1	Body size	20.00 BSC			$Θ_3$		11°	12°	13°
D_2		17.20 BSC			aaa		0.20		
E	Footprint	22.00 BSC			bbb		0.20		
E_1	Body size	20.00 BSC			ccc		0.08		
E_2		17.20 BSC			ddd		0.07		
e	Lead pitch	0.40 BSC							

7.4. Marking Specification

Figure 7.2 shows the markings of the SiI9616 package. Refer to Figure 7.1 on page 72 for specifics.

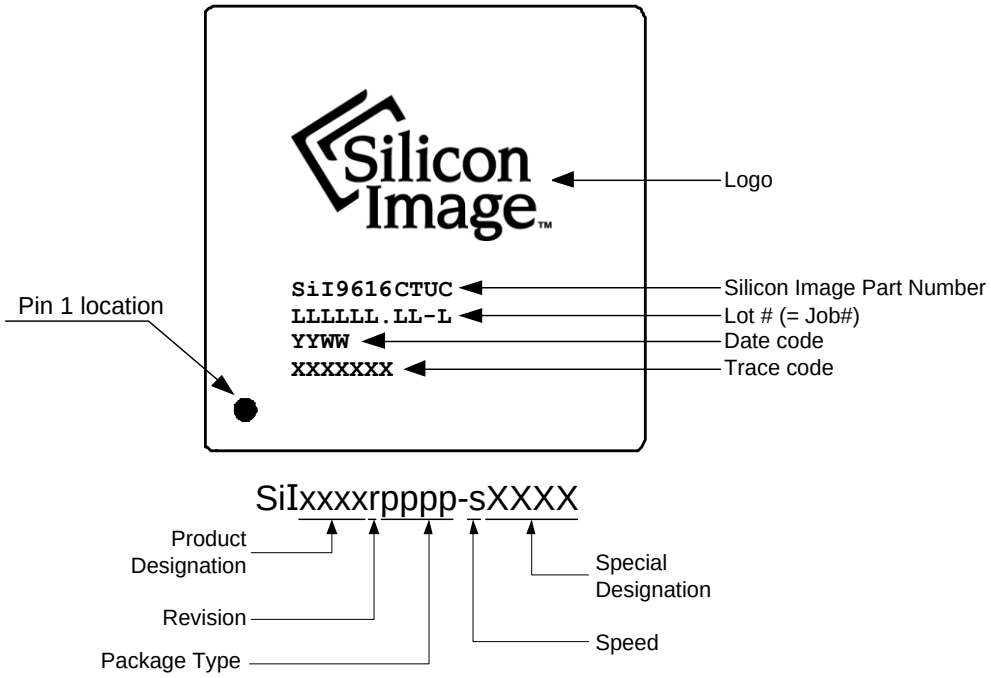


Figure 7.2. Marking Diagram

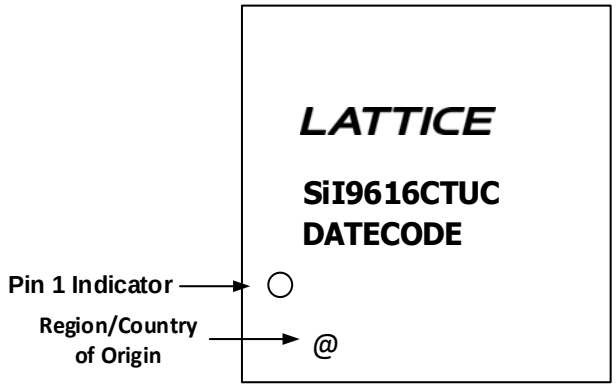


Figure 7.3. Alternate Marking Diagram

7.5. Ordering Information

Production Part Numbers:

TMDS Clock Range	Part Number
25 MHz – 300 MHz	SiI9616CTUC

The universal package may be used in lead-free and ordinary process lines.

References

Standards Documents

This is a list of standards abbreviations appearing in this document, and references to their respective specifications documents.

Abbreviation	Standards publication, organization, and date
HDMI	*High Definition Multimedia Interface,* Revision 1.4, HDMI Consortium; June 2009
HCTS	*HDMI Compliance Test Specification,* Revision 1.3c, HDMI Consortium; July 2008
HDCP	*High-bandwidth Digital Content Protection,* Revision 1.3, Digital-Content Protection, LLC; December 2006
E-EDID	*Enhanced Extended Display Identification Data Standard,* Release A Revision 1, VESA; February 2000
E-DID IG	*VESA EDID Implementation Guide*, VESA; June 2001.
CEA-861	*A DTV Profile for Uncompressed High Speed Digital Interfaces,* EIA/CEA; January 2001
CEA-861-B	*A DTV Profile for Uncompressed High Speed Digital Interfaces*, Draft 020328, EIA/CEA; March 2002
CEA-861-D	*A DTV Profile for Uncompressed High Speed Digital Interfaces,* EIA/CEA; July 2006
EDDC	*Enhanced Display Data Channel Standard,* Version 1.1, VESA; March 2004

Standards Groups

For information on the specifications that apply to this document, contact the responsible standards groups appearing on this list.

Standards Group	Web URL
ANSI/EIA/CEA	http://global.ihs.com
VESA	http://www.vesa.org
DVI	http://www.ddwg.org
HDCP	http://www.digital-cp.com
HDMI	http://www.hdmi.org

Lattice Semiconductor Documents

This is a list of the related documents that are available from your Lattice Semiconductor sales representative. *The Programmer's Reference requires an NDA with Lattice Semiconductor.*

Document	Title
SiI-PR-1069	*SiI9616/ SiI9612 Programmer's Reference*
SiI-PR-0041	*CEC Programming Interface (CPI) Programmer's Reference*
SiI-AN-0129	*PCB Layout Guidelines: Designing with Exposed Pads*

Technical Support

For assistance, submit a technical support case at www.latticesemi.com/techsupport.

Revision History

Revision B, June 2017

Figure 7.3. Alternate Marking Diagram added per PCN13A16

Revision A, February 2016

Updated to latest template.

Revision A, February 2013

First production release.

7th Floor, 111 SW 5th Avenue
Portland, OR 97204, USA
T 503.268.8000
www.latticesemi.com