LatticeMico Fault Logger

The LatticeMico Fault Logger IP allows the user's design to store Analog Sense and Control (ASC) RDAT (read data) to FLASH based upon user defined trigger criteria. It does this by continuously buffering RDAT information in FPGA memory, then sending that information to FLASH when the user defined trigger is asserted.

The Lattice IP offers two different ways to do fault logging:

- Smaller designs and fewer FPGA resources can use the fault logging function that is embedded on the ASC device.
- Larger designs that need features such as timestamp or user data logging can use the fault logger IP described here.

For more information refer to the Platform Designer documentation in Diamond online help.

Version

This document describes the 1.2 version of the LatticeMico Fault Logger.

Features

The LatticeMico Fault Logger IP must be used together with the Embedded Functional Block (EFB) of the MachXO2/Platform Manager 2 device or the Soft-EFB of other devices, and has the following features to support the fault logging task

- RDAT frame buffering for any number of ASC's.

- Writes fault log snapshot to either MachXO2/Platform Manager 2 embedded User Flash Memory (UFM) or to an external FLASH memory.
- User defined trigger (to start the write-to-FLASH operation).
- Maskable interrupt, set by the user defined trigger.
- WISHBONE slave interface to LatticeMico8 microcontroller.
- Storage of FLASH related opcodes.
- Four bytes of additional storage for user-defined data.
- Optional internal or external time stamp.
- All data is register-mapped and accessible by the LatticeMico8 microcontroller from the WISHBONE bus.
- Configurable to use either EBR or distributed RAM.
- Fault Record Counter function for ECP5 devices.
- External SPI Flash memory error flag signal on ECP5 devices.

Functional Description

Refer to Figure 1 on page 3. The fault logger IP continuously buffers RDAT frames into FPGA memory during normal operation. When it receives a trigger from the user logic (typically Logibuilder logic), the fault logger IP will suspend RDAT frame buffering and asserts a LatticeMico8 microcontroller interrupt. The LatticeMico8 microcontroller will then read the fault log snapshot via WISHBONE byte reads and write the data to FLASH. When the entire fault log is stored to FLASH, the LatticeMico8 microcontroller will clear the fault log IP interrupt and the fault logger IP will resume normal operation.

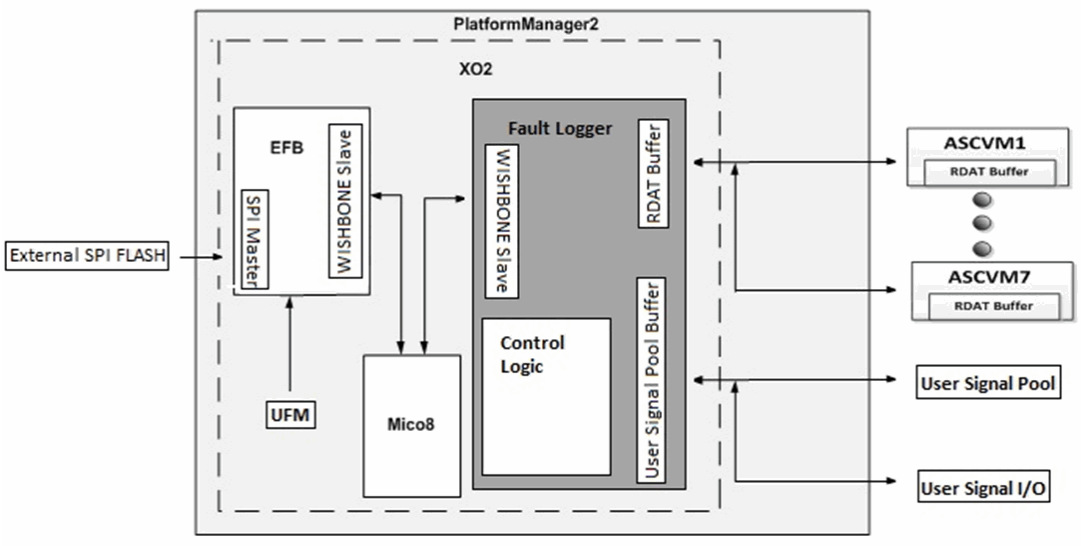
The fault logger can be configured to buffer between one and eight RDAT frames at a time, depending on user choice. A new RDAT frame is presented to the fault logger IP once every 16 µs by the ASCVM. The RDAT data for all logged ASC's is presented to the fault logger at the same time, but on separate interfaces. Malformed RDAT frames (CRC errors) are filtered out by the ASCVM and are not presented to the fault logger.

Fault Log Triggering

The fault log trigger is an input from the user signal pool and should be connected by the user. A rising edge on this signal (usp_trigger_i) constitutes a "trigger event". This will suspend all data buffering and will cause a fault logger interrupt to be sent to the LatticeMico8 microcontroller. The fault logger IP will also assert a busy signal output (usp_busy_o) to indicate that the fault log is being stored to FLASH and that it will ignore all trigger events until the LatticeMico8 microcontroller clears the fault logger IP interrupt.

The designer can select which user signal pool node will be connected to the trigger signal. The signal should be a registered node to keep it synchronous to the Fault Logger IP synchronous logic.

Figure 1: Fault Logger Block Diagram



User Log Storage

Users can store 4 bytes of user signal pool data in the fault log. These fault logger inputs are buffered into FPGA memory once every 4 µs and will be included as part of the fault log written to FLASH. Buffering of these signals is suspended while usp_busy_o is asserted.

The designer can enable user log bytes and select which design signals will be connected to the user log inputs.

The user log bytes are WISHBONE register readable and are included as part of the fault log written to FLASH. Refer to “Fault Log Mapping Table” on page 4 to see where these signals reside in a fault log map. Refer to “ASC Fault Log Record Memory Map” on page 5 when ASC is configured for Fault Log Mode. More information about how to configure the user log bytes refer to Platform Designer documentation in Lattice Diamond online help.

Timestamp Function

The user may optionally include an internal timestamp function that logs the number of seconds since the last reset of the MachXO2/Platform Manager 2/ ECP5. The timestamp counts up to 10 years and will not roll over. It is WISHBONE register readable and is included as part of the fault log written to FLASH. This internal timestamp function can only be included if parameters have been set with `FAULTLOGGER_TIMESTAMP_ENABLED=1` and `FAULTLOGGER_EXTTIMESTAMP_ENABLED=0`.

The user can also provide an external time stamp to configure Fault Logger IP. When doing so, the user must also provide an additional input timestamp signal to the usp_timestamp_i port and set

FAULTLOGGER_TIMESTAMP_ENABLED=1 and FAULTLOGGER_EXTTIMESTAMP_ENABLED=1.

Please see the Fault Log Mapping Table (generated by Platform Designer) to see where the timestamp resides in a fault log map, or see Platform Designer for information about how to enable the timestamp option.

Please see “Configuration Parameters” for more information about the fault log timestamp.

Fault Log Mapping Table

Table 1 is the Fault Log Map. The length of the fault log will vary with differing user configurations. For example, a fault log that logs three ASCs will be shorter than a fault log that includes eight ASCs. The location of similar data within a fault log will also change with differing configurations. For example, the address of the timestamp will be at a lower address location in a fault log with two ASCs than if the fault log includes seven ASCs. When using the External SPI Flash mode, each Fault Log will be mapped to 128 bytes to match the SPI Flash memory page limitation.

Platform Designer provides an ASCII based, Fault Log Mapping Table file to tell the user where individual RDAT bits and user log and timestamp bytes are for a given Fault Logger IP configuration. Please refer to the Platform Designer documentation in the Diamond online help for the usage and location of this automatically generated document.

Table 1: Fault Log Map

Element Number	Name	Number of Bytes	Required/ Optional	Description
0	HEADER	1	Required	The fault flag is the first byte of FLASH storage map. 0x3C in this location indicates that there is a fault log snapshot stored in this FLASH page. This flag is not stored in the fault logger IP, but is inserted by LatticeMico8 microcontroller.
1	LENGTH	1	Required	Total number of bytes in the storage element map. This value will be calculated by software at startup and then stored in parameter FAULT_LOG_LENGTH.
2	ASC0 RDAT	7	Required	This is the RDAT frame from ASC0. The contents of this element will be the same contents and ordering of the data within a 3WI RDAT frame.
3	ASC1 RDAT	7	Optional.	Same as ASC0 RDATA element, except that inclusion depends on parameter FAULTLOGGER_ASC_LOG_CNT >= 2.
4	ASC2 RDAT	7	Optional.	Same as ASC0 RDATA element, except that inclusion depends parameter FAULTLOGGER_ASC_LOG_CNT >= 3.
5	ASC3 RDAT	7	Optional.	Same as ASC0 RDATA element, except that inclusion depends parameter FAULTLOGGER_ASC_LOG_CNT >= 4.
6	ASC4 RDAT	7	Optional.	Same as ASC0 RDATA element, except that inclusion depends parameter FAULTLOGGER_ASC_LOG_CNT >= 5.

Table 1: Fault Log Map (Continued)

Element Number	Name	Number of Bytes	Required/ Optional	Description
7	ASC5 RDAT	7	Optional.	Same as ASC0 RDATA element, except that inclusion depends parameter FAULTLOGGER_ASC_LOG_CNT >= 6.
8	ASC6 RDAT	7	Optional.	Same as ASC0 RDATA element, except that inclusion depends parameter FAULTLOGGER_ASC_LOG_CNT >= 7.
9	ASC7 RDAT	7	Optional.	Same as ASC0 RDATA element, except that inclusion depends parameter FAULTLOGGER_ASC_LOG_CNT >= 8.
10	USER0	1	Required.	First byte of user log data and corresponds to signal USP_USRLOG0_I.
11	USER1	1	Required.	Second byte of user log data and corresponds to signal USP_USRLOG1_I.
12	USER2	1	Required.	Third byte of user log data and corresponds to signal USP_USRLOG2_I.
13	USER3	1	Required.	Fourth byte of user log data and corresponds to signal USP_USRLOG3_I.
14	TIME	4	Optional	Timestamp. Indicates distance since last power on reset. Only included if parameter FAULTLOGGER_TIMESTAMP_ENABLED=1.
15	FOOTER	1	Required	End delimiter. Value is always 0x2A. Not stored in fault logger IP. This flag is not stored in the fault logger IP, but is inserted by LatticeMico8 microcontroller.

ASC Fault Log Record Memory Map

Table 2 is the ASC fault log record memory map. When the ASC is configured for Fault Log Mode, the memory block is used to record the status of the ASC GPIOs, VMON, IMON, TMON and other significant logic signals on the occurrence of the user defined fault trigger condition.

Each fault record has seven bytes: six bytes of ASC specific data and one byte of user specified FPGA signals.

Table 2: ASC Fault Log Record Memory Map

Byte	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	0	1	1	1	1	0	0
1	0	0	0	1	0	0	0	1
2	FL_FULL	FL_ACT	0	0	1	EE_DONE	1	AGOOD
3	AGOOD	RGPIO10	RGPIO9	RGPIO8	RGPIO7	RGPIO6	RGPIO5	RGPIO4
4	RGPIO3	RGPIO2	RGPIO1	RHVOUT4	RHVOUT3	RHVOUT2	RHVOUT1	IMON_1B
5	IMON_1A	HIMONB	HIMONA	HVMONB	HVMONA	VMON_9B	VMON_9A	VMON_8B

Table 2: ASC Fault Log Record Memory Map

Byte	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
6	VMON_8A	VMON_7B	VMON_7A	VMON_6B	VMON_6A	VMON_5B	VMON_5A	VMON_4B
7	VMON_4A	VMON_3B	VMON_3A	VMON_2B	VMON_2A	VMON_1B	VMON_1A	TMON_2B
8	TMON_2A	TMON_1B	TMON_1A	TMonInt_B	TMonInt_A	1	0	1
9	USR0[7]	USR0[6]	USR0[5]	USR0[4]	USR0[3]	USR0[2]	USR0[1]	USR0[0]
10	USR1[7]	USR1[6]	USR1[5]	USR1[4]	USR1[3]	USR1[2]	USR1[1]	USR1[0]
11	USR2[7]	USR2[6]	USR2[5]	USR2[4]	USR2[3]	USR2[2]	USR2[1]	USR2[0]
12	USR3[7]	USR3[6]	USR3[5]	USR3[4]	USR3[3]	USR3[2]	USR3[1]	USR3[0]
13	Timer[31]	Timer[30]	Timer[29]	Timer[28]	Timer[27]	Timer[26]	Timer[25]	Timer[24]
14	Timer[23]	Timer[22]	Timer[21]	Timer[20]	Timer[19]	Timer[18]	Timer[17]	Timer[16]
15	Timer[15]	Timer[14]	Timer[13]	Timer[12]	Timer[11]	Timer[10]	Timer[9]	Timer[8]
16	Timer[7]	Timer[6]	Timer[5]	Timer[4]	Timer[3]	Timer[2]	Timer[1]	Timer[0]
17	0	0	1	0	1	0	1	0

Configuration

The following sections describe the graphical user interface (UI) parameters, the hardware description language (HDL) parameters, and the I/O ports that user can use to configure and operate the LatticeMico Fault Logger. For more information refer to the Platform Designer documentation in Diamond online help.

UI Parameters

Table 3 shows the UI parameters available for configuring the LatticeMico Fault Logger through the Mico System Builder (MSB) interface.

Table 3: Fault Logger UI Parameters

Dialog Box Options	Description	Allowable Values	Default Value
Instance Name	Specifies the name of the Fault Logger instance	Alphanumeric and underscores	faultlogger
Lattice Family	Specifies the device family name	MachXO2, LPTM2, ECP5U, ECP5UM	MachXO2
Base Address	Specifies the base address for configuring the Fault Logger. The minimum boundary alignment is 0x80.	0X80000000–0XFFFFFFFF	0X80000000

SPI/I^{2}C Connecting Module Setting

Table 3: Fault Logger UI Parameters (Continued)

Dialog Box Options	Description	Allowable Values	Default Value
Use Harden EFB	Select this option to use Harden EFB	selected | not selected	selected
Use Soft EFB	Select this option to use Soft EFB	selected | not selected	not selected
Fault Logger Setting			
External Time Stamp Enable	Select this option to enable External Time Stamp. Can only be enabled when Use Soft EFB is selected.	selected | not selected	not selected
Internal Time Stamp Enable	Select this option to enable Internal Time Stamp. Can only be enabled when External Time Stamp Enable is not selected.	selected | not selected	selected
Number of ASC Log	Specifies the number of ASC Log	1 – 8	1
Number of User Log	Specifies the number of User Log	0 – 4	0
Use USER MCLK Macro	Select this option to enable the ECP5's USERMCLK macro. Can only be enabled when Use Soft EFB is selected.	selected | not selected	not selected
RDAT Storage Setting			
Distributed RAM	When selected, RDAT data will be stored in Distributed RAM	selected | not selected	selected
EBR	When selected, RDAT data will be stored in EBR	selected | not selected	not selected
Flash Memory Setting			
Flash Mode			
Maximum Memory Storage	Specifies the number of bytes in the external Flash Storage	0- 268435456	100
User Flash Memory	When selected, fault log data will be stored in User Flash Memory	selected | not selected	selected
External SPI Flash	When selected, fault log data will be stored in external SPI Flash	selected | not selected	not selected
Starting Address of SPI Flash for Log Data	Specifies the starting address in the SPI Flash space to reserve for the Fault Log data	0- 268435456	0x000000
SPI Chip Select Number	Specifies which chip select line is connected to external SPI Flash.	0 - 7	0

Table 3: Fault Logger UI Parameters (Continued)

Dialog Box Options	Description	Allowable Values	Default Value
Prescale Value for SPI	A calculated prescale value for the SPI IP, based on the system clock frequency and the SPI bus frequency. Can only be enabled when Use Soft EFB is selected. $F_{msck} = F_{source} / (N_{spibr} + 1)$	0x00 - 0x3F	0x00
SPI Flash Command			
Read	Specifies the opcode for external SPI Flash Read (READ)	0 - 255	3
Write	Specifies the opcode for external SPI Flash Write (PP)	0 - 255	2
Write Enable	Specifies the opcode for external SPI Flash Write Enable (WREN)	0 - 255	6
Write Disable	Specifies the opcode for external SPI Flash Write Disable (WRDI)	0 - 255	4
Read Status	Specifies the opcode for external SPI Flash Read Status (RDSR)	0 - 255	5
Write Status	Specifies the opcode for external SPI Flash Write Status (WRSR)	0 - 255	1

HDL Parameters

Table 4 lists the parameters that appear in the HDL.

Table 4: Fault Logger HDL Parameters

Parameter Name	Description	Allowable Values
LATTICE_FAMILY	Define the device family for the IP	MACHXO2 | LPTM2 | ECP5U | ECP5UM
FAULTLOGGER_ASC0_ASC1012	A value of 1 defines the ASC0 is configured as ASC1220, otherwise, ASC0 is configured as ASC1012	0 | 1
FAULTLOGGER_ASC_LOG_CNT	Define the total number of ASC Log	1 to 8
FAULTLOGGER_USER_LOG_CNT	Define the total number of User Log	0 to 4
FAULTLOGGER_TIMESTAMP_ENABLED	A value of 1 defines that the Time Stamp is enabled	0 | 1
FAULTLOGGER_EXTTIMESTAMP_ENABLED	A value of 1 defines that the External Time Stamp is enabled	0 | 1

Table 4: Fault Logger HDL Parameters (Continued)

Parameter Name	Description	Allowable Values
FAULTLOGGER_STORAGE_DISTRAM	A value of 1 defines the Distributed Ram is used for storage, otherwise, EBR is used for storage	0 | 1
FAULTLOGGER_SPI_USERCLOCK	A value of one defines that the ECP5's USERMCLK macro is enabled	0 | 1
FAULTLOGGER_FPGA	A value of one defines that SPI Arbitrator Logic will be used in an ECP5, or in any FPGA without Harden EFB.	0 | 1
Control Register Parameters		
FAULTLOGGER_SPIFLASH_READ_CMD	Define the opcode for SPI Flash Read (READ)	0 to 255
FAULTLOGGER_SPIFLASH_WRITE_CMD	Define the opcode for SPI Flash Write (PP)	0 to 255
FAULTLOGGER_SPIFLASH_WREN_CMD	Define the opcode for SPI Flash Write Enable (WREN)	0 to 255
FAULTLOGGER_SPIFLASH_WRDI_CMD	Define the opcode for SPI Flash Write Disable (WRDI)	0 to 255
FAULTLOGGER_SPIFLASH_RDSR_CMD	Define the opcode for SPI Flash Read Status (RDSR)	0 to 255
FAULTLOGGER_SPIFLASH_WRSR_CMD	Define the opcode for SPI Flash Write Status (WRSR)	0 to 255
FAULTLOGGER_SPI_CHIP_SELECT	Define the SPI Flash chip select line	0 to 7
FAULTLOGGER_LOG_CNT	Define the number of bytes in the UFM or SPI Flash	0 to 268435456
FAULTLOGGER_SPIFLASH_STAADDR	Define the starting address in the SPI Flash space to reserve for the Fault Log data.	0x000000 to 0xFFFFFF
FAULTLOGGER_SPIBR	Define the calculated prescale value for SPI IP, based on the system clock frequency and the SPI bus frequency. $F_{msck} = F_{source} / (N_{spibr} + 1)$	0x00 to 0x3F

I/O Ports

Table 5 describes the input and output ports of the LatticeMico Fault Logger.

Table 5: Fault Logger I/O Ports

I/O Port	Direction	Active	Description
System Clock and Reset			
clk_wishbone	I	—	WISHBONE System Clock

Table 5: Fault Logger I/O Ports (Continued)

I/O Port	Direction	Active	Description
clk_3wi	I	—	Logibuilder Clock used to enable loading of the user log signals from the user signal pool buffers.
resetn	I	Low	System Reset
WISHBONE Slave Signal			
WBS_CYC_I	I	High	Indicates a valid bus cycle is present on the bus.
WBS_STB_I	I	High	Asserts an acknowledgment in response to the assertion of the WISHBONE Master strobe.
WBS_WE_I	I	—	Level sensitive Write/Read control signal. Low - Read operation, High - Write operation
WBS_ADR_I	I	—	32-bit wide address used to select a specific register
WBS_DAT_I	I	—	8-bit data used to read a byte of data from a specific register
WBS_CTI_I	I	—	Not used, always tied to 0
WBS_BTE_I	I	—	Not used, always tied to 0
WBS_LOCK_I	I	—	Not used, always tied to 0
WBS_SEL_I	I	—	Not used, always tied to 0
WBS_DAT_O	O	—	8-bit data used to read a byte of data from a specific register
WBS_ACK_O	O	High	Indicates the requested transfer is acknowledged.
WBS_ERR_O	O	—	Indicates the address is incorrect
WBS_RTY_O	O	—	Not used, always tied to 0
User Signal Pool Ports			
usp_trigger_i	I	Low to High	This input triggers storage of all signals to FLASH memory. A transition from 0 to 1 constitutes a trigger
usp_db_busy_i	I	High	Dual-boot or ASC-boot busy signal

Table 5: Fault Logger I/O Ports (Continued)

I/O Port	Direction	Active	Description
usp_busy_o	O	High	This output indicates that the fault logger is currently having its fault log contents being stored to FLASH. While this busy signal is asserted, all fault log triggers will be ignored.
usp_usrlog0_i	I	—	User log signal byte 0. This port will only be used if USR_LOG_CNT>=1.
usp_usrlog1_i	I	—	User log signal byte 1. This port will only be used if USR_LOG_CNT>=2.
usp_usrlog2_i	I	—	User log signal byte 2. This port will only be used if USR_LOG_CNT>=3.
usp_usrlog3_i	I	—	User log signal byte 3. This port will only be used if USR_LOG_CNT=4.
usp_timestamp_i	I	—	User-provided External Time Stamp (optional). Only available for ECP5.
usp_recordreg_o	O	—	The register value of the Fault Logger Record counter. Only available for ECP5.
usp_memerr_o	O	High	Indicates that the memory is full or contains invalid data. This is the value of the FLTLGINTPTREG.FLASHFULL register's bit. Only available for Fault Logger SPI mode.
ASCVM Interface Ports			
rdat0_data_i	I	—	This is the RDAT data from ASC0. This port will be connected to ASCVM output fl_asc0_data.
rdat0_valid_i	I	High	This is the RDAT valid bit for the data. This port will be connected to ASCVM output fl_asc0_valid.
rdat1_data_i	I	—	This is the RDAT data from ASC1. This port will be connected to ASCVM output fl_asc1_data. This port will only be used if ASC1 is logged
rdat1_valid_i	I	High	This is the RDAT valid bit for the data. This port will be connected to ASCVM output fl_asc1_valid. This port will only be used if ASC1 is logged
rdat2_data_i	I	—	This is the RDAT data from ASC2. This port will be connected to ASCVM output fl_asc2_data. This port will only be used if ASC2 is logged
rdat2_valid_i	I	High	This is the RDAT valid bit for the data. This port will be connected to ASCVM output fl_asc2_valid. This port will only be used if ASC2 is logged
rdat3_data_i	I	—	This is the RDAT data from ASC3. This port will be connected to ASCVM output fl_asc3_data. This port will only be used if ASC3 is logged

Table 5: Fault Logger I/O Ports (Continued)

I/O Port	Direction	Active	Description
rdat3_valid_i	I	High	This is the RDAT valid bit for the data. This port will be connected to ASCVM output fl_asc3_valid. This port will only be used if ASC3 is logged
rdat4_data_i	I	—	This is the RDAT data from ASC4. This port will be connected to ASCVM output fl_asc4_data. This port will only be used if ASC4 is logged
rdat4_valid_i	I	High	This is the RDAT valid bit for the data. This port will be connected to ASCVM output fl_asc4_valid. This port will only be used if ASC4 is logged
rdat5_data_i	I	—	This is the RDAT data from ASC5. This port will be connected to ASCVM output fl_asc5_data. This port will only be used if ASC5 is logged
rdat5_valid_i	I	High	This is the RDAT valid bit for the data. This port will be connected to ASCVM output fl_asc5_valid. This port will only be used if ASC5 is logged
rdat6_data_i	I	—	This is the RDAT data from ASC6. This port will be connected to ASCVM output fl_asc6_data. This port will only be used if ASC6 is logged
rdat6_valid_i	I	High	This is the RDAT valid bit for the data. This port will be connected to ASCVM output fl_asc6_valid. This port will only be used if ASC6 is logged
rdat7_data_i	I	—	This is the RDAT data from ASC7. This port will be connected to ASCVM output fl_asc7_data. This port will only be used if ASC7 is logged
rdat7_valid_i	I	High	This is the RDAT valid bit for the data. This port will be connected to ASCVM output fl_asc7_valid. This port will only be used if ASC7 is logged
Other signals			
fl_irq_o	O	High	Interrupt from fault logger IP to LatticeMico8 microcontroller. This signal will go high when the fault logger has received a fault log trigger. This interrupt is sticky (and will stay high until the interrupt is cleared by the LatticeMico8 microcontroller)
clk_logibuilder	I	—	The rising edge of this 250 kHz clock allows the user log and signals to be loaded into the user signal pool buffers. This signal should be connected automatically to the ASCVM's Logibuilder clock output.
SPI Flash Interface (Following Ports are for ECP5 or FPGAs without harden EFB)			
SPI Flash Interface			
flash_mosi	O	—	External signal, connected to SPI Flash Data IN
flash_miso	I	—	External signal, connected to SPI Flash Data OUT

Table 5: Fault Logger I/O Ports (Continued)

I/O Port	Direction	Active	Description
flash_clk	O	—	External signal, connected to SPI Flash Clock. When using configuration flash, this serves as an output node to USERMCLK macro.
flash_mcsn	O	—	External signal, connected to SPI Flash Data Chip Select
Fault Log SPI Interface			
faultlog_clk_oe	I	—	Connect to the Soft EFB's spi_clk_oe output
faultlog_clk_o	I	—	Connect to the Soft EFB's spi_clk_o output
faultlog_clk_i	O	—	Connect to the Soft EFB's spi_clk_i output
faultlog_mosi_oe	I	—	Connect to the Soft EFB's mosi_oe output
faultlog_mosi_o	I	—	Connect to the Soft EFB's mosi_o output
faultlog_mosi_i	O	—	Connect to the Soft EFB's mosi_i output
faultlog_miso_oe	I	—	Connect to the Soft EFB's miso_oe output
faultlog_miso_o	I	—	Connect to the Soft EFB's miso_o output
faultlog_miso_i	O	—	Connect to the Soft EFB's miso_i output
faultlog_mcsn_oe	I	—	Connect to the Soft EFB's mscn_oe output. mscn_oe/ mscn_o pairs are 8-bit buses from the Soft EFB. By default, the mcsn_oe[0]/mcsn_o[0] pair is connected to the faultlog_mcsn_oe/faultlog_mcsn_o pair. If the user chooses chip select, Platform Designer selects one of the eight bits from the mcsn_oe/mcsn_o pairs to connect to the faultlog_mcsn_oe/faultlog_mcsn_o pair, based on the value of the FAULTLOGGER_SPI_CHIP_SELECT parameter.
faulutlog_mscn_o	I	—	Connect to the Soft EFB's mscn_o output
External SPI Master Interface			
extspi_mosi	I	—	Connect to the external SPI Master's MOSI output
extspi_miso	O	—	Connect to the external SPI Master's MISO output
extspi_clk	I	—	Connect to the external SPI Master's SCLK output
extspi_mcsn	O	—	Connect to the external SPI Master's CSN output
Miscellaneous Signals			
extspi_req	I	—	Request input from the external SPI Master
extspi_grant	O	—	Grant output signal from the SPI Arbitrator

Register Descriptions

The LatticeMico Fault Logger WISHBONE module has a register map to allow the service of the hardened functions through the WISHBONE bus interface read/write operations. Table 6 through Table 8 describe the register map of the Fault Logger module.

Table 6: WISHBONE Addressable Registers for Fault Logger Module

Register Name	Register Function	Address	Access
CONTENT	Holds the information of the Fault Log	0x00 - 0x59	Read
IRQ	Interrupt Request Register	0x60	Read/Write
SPI_RD_CMD	Holds the opcode for SPI Flash Read (READ)	0x61	Read
SPI_WR_CMD	Holds the opcode for SPI Flash Write (PP)	0x62	Read
SPI_WREN_CMD	Holds the opcode for SPI Flash Write Enable (WREN)	0x63	Read
SPI_WRDI_CMD	Holds the opcode for SPI Flash Write Disable (WRDI)	0x64	Read
SPI_RDSR_CMD	Holds the opcode for SPI Flash Read Status (RDSR)	0x65	Read
SPI_WRSR_CMD	Holds the opcode for SPI Flash Write Status (WRSR)	0x66	Read
SPI_CHP_SEL	Holds the chip select line of the SPI Flash	0x67	Read
LOG_CNT	Indicates data capacity (in bytes) of the fault log flash	0x70 - 0x73	Read/Write
SPISTARTADDR	Indicates Start address for the Flash storage space	0x74-0x77	Read/Write
FLSPIARBREG	Indicates Fault Logger SPI Arbitrator ownership	0x78	Read/Write
SPIBRREG	Indicates the value of the FAULTLOGGER_SPIBR parameter	0x79	Read/Write
FLRECCNTREG	Indicates Fault log Record Count.	0x7S-0x7B	Read/Write

Table 7 and Table 8 provide details about each register in the LatticeMico Fault Logger.

Fault Log Content Register Definition – CONTENT

The WISHBONE host has Read-Only access to these registers. The fault log actual length of the fault log will vary, but the MachXO2/Platform Manager 2 can use up to 0x45 (dec 69). Addresses 0x46-0x59 are reserved for future expansion of the fault log. For details on the byte per byte contents of the fault log contents, please see the “Fault Log Map” on page 4.

Interrupt Request Register Definition – IRQ

The WISHBONE host has Read and Write access to these registers.

Table 7: CHx_INFO Register Bit Definition

Bit	Field	Description	Access
0	IRQ	Interrupt Bit for Fault Log event	Read
1	IRQCLR	Interrupt Clear Bit for Fault Log event	Read/Write
2	IRQMSK	Interrupt output mask. Asserted low. If this bit is 0, output fl_irq_o will remain low, even when the interrupt bit (FLTLGINTPTREG.IRQ) is high.	Read/Write
3	FLASHFULL	Indicate that the flash is full or contains invalid data	Read/Write
	IRQ2	Interrupt Bit for External SPI master event. This bit is set when the External SPI Master has completed its event.	Read
	IRQCLR2	Interrupt Clear Bit for External SPI Master event.	Read/Write
7:4	RSVD	Reserved Bit	Read/Write

SPI Flash Command Register Definition

SPI Flash Command Registers are 8-bit registers, each register holds a specific SPI Flash command and correlates to a corresponding Verilog parameter. The WISHBONE host has Read-Only access to these registers.

Table 8: SPI Flash Command Register Definition

Register Name	Corresponding Verilog Parameter	Address	Access
SPI_RD_CMD	FAULTLOGGER_SPIFLASH_READ_CMD	0x61	Read
SPI_WR_CMD	FAULTLOGGER_SPIFLASH_WRITE_CMD	0x62	Read
SPI_WREN_CMD	FAULTLOGGER_SPIFLASH_WREN_CMD	0x63	Read
SPI_WRDI_CMD	FAULTLOGGER_SPIFLASH_WRDI_CMD	0x64	Read
SPI_RDSR_CMD	FAULTLOGGER_SPIFLASH_RDSR_CMD	0x65	Read
SPI_WRSR_CMD	FAULTLOGGER_SPIFLASH_WRSR_CMD	0x66	Read

SPI Flash Chip Select Register Definition - SPI_CHP_SEL

SPI_CHP_CMD is an 8-bit register that specifies which chip select line (LatticeMico EFB/SoftEFB SPI Master) is connected to the fault logging SPI flash. This register correlates to the Verilog parameter FAULTLOGGER_SPI_CHIP_SELECT. The WISHBONE host has Read-Only access to these registers.

Fault Log Data Capacity Register Definition – LOG_CNT

LOG_CNT is a 32-bit registers that indicates data capacity (in bytes) of the fault log FLASH. This field is context dependent: it can show the max storable data in either the UFM or external SPI FLASH. This register correlates to Verilog parameter FAULTLOGGER_LOG_CNT. The WISHBONE host has Read and Write access to this register.

SPI Flash Fault Log Starting Address Register Definition - SPI_START_ADDR

SPI_START_ADDR is a 32-bit register that indicates the start address (in bytes) of the FLASH storage space. This register correlates to the Verilog parameter FAULTLOGGER_SPIFLASH_STAADDR. The WISHBONE host has Read and Write access to this register. This parameter is only valid for ECP5 devices.

Fault Log SPI Arbitrator Ownership Register Definition - FL_SPI_ARB_REG

FL_SPI_ARB_REG is an 8-bit register that indicates ownership of the Fault Logger arbitrator. The WISHBONE host has Read and Write access to this register. The following table describes legal patterns of the Fault Logger SPI arbitrator.

Table 9: Fault Logger Ownership Legal Pattern

Ownership	Pattern	Description
Default	0x00	Default value of the arbitrator
MICO	0x03	Indicates that Mico owns the arbitrator
External SPI master	0x05	Indicates that the external SPI master owns the arbitrator

Soft-EFB SPI Baud Rate Register Definition - SPI_BR_REG

LOG_CNT is an 8-bit register that indicates the Soft-EFB SPI's desired baud rate. This register correlates to the Verilog parameter FAULTLOGGER_SPIBR. The WISHBONE host has Read and Write access to this register.

Fault Log Record Counter Register Definition - FL_REC_CNT_REG

LOG_CNT is a 16-bit register that allows the WISHBONE host to store the amount of Fault Log entries in SPI FLASH. The WISHBONE host has Read and Write access to this register.

LatticeMico8 Microcontroller Software Support

This section describes the LatticeMico8 microcontroller software support provided for the LatticeMico Fault Logger component.

Device Driver

The Fault Logger device driver interacts directly with the Fault Logger instance. This section describes the limitations, type definitions, structure, and functions of the Fault Logger device driver.

Type Definitions

This section describes the type definitions for the Fault Logger device context structure. This structure, shown in Figure 2, contains the Fault Logger component instance-specific information and is dynamically generated in the DDStructs.h header file. This information is largely filled in by the managed build process by extracting the Fault Logger component-specific information from the platform specification file. As part of the managed build process, designers can choose to control the size of the generated structure, and hence the software executable, by selectively enabling some of the elements in this structure via C preprocessor macro definitions. These C preprocessor macro definitions are explained later in this document. You should not manipulate the members directly, because this structure is for exclusive use by the device driver. Table 10 describes the parameters of the Fault Logger device context structure shown in Figure 2.

Device Context Structure

Figure 2 shows the Fault Logger device context structure.

Figure 2: Fault Logger Device Context Structure

```
struct st_MicoFLCtx_t {
    const char *    name;
    size_t          base;
    unsigned char   intrLevel;
    unsigned char   mem_mode;
    unsigned char   fl_spibr;
    unsigned long   flash_start_addr;
    unsigned long   curr_addr;
    unsigned long   max_addr;
    unsigned int    record_cnt;
    unsigned long   last_empty_addr;
    void *          p_efb;
    void *          p_sefb;
} MicoFLCtx_t;
```

Table 10 describes the Fault Logger device context parameters.

Table 10: Fault Logger Device Context Parameters

Parameter	Data Type	Description
name	const char*	Fault Logger instance name (entered in MSB)
base	size_t	MSB-assigned base address for this instance
intrLevel	unsigned char	Processor interrupt line to which this instance is connected
mem_mode	unsigned char	This value specifies the current Flash Memory Mode (UFM/SPI Flash)
fl_spibr	unsigned char	This value specifies the expected Soft-EFB SPI baud rate
flash_start_addr	unsigned long	This value specifies the start address for fault log storage
curr_addr	unsigned long	This value specifies the current Flash Memory Address
max_addr	unsigned long	This value specifies the maximum flash storage
record_cnt	unsigned int	This value specifies the number of sets of log data contained in SPI Flash
flash_start_addr	unsigned long	This value specifies the last empty address before the external SPI master accesses SPI Flash
p_efb	void*	This value points to the EFB instance used by Fault Logger
p_sefb	void*	This value points to the Soft-EFB instance used by Fault Logger

C Preprocessor Macro Definitions

This section describes the C preprocessor macro definitions that are available to the software developer. There are two types of macro definitions: 'object-like' and 'function-like'.

The 'object-like' macro definitions do not take any arguments and are used to control the size of the generated application executable. There are three ways an 'object-like' macro definition can be used by the software developer.

1. Manually adding the -D<*macro name*> option to the compiler's command line in the application's 'Build Properties'. Refer to the LatticeMico8 Developer User Guide for more information on how to manually add the macro definition in the application's 'Build Properties' GUI.
2. Automatically adding the -D<*macro name*> option to the compiler's command-line in the application's 'Build Properties' by enabling the 'check-box' associated with the macro definition. Refer to the LatticeMico8 Developer User Guide for more information on how to set up the check/ uncheck the macro definitions in the application's 'Build Properties' GUI.
3. Manually adding the macro definition to the C code using the following syntax:

   ```
   #define <macro name>
   ```

It is recommended that the developer use option 1 or 2.

- __MICOFL_NO_SPI_INIT_VALIDATION__

  This preprocessor macro definition disables code and data structures within the device driver that disable the LatticeMico8 EFB SPI module in the software driver and application. In order words, LatticeMico8 assumes the connected SPI Flash is NOT shared with other SPI Master, and does not check whether the SPI is occupied by other SPI Master or not during the power cycle. It is not defined by default.

- __MICOFL_USER_IRQ_HANDLER__

  This preprocessor macro definition disables code and data structures within the device driver that allow the user to define the custom interrupt routine, the default routine will be disabled. It is not defined by default.

Table 11: C Preprocessor Function-like Macros For Fault Logger

Macro Name	Second Argument to Macro / Third Argument to Macro (if exist.	Description
MICO_FL_READ_CONTENT	The 8-bit value reads from the Fault Log content / address offset	This macro reads a character from the Fault Log content register with a specific address offset
MICO_FL_READ_IRQ	The 8-bit value reads from the Interrupt register.	This macro reads a character from the Interrupt register.
MICO_FL_WRITE_IRQ	The 8-bit value reads from the Interrupt register.	This macro reads a character to the Interrupt register.
MICO_FL_READ_SPI_RD_CMD	The 8-bit value reads from the SPI Flash Read Command register.	This macro reads a character to the SPI Flash Read Command register
MICO_FL_READ_SPI_WR_CMD	The 8-bit value reads from the SPI Flash Write Command register.	This macro reads a character to the SPI Flash Write Command register

Table 11: C Preprocessor Function-like Macros For Fault Logger (Continued)

Macro Name	Second Argument to Macro / Third Argument to Macro (if exist.	Description
MICO_FL_READ_SPI_WREN_CMD	The 8-bit value reads from the SPI Flash Write Enable Command register.	This macro reads a character to the SPI Flash Write Enable Command register
MICO_FL_READ_SPI_WRDI_CMD	The 8-bit value reads from the SPI Flash Write Disable Command register.	This macro reads a character to the SPI Flash Write Disable Command register
MICO_FL_READ_SPI_RDSR_CMD	The 8-bit value reads from the SPI Flash Read Status Command register.	This macro reads a character to the SPI Flash Read Status Command register
MICO_FL_READ_SPI_WRSR_CMD	The 8-bit value reads from the SPI Flash Write Status Command register.	This macro reads a character to the SPI Flash Write Status Command register
MICO_FL_READ_SPI_CHP_SEL	The 8-bit value reads from the SPI Flash Chip Select register.	This macro reads a character to the SPI Flash Chip Select register
MICO_FL_READ_LOG_CNT_OFFSET	The 8-bit value reads from Fault Log Data Capacity register / address offset	This macro reads a character from the Fault Log Data Capacity register with a specific address offset
MICO_FL_WRITE_LOG_CNT_OFFSET	The 8-bit value writes to Fault Log Data Capacity register / address offset	This macro writes a character to the Fault Log Data Capacity register with a specific address offset
MICO_FL_READ_SPI_START_ADDR	The 8-bit value reads from SPI Starting Address register	This macro reads a character from the SPI Start Address register
MICO_FL_WRITE_SPI_START_ADDR	The 8-bit value writes to SPI Starting Address register	This macro writes a character to the SPI Start Address register
MICO_FL_READ_SPI_ARB_REG	The 8-bit value reads from Fault Log SPI Arbitrator register	This macro reads a character from the Fault Log SPI Arbitrator register
MICO_FL_WRITE_SPI_ARB_REG	The 8-bit value writes to Fault Log SPI Arbitrator register	This macro writes a character to the Fault Log SPI Arbitrator register
MICO_FL_READ_SPI_BR_REG	The 8-bit value reads from SPI Baud Rate register	This macro reads a character from the SPI Baud Rate register
MICO_FL_WRITE_SPI_BR_REG	The 8-bit value writes to SPI Baud Rate register	This macro writes a character to the SPI Baud Rate register
MICO_FL_READ_RECCNT_REG	The 8-bit value reads from Fault Log Record Counter register	This macro reads a character from the Fault Log Record Counter register
MICO_FL_WRITE_RECCNT_REG	The 8-bit value writes to Fault Log Record Counter register	This macro writes a character to the Fault Log Record Counter register

Note: The first argument to the macro is the Fault Logger address.

- __MICOFL_USE_SOFT_EFB__

This preprocessor macro definition indicates whether Fault Logger is using Soft-EFB. It is not defined by default.

Functions

This section describes the implemented device-driver-specific functions.

MicoFLInit Function

```
void MicoFLInit (MicoFLCtx_t *ctx);
```

This is the Fault Logger initialization function.

Table 12 describes the parameter in the MicoFLInit function syntax

Table 12: MicoFLInit Function Parameter

Parameter	Description
MicoFLCtx_t	Pointer to a valid MicoFLCtx _t structure representing a valid Fault Logger instance.

MicoFLRegisterEFB Function

```
void MicoFLRegisterEFB (MicoFLCtx_t *ctx,
                        MicoEFBCtx_t *p_efb);
```

This function registers an EFB instance into the Fault Logger instance. This EFB will be used for the communication between Fault Logger control and the UFM or external SPI Flash.

Table 13 describes the parameters in the MicoFLRegisterEFB function syntax.

Table 13: MicoFLRegisterEFB Function Parameters

Parameter	Description
MicoFLCtx_t	Pointer to a valid MicoFLCtx_t structure representing a valid Fault Logger instance.
MicoEFBCtx_t	Pointer to a valid MicoEFBCtx_t structure representing a valid EFB instance.

MicoFL_UFMValidation Function

```
void MicoFL_UFMValidation(MicoFLCtx_t *ctx);
```

This function validate whether the User Flash memory (UFM) contains a valid Fault Log and check for the next available empty slot for the next entry. This function should be called only once during the system power-up. Error code will return when the validation process is failed.

Table 14 describes the parameter in the MicoFL_UFMValidation function syntax.

Table 14: MicoFL_UFMValidation Function Parameter

Parameter	Description
MicoFLCtx_t	Pointer to a valid MicoFLCtx _t structure representing a valid Fault Logger instance.

Table 15 describes the values returned by the MicoFL_UFMValidation Function.

Table 15: Values Returned by the MicoFL_UFMValidation Function

Parameter	Description
0	Valid log file
-1	Invalid log file
-2	Unexpected return

MicoFL_SPIValidation Function

```
void MicoFL_SPIValidation(MicoFLCtx_t *ctx);
```

This function validate whether the external SPI memory contains a valid Fault Log and check for the next available empty slot for the next entry. This function should be called only once during the system power-up. Error code will return when the validation process is failed.

Table 16 describes the parameter in the MicoFL_SPIValidation function syntax.

Table 16: MicoFL_SPIValidation Function Parameter

Parameter	Description
MicoFLCtx_t	Pointer to a valid MicoFLCtx _t structure representing a valid Fault Logger instance.

Table 17 describes the values returned by the MicoFL_SPIValidation Function.

Table 17: Values Returned by the MicoFL_SPIValidation Function

Parameter	Description
0	Valid log file
-1	Invalid log file
-2	Unexpected return

MicoFL_WriteUFM Function

```
void MicoFL_WriteUFM (MicoFLCtx_t *ctx);
```

This function record the fault logger snapshot to the User Flash Memory (UFM). Error code will return when the write process is failed.

Table 18 describes the parameter in the MicoFL_WriteUFM function syntax.

Table 18: MicoFL_WriteUFM Function Parameter

Parameter	Description
MicoFLCtx_t	Pointer to a valid MicoFLCtx _t structure representing a valid Fault Logger instance.

Table 19 describes the values returned by the MicoFL_WriteUFM Function.

Table 19: Values Returned by the MicoFL_WriteUFM Function

Parameter	Description
0	Valid log file
-1	Write to an invalid memory (Not enough space)

MicoFL_WriteSPI Function

```
void MicoFL_WriteSPI (MicoFLCtx_t *ctx);
```

This function record the fault logger snapshot to the external SPI Flash memory. Error code will return when the write process is failed.

Table 20 describes the parameter in the MicoFL_WriteSPI function syntax.

Table 20: MicoFL_WriteSPI Function Parameter

Parameter	Description
MicoFLCtx_t	Pointer to a valid MicoFLCtx _t structure representing a valid Fault Logger instance.

Table 21 describes the values returned by the MicoFL_WriteSPI Function.

Table 21: Values Returned by the MicoFL_WriteSPI Function

Parameter	Description
0	Write successfully
-1	Write to an invalid memory (not enough space),

MicoFLISR Function

```
void MicoFLISR (MicoFLCtx_t *ctx);
```

This function is the Fault Logger Interrupt handler. Each Fault Logger instance has it's own default interrupt handler implementation. If the developer wishes to use their own interrupt handler, they must define __MICOFL_USER_IRQ_HANDLER__ preprocessor.

Table 22 describes the values returned by the MicoFLISR Function.

Table 22: MicoFL_WriteUFM Function Parameter

Parameter	Description
MicoFLCtx_t	Pointer to a valid MicoFLCtx _t structure representing a valid Fault Logger instance.

MicoFLRegisterSEFB Function

```
void MicoFLRegisterSEFB (MicoFLCtx_t *ctx,
                         MicoEFBCtx_t *p_sefb);
```

This function registers a Soft-EFB instance into the Fault Logger instance. This Soft-EFB handles the communication between Fault Logger control and the external SPI Flash.

Table 23 describes the parameters in the MicoFLRegisterSEFB function syntax.

Table 23: MicoFLRegisterSEFB Function Parameters

Parameter	Description
MicoFLCtx_t	Pointer to a valid MicoFLCtx _t structure representing a valid Fault Logger instance.
MicoSEFBCtx_t	Pointer to a valid MicoSEFBCtx_t structure representing a valid Soft-EFB instance.

MicoFL_Soft_SPIValidation Function

```
void    MicoFL_Soft_SPIValidation    (MicoFLCtx_t    *ctx,
unsigned char power_on);
```

This function validates whether the external SPI memory contains a valid Fault Log and checks for the next available empty slot for the next entry. This function is called once during the system power-up and is called again if the Memory Error bit is flagged. A failed validation process will return an error code.

Table 24 describes the parameters in the MicoFL_Soft_SPIValidation function syntax.

Table 24: MicoFL_Soft_SPIValidation Function Parameters

Parameter	Description
MicoFLCtx_t	Pointer to a valid MicoFLCtx _t structure representing a valid Fault Logger instance.
unsigned char	Indicates whether this function was called during power-up. A value of 0 indicates that it was not called.

Table 25 describes the values returned by the MicoFL_Soft_SPIValidation function.

Table 25: Values returned by the MicoFL_Soft_SPIValidation Function

Parameter	Description
0	Valid log file
-1	Invalid log file
-2	Unexpected return

MicoFL_WriteSoftSPI Function

```
void MicoFL_WriteSoftSPI (MicoFLCtx_t *ctx);
```

This function record the fault logger snapshot to the external SPI Flash memory. Error code will return when the write process is failed.

Table 26 describes the parameter in the MicoFL_WriteSoftSPI function syntax.

Table 26: MicoFL_WriteSoftSPI Function Parameter

Parameter	Description
MicoFLCtx_t	Pointer to a valid MicoFLCtx _t structure representing a valid Fault Logger instance.

Table 27 describes the values returned by the MicoFL_WriteSoftSPI function.

Table 27: Values returned by the MicoFL_WriteSoftSPI function

Parameter	Description
0	Write was successful
-1	Wrote to invalid memory (not enough space)

Software Usage Example

This section provides an example of using the Fault Logger. The example is shown in Figure 3 and assumes the presence of a Fault Logger component named “faultlogger”, and a EFB component named “efb”.

Figure 3: Fault Logger Software Example

```
#include "MicoUtils.h"
#include "DDStructs.h"
#include "MicoEFB.h"
#include "MicoFL.h"

int main(void){
MicoFLCtx_t *fl = &faultlogger_faultlogger;
  MicoEFBCtx_t *efb = &efb_efb;

  size_t fl_address = (size_t)(fl->base);

  // Register the EFB instance into Fault Logger
  MicoFLRegisterEFB(fl, efb);

  // Validate the Fault Logger Flash Memory
  MicoFL_SPIValidation(fl);

  #ifdef __MICO_NO_INTERRUPTS__
  do{
      MICO_FL_READ_IRQ(fl_address, status);
    if (status & MICO_FL_IRQ_TRI){
      MicoFL_WriteSPI(fl);
    }
  }while(1);
  #else
  MICO_FL_WRITE_IRQ(fl_address ,MICO_FL_IRQ_EN);
  #endif

  return(0);
}
```

Revision History

Component Version	Description
1.0	Initial release.
1.1	Fixed Fault Logger masked-out issue that occurred when Dual-Boot is busy. Added section “ASC Fault Log Record Memory Map” on page 5.
1.2	Added ECP5 support with new scan, record counter, Fault Log SPI arbitrator, and external timestamp functions.

Trademarks