Video Pipeline

September 2015 Reference Design RD1213

Introduction

This document describes the structure and implementation of a video pipeline demo design running in the Lattice ECP3-150EA-8FN1156C device based on the Sparrowhawk FX Board. This demo takes two of the four video streams from DVI and SDI inputs and then combines them into one with different configuration modes. The video processing IPs including de-interlacer, scaler, video frame buffer, color space converter and video interface IPs including DVI, SDI together with the Mico8 and UART as the interactive interface are used in this demo design to support multiple video input formats and configurable out dimensions for the PIP (picture in picture) and PAP (picture and picture).

Features

- Supports two DVI inputs and two SDI inputs
- Supports the processing of two video channels simultaneously
- Supports the OSD function
- Supports the configurable modes and parameters through the RS232 interface
- Supports the DVI and SDI output at 1080p60 or 720p60 mode

Functional Description

Figure 1 illustrates the major parts on the Sparrowhawk FX main board. The SDI add-on board provides the SDI input and output ports which are connected with the main board through a slot. The DVI inputs and outputs are directly connected with the main board. The RS232 port which communicates with the computer is used as the interactive interface for users to configure the registers/parameters/modes for the demo. The two DDR3 onboard memories are used for the frame buffer in the demo design.

Figure 1. Major Devices on the Sparrowhawk FX Board

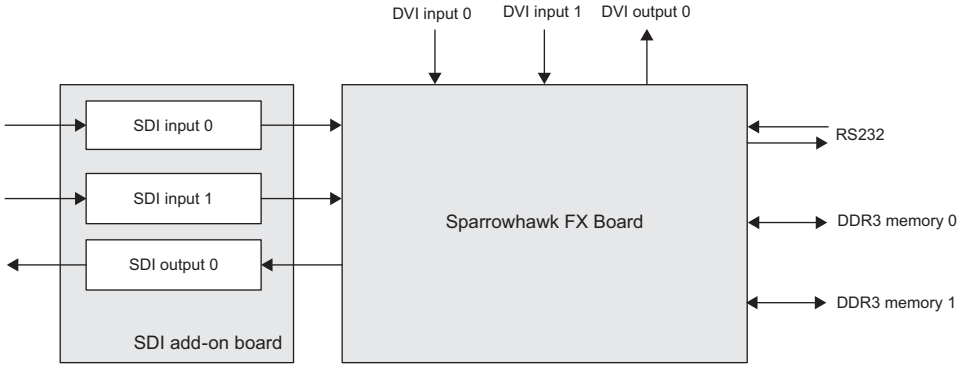
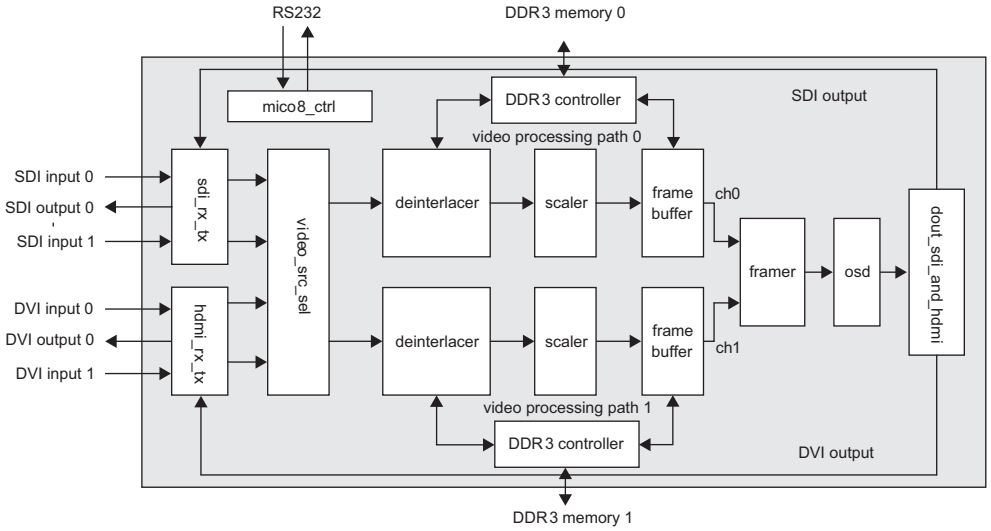


Figure 2 illustrates the functional modules in this demo design. The PCS receives the DVI/SDI serial video steam and converts it into parallel video data. After the decoder of DVI/SDI IP, the two video streams and the corresponding synchronous signals on the two video channels are selected from the four video sources and connected with the video processing IPs. It can be seen from the diagram that there are two identical data paths for the video processing on the two video channels. The onboard DDR3 memories are used for the de-interlacer IP and the frame buffer IP. Finally, the two video steams are combined into one picture with OSD and transmitted to the DVI and SDI interface.

Figure 2. Demo Design Modules



The function of each module is described below:

- **sdi_tx_rx** – Converts the serial input SDI data to parallel video data and generates the timing synchronous signals to the video processing IPs. It also converts the parallel video data after the processing to the serial SDI data.
- **hdmi_tx_rx** – Converts the serial input HDMI data to parallel video data and generates the timing synchronous signals to the video processing IPs. It also converts the parallel video data after the processing to the serial HDMI data.
- **video_src_sel** – Selects two video data from the four sources and generates some configuration parameters for the video processing IPs.
- **video_ip_dsp** – Includes the three video processing IPs: de-interlacer, scaler and frame buffer, and the DDR3 controller together with the arbiter; and they are on both the video processing path 0 and video processing path 1.
- **framer** – Combine the two video data into one picture either at 720p or 1080p mode.
- **osd** – Adds the video information, date and time which can be changed by users through RS232 interface, and other fixed texts to the video data.
- **dout_sdi_and_hdmi** – Generates the SDI/DVI data and timing signals which can be directly connected with the corresponding IPs.
- **mico8_ctrl** – Includes the main Mico8 core and the UART controller which is used to communicate with the computer through the RS232 interface.

Demo Setup and Configuration

Figure 3 shows the picture of the Sparrowhawk FX Board and the SDI add-on board and which ports on the two boards are used in this demo. The four video sources come from two SDI inputs and two DVI inputs and the video output are connected with the monitor through DVI output 0. Users can run the software HyperTerminal through the RS232 interface to configure the video source, OSD color, OSD enabling on the four lines, the location and dimension for the video from path 0 and path 1 and the date and time.

Figure 3. Ports and Switches Used in the Demo

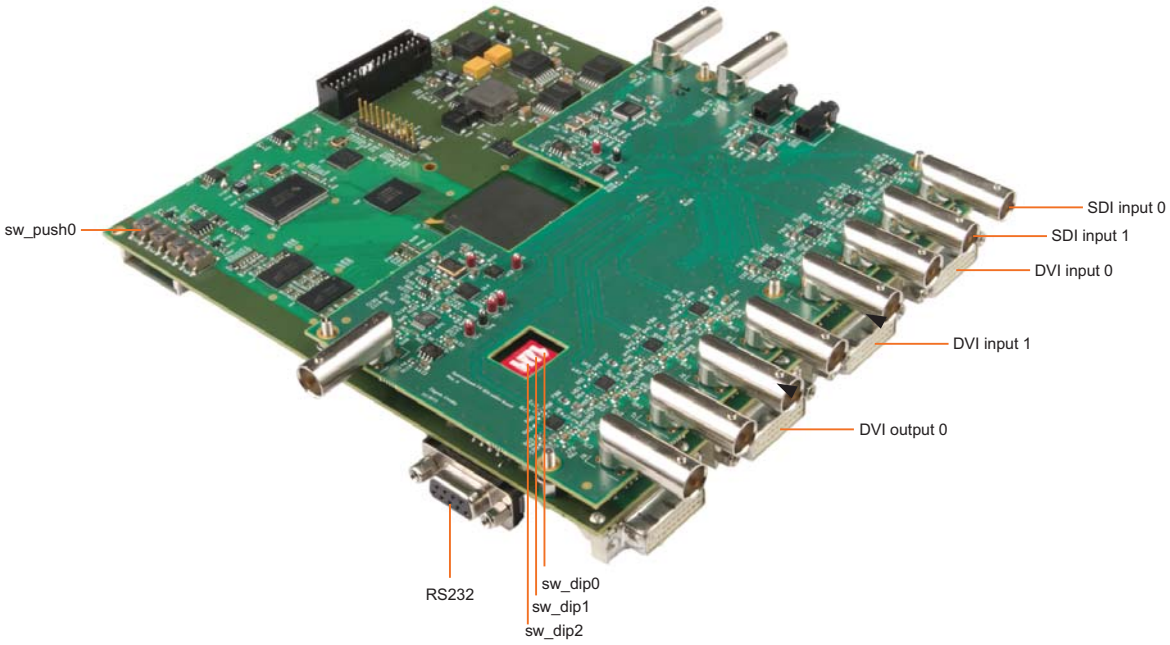


Table 1. Switch and Push-button Definitions

Switch/Push Button	Definition
sw_push0	Global reset
sw_dip0	'1' – video output is 1080p; '0' – video output is 720p
sw_dip1	'1' – enable local pattern generation for video path 1 if there is no active video on this path
sw_dip2	'1' – the logics will be automatically reset if there is error; '0' – users should press sw_push0 to issue the manual global reset

The following tables describe the usage of the HyperTerminal to configure the demo.

Table 2. Video Channels Combination Selection[1]

Video Channel	Video Channels Combination Selection											
	0	1	2	3	4	5	6	7	8	9	a	b
CH0	vid0	vid0	vid0	vid1	—	—	vid1	—	—	vid1	—	—
CH1	vid1	—	—	vid0	vid0	vid0	—	vid1	—	—	vid1	—
CH2	—	vid1	—	—	vid1	—	vid0	vid0	vid0	—	—	vid1
CH3	—	—	vid1	—	—	vid1	—	—	vid1	vid0	vid0	vid0

1. CH0---DVI input 0; CH1---DVI input 1; CH2---SDI input 0(J1); CH3---SDI input 1(J2); vid0—-video path 0; vid1---video path 1

If vid0 and vid1 have an overlap on the display, vid1 is always in front, which means that the video data is from vid1 at the overlap area.

Table 3. OSD Color Selection

OSD Color Selection						
0	1	2	3	4	5	6-f
Red	Green	Blue	Yellow	Magenta	Cyan	Different grey grades from black to white

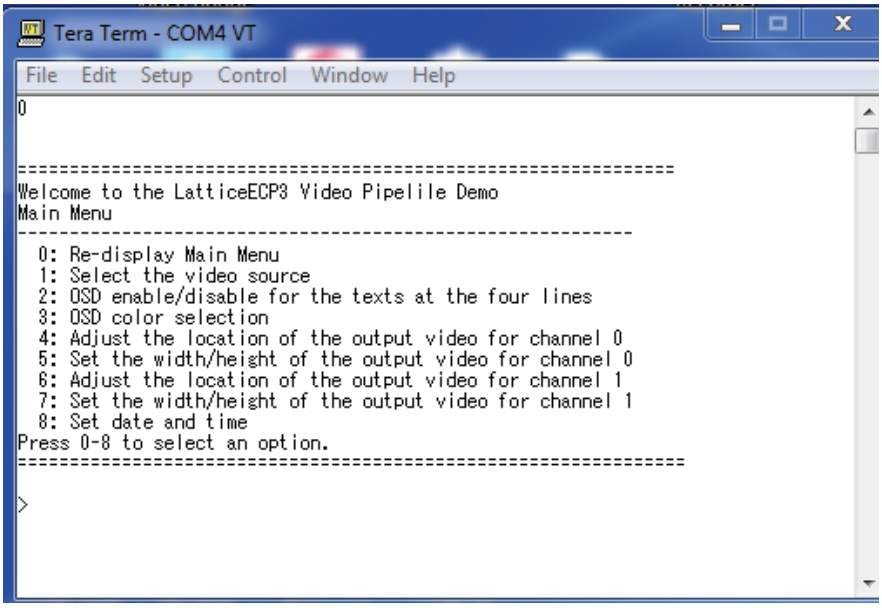
Table 4. OSD Enable/Disable for the Texts on the Four Lines

Bit	Definition
bit0	'1' – enable the video information on the video path 0 display on the monitor
bit1	'1' – enable the video information on the video path 1 display on the monitor
bit2	'1' – enable the fixed texts “LatticeECP3 VIDEO PIPELINE DEMO” display on the monitor
bit3	'1' – enable the date and time display on the monitor

When setting the dimension of the video after scaler from the path 0/1, the value of the horizontal width should be the actual frame width minus and the value of the vertical height should be the actual frame height minus 1. The actual frame width should be multiples of 8. The number of the horizontal location for the output video should be even.

Figure 4 shows a serial port term snapshot. Configure the baud rate to 115200, Data bits to 8, Parity to None, Stop bits to 1 and Flow control to None.

Figure 4. Snapshot of the Main Menu in the HyperTerminal



Two videos can be displayed on the monitor by the Video Channels Combination Selection in Table 2.

Figure 5. Dual Video Display

Technical Support Assistance

Submit a technical support case via www.latticesemi.com/techsupport.

Revision History

Date	Version	Change Summary
September 2015	1.0	Initial release.