Product Bulletin

January 2026 **#PB1412 Rev 1.2**

I2C Read-back Failure Mode on Specific Use Scenario in MachXO2, MachXO3, and MachXO4 Products and Work-Around Solutions

Lattice is issuing this Product Bulletin to inform that it identified a potential failure mode on I2C read-back under certain use case scenarios in MachXO2, MachXO3, and MachXO4 Devices. The failure mode is a limited use case, and most customers will not be impacted. However, for the limited set of customers using the device in the use modes described below, there is a risk in I2C read-back. We are communicating the potential failure modes and workaround solutions to address it.

There is no datasheet specification change due to this finding. Datasheet specification remains same as before. Since MachXO2 was introduced, thousands of customers globally installed millions of units' devices. To date, only a few customers noticed this issue in their specific application environment and using solutions identified below have successfully mitigated the issue.

Known Issue

I2C Read-back Data is undefined in certain cases if the Embedded Function Block (EFB) WISHBONE clock input port ('wb_clk_i') is unconnected or is too slow.

No Customer Application Issue when:

1. I2C ports are NOT used in the customer application.
2. I2C ports are used in MASTER mode only.
    a. Neither port is used for Configuration, Embedded Programming or User Slave I2C.
3. I2C ports are used in User or Configuration SLAVE mode but:
    a. EFB Hard IP block is instantiated and WISHBONE clock is running >3.0 MHz.

Customer Application Is Exposed when:

1. Primary or Secondary I2C port is used in User or Configuration SLAVE mode, and
    a. EFB Hard IP block is instantiated with wishbone clock is running <3.0 MHz, or
    b. No EFB block is instantiated.

    Note, for the purposes of this document, UFM access in XO2, XO3LF and XO4 should be considered a Configuration Slave mode.

See Appendix 3 “Decision Tree” for a detail of possible use cases

If exposed, Lattice suggest one of the following two workaround options:

- Option 1: FPGA Design Update (Preferred)
    - No PCB change, FPGA code needs to be updated.

- Option 2: I2C Configuration Algorithm Update (Limited application)
    - No change on FPGA, but requires a I2C system controller software update.
    - Only targets Configuration SLAVE mode.
    - Not applicable if:
        - I2C User Slave ports are used and WISHBONE clock < 7.5x I2C bus speed

Workaround Option 1: FPGA Design Update:

Instantiate EFB and connect Wishbone Clock of rate at least 7.5x the I2C bus rate (e.g. >3.0 MHz for 400 kHz I2C bus).

Workaround Option 2: I2C Configuration Update:

Ensure certain configuration commands are executed within a valid configuration edit mode.

Further details are explained in Appendix 1: “Common Application Issues”, Appendix 2: “Frequently Asked Questions” and Appendix 3: “Decision Tree”.

Customers are advised to use workaround to prevent any possibility of field failures or performance marginality. Lattice Semiconductor has no plan to further update the MachXO2, MachXO3 and MachXO4 product family.

CONTACT

If you have any questions or require additional information, please open a technical support case at:

http://www.Latticesemi.com/techsupport

Sincerely,

Lattice Semiconductor MachXO2, MachXO3 and MachXO4 Product Line Management

Revision History

Date	Version	Description of Revisions
January 14, 2026	1.2	• Added MachXO4 • Updated Appendix 2 • Editorial fixes
March 4, 2015	1.1	• Improved Option 2 wording • Added FAQ in Appendix 2 with a solution to EFB synthesis optimization.
February 23, 2015	1.0	• Initial Release

Appendix 1: Common Application Issues

Workaround Option 1: FPGA Design Update

Possible Use Scenarios	Recommended Workaround
EFB already instantiated, but 'wb_clk_i' is too slow	Reduce I2C bus speed or Increase 'wb_clk_i' rate
Design does not contain fast clock	Instantiate OSCH with Freq >= 3 MHz and connect to 'wb_clk_i'
In-field FPGA upgrade fails due to this issue	User must implement I2C Configuration Update, or utilize an alternate sysConfig port if available (for example, JTAG or SPI) to recover I2C access.
Design uses power control	No impact - wake on I2C option wakes OSCH
FPGA Design is User I2C 'Master' only. (no Configuration, Embedded programming, UFM, or Slave I2C)	No work-around is necessary
Only UFM is accessed by external Master, with I2C bus speed <=200 kHz (no Configuration, Embedded programming, or Slave I2C)	No work-around is necessary if impacted commands are not used.
Design is 'validated' and cannot be re-built without incurring significant revalidation effort	Contact Lattice for further assistance.

Workaround Option 2: I2C Configuration Update

Possible Use Scenarios	Recommended Workaround
Device ID check is prior to ISC_ENABLE/X command	Remove Device_ID check, or move Device_ID check to after the ISC_ENABLE/X command
SRAM Done bit check is after ISC_DISABLE command	Remove READ_STATUS command
TRACE_ID, Check Busy, Read UserCode commands are used (rare)	Issue ISC_ENABLE_X (SRAM mode) prior to command, then ISC_DISABLE when done.
Design uses Embedded I2C - user has no control over algorithm	User must implement FPGA Design Update, or Contract Lattice for further assistance
I2C User Slave mode could still have marginal timing problem if WISHBONE clock does not meet 7.5x rule	User must implement FPGA Design Update

Appendix 2: Frequently Asked Questions

1. Can Blank devices be programmed via I2C?
    a. Yes. Blank or Erased devices are not in User Mode (DONE is false). Therefore these devices are not affected by the issue.
2. Can programmed devices be re-programmed via I2C?
    a. Yes. Once the device is placed into a valid configuration edit mode, devices are not affected by the issue. However, in typical I2C access flows, some commands are commonly executed prior to entering, or after exiting a valid configuration edit mode (for example, Read Device ID). The FPGA must be updated or the access flows modified per this document.
3. What are the impacted configuration commands?
    a. 0x19 Read Trace ID
    b. 0x3C Read Status (common after Refresh or Disable)
    c. 0xC0 Read Usercode
    d. 0xE0 Read Device ID (common check prior to Erase/Program/Verify etc.)
    e. 0xF0 Check Busy
4. The following relevant documents have already been updated
    a. FPGA-TN-02155: MachXO2 Programming and Configuration User Guide
    b. FPGA-TN-02163: Using User Flash Memory and Hardened Control Functions in MachXO2 Devices Reference Guide
    c. FPGA-TN-02055: MachXO3 Programming and Configuration User Guide
    d. FPGA-TN-02064: Using Hardened Control Functions in MachXO3 Devices Reference Guide
    e. FPGA-TN-02393: MachXO4 Programming and Configuration User Guide
    f. FPGA-TN-02404: MachXO4 Hardened Control Functions Reference Guide
5. How will Radiant and Diamond Design Software help users avoid the issue?
    a. Two new Design Rule Checks (DRCs) will be added. The rules are:
        i. If I2C port is persisted, Diamond software will check if 'wb_clk_i' is connected:
            1. If 'wb_clk_i' is not connected, DRC will Error and stop

2. If ’wb_clk_i’ is connected but the frequency preference for the net is <3.0 MHz, DRC will Warn and continue.

6. Will Radiant and Diamond Programmer change?

    a. Yes. Radiant and Diamond Programmer already added a ‘Recovery' mode to erase the device via I2C without the Device ID check. Once erased, all operations are possible.

7. When will updates for Radiant, Radiant Programmer, Diamond, and Diamond Programmer be available?

    a. The full updates in Diamond and Diamond Programmer have been implemented starting version 3.5, released in May 2015.

    b. For Radiant and Radiant Programmer, partial updates (except the DRC check for the I2C port described in FAQ #5) have been implemented starting version 2025.2, released in December 2025. The remaining DRC rule will be added in version 2026.1, scheduled for release in June 2026.

8. Is the Platform Manager device (LPTM21) affected?

    a. Possibly. If the design was compiled previous to Diamond 3.5, contains no EFB-based IP (e.g. Dual Boot, VID, Fault Log, PMBUS) and requires I2C Background programming, the Customer application is exposed.

9. How do I ensure the EFB and the clock connection do not get optimized away by synthesis?

    a. If the EFB is instantiated with no ports or connections other than ‘wb_clk_i’, most synthesis tools will conclude the circuit is unnecessary (as there are no references to its outputs) and remove both the EFB and the ‘wb_clk_i’ connection from the netlist. To avoid this, generate the EFB with at least one I2C port (e.g. Primary I2C or Configuration I2C) in addition to the WISHBONE port. Then route the EFB ‘i2c1_scl’ and ‘i2c1_sda’ pins to the top level design port list. Routing the I2C port to the top level will have no impact to the original design, as the I2C port pins were necessarily reserved (via persistence) to preserve I2C access from the beginning.

Appendix 3: Decision Tree

Question 1 Does this MachXO2/3/4 design utilize the Primary or Secondary I2C port?

- *Yes: Go to question 2*
- *No: No impact. STOP*

Question 2 Is the Primary I2C port used on a non-blank device for Configuration, Embedded Programming, or UFM access?

- *Yes: Go to question 4*
- *No: Go to question 3*

Question 3 Is the Primary or Secondary I2C port used on as an I2C slave in User mode?

- *Yes: Go to question 4*
- *No: No impact. STOP*

Question 4 Is the EFB Hard IP block instantiated?

- *Yes: Go to question 5*
- *No: Go to question 6*

Question 5 Is the EFB wb_clk_i port connected to an active clock with frequency > 7.5x I2C bus frequency (SCL rate)?

- *Yes: No impact. STOP*
- *No: Go to question 6*

Question 6 Is the design in Production?

- *Yes: Go to question 7*
- *No: "FPGA design update" is recommended. STOP*

Question 7 Is this an XO2 -AIX, XO3, or XO4 design?

- *Yes: "FPGA design update" is recommended. STOP*
- *No: Go to question 8*

Question 8 Is a "FPGA design update" possible?

- *Yes: “FPGA design update” is recommended. STOP*
- *No: Implement "I2C Configuration Update". STOP*