DDR3 Demo for the ECP5/ECP5-5G Versa Development Kit

User Guide

FPGA-UG-02138-1.4

July 2022

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1. Introduction

This document provides technical information and instructions for using the ECP5™ and ECP5-5G™ DDR3 demo design. This demo design demonstrates the functionality of the Lattice DDR3 IP operating core at a speed of 400 MHz and 800 Mbps using the ECP5 Versa Development Board and the ECP5-5G Versa Development Board. This document provides a circuit description of the demo logic as well as instructions for running the DDR3 demo.

The ECP5/ECP5-5G Versa Development Board has an on-board 16-bit DDR3 SDRAM. The demo design generates 16-bit test data, and writes it to the onboard DDR3 SDRAM. The design reads the DDR3 SDRAM data and compares it with original expected data. When there is a mismatch between the standard and read data, the design will flag an error signal. The demo design also allows the user to run the design with different parameters using on-board DIP switches. User Guide.

The demo package includes the following:

- DDR3 IP core configuration files (.sbx)
- Verilog source code for the demo logic design
- Lattice Diamond® implementation project file (.ldf) and preference file (.lpf) for the demo project
- DDR3 demo bitstream file (.bit)

Demo design hardware requirements:

- ECP5/ECP5-5G Versa Development Board with ECP5/ECP5-5G-45 FPGA, 381-ball package
- 12 V DC power supply for the ECP5 Versa Development Board
- Windows PC machine for implementing the demo project and downloading the bitstream
- USB cable for programming the ECP5 device

Demo design software requirements:

- Lattice Diamond design software, version 3.8 or later
- Programmer software for bitstream download

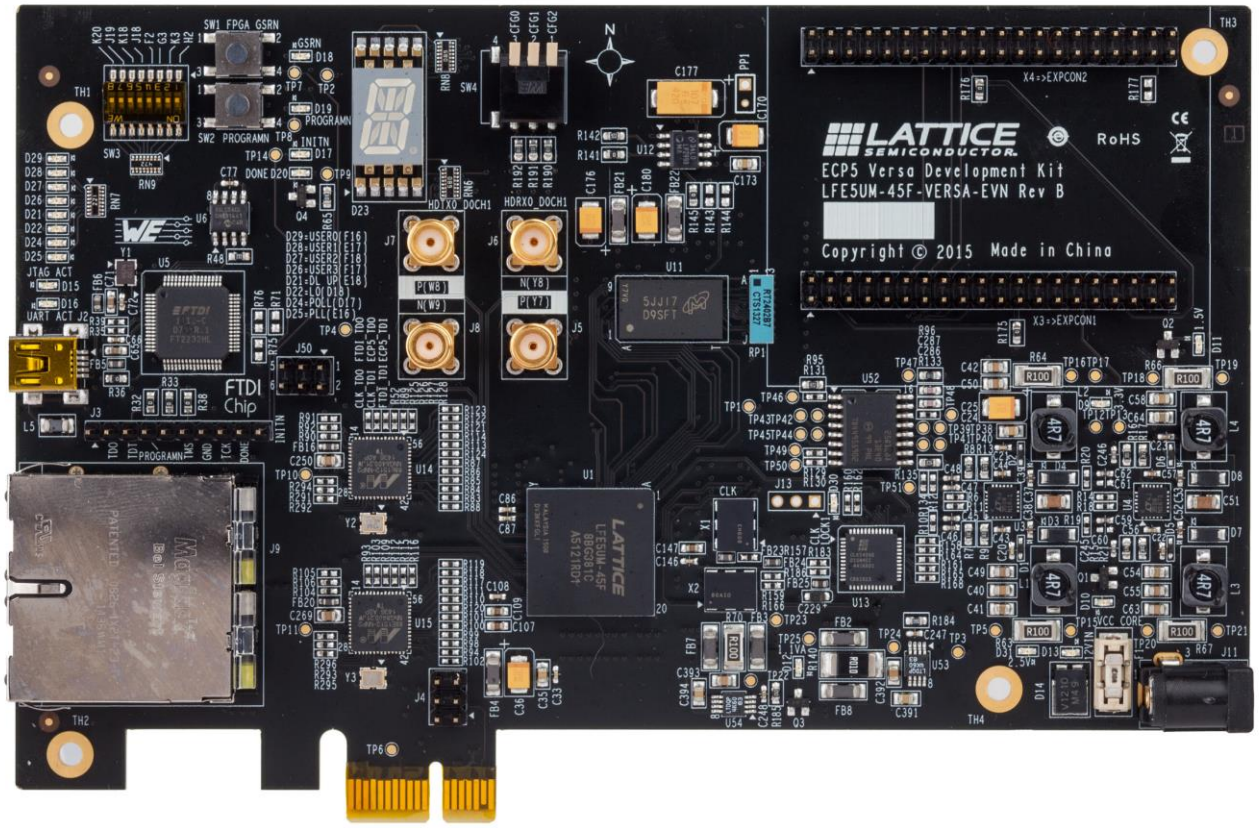

Figure 1.1. ECP5 Versa Development Board

2. DDR3 Demo Design Overview

The DDR3 demo design consists of two major parts: a DDR3 controller IP core and the user logic block. The DDR3 SDRAM Controller IP core interfaces to the on-board external DDR3 SDRAM directly and performs control, read and write operations. The user logic block generates test data to be written to the SDRAM. The DDR3 Controller then writes the data to the on-board DDR3 SDRAM. The DDR3 controller also reads the SDRAM data which it passes to the user logic block. The user logic block compares the read data with the expected data and flags an error if it detects a data mismatch. The demo parameters can be modified using on-board DIP switches. The status of the running demo design is indicated with on-board LEDs.

Further sections describe the sub-modules in the user logic design in detail. Figure 2.1 illustrates a block diagram of the demo design.

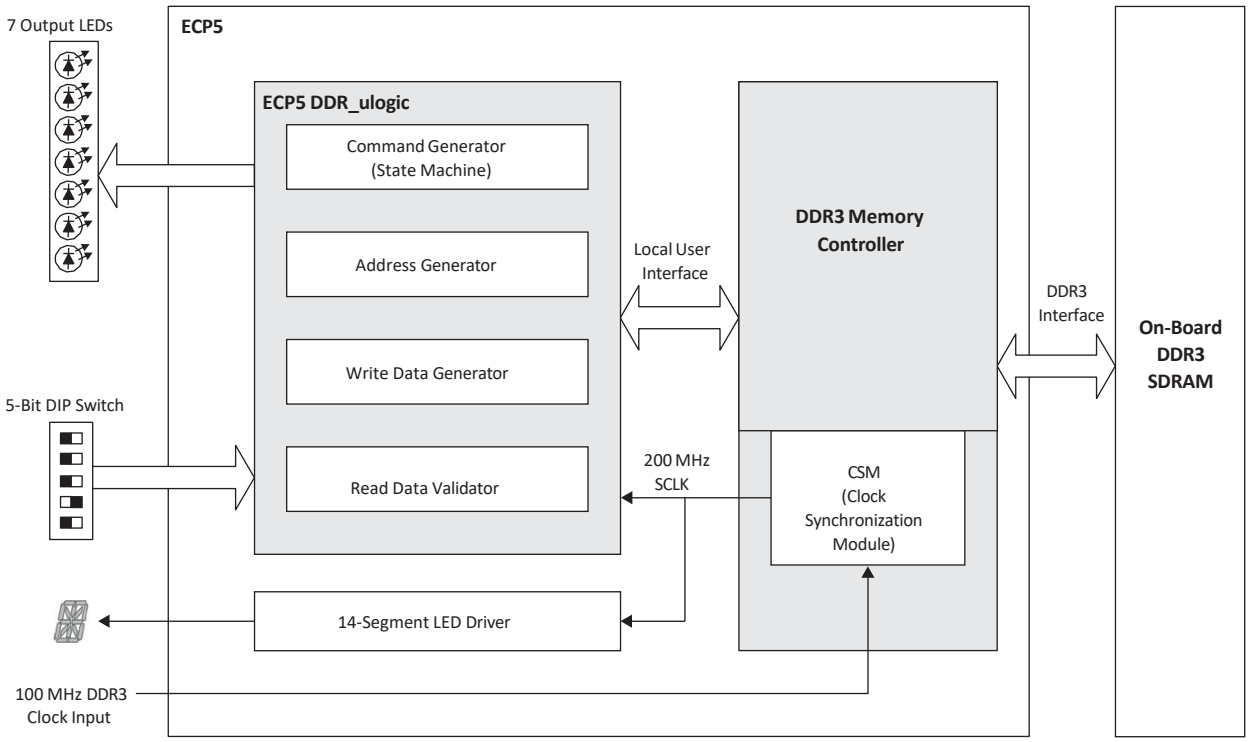

Figure 2.1. DDR3 Demo Design Block Diagram

2.1. DDR3 SDIP Core

This demo is supplied with a fully generated DDR3 SDRAM Controller IP core. The IP core used to generate the DDR3 controller core is the DDR3 SDRAM Controller IP core, version 3.1. The user must install version 3.0 before updating and generating the IP core in the demo project. Double Data Rate (DDR3) SDRAM Controller IP Core User Guide (FPGA-IPUG-02047) for details on generating the IP Core. The controller generated with this IP core interfaces directly with the external, on-board DDR3 SDRAM and performs control operations. The demo has been designed to support a DDR3 data bus width of 16 bits since the DDR3 memory module installed in the ECP5/ECP5-5G Versa Development Board is 16 bits wide.

2.2. User Logic

The user logic implemented in the DDR3 demo design provides the following functions:

- Command Generation State machine programs the mode registers and controls DDR3 read and write operations
- Address generation
- Write data generation
- Read data validation
- Control and observation

2.2.1. Command Generator State Machine

The state machine controls the demo using the user control input through 5 switch inputs (part of the 8-bit DIP switch on the ECP5/ECP5-5G Versa Development Board). Once the ECP5/ECP5-5G device is programmed or a system reset is applied by pressing the GSR button, the state machine programs all DDR3 mode registers (MR0~MR3) based on the user test configuration (DIP switch setting) – see Table 4.3 for details on the configuration settings. Then, it generates a write command sequence. The write command may be repeated up to 32 times using either the command burst feature or multiples of single write commands depending on the user setting. After the write command sequence, a read command sequence is initiated. The read command sequence may also be repeated up to 32 times in the same way as the write command sequence. The read command sequence that follows the write command sequence always includes the same number of commands as the write command sequence. The state machine makes sure that both the write and the following read command sequences are always the same even when the user test configuration is changed at any time during the command sequences. This allows the DDR3 demo to be dynamically reconfigurable.

2.2.2. Address Generation

The address generation block provides the start address for the current user read/write command which is generated by the state machine. When the burst command mode is enabled, the address generation block automatically calculates the next address according to the demo control input.

2.2.3. Write Data Generation

The demo uses either PRBS or sequential data patterns. When PRBS is selected, a 128-bit PRBS pattern generator is connected to the local write data bus to generate a 16-bit DDR3 data pattern. For 16-bit DDR3 data, the lower 64 bits [63:0] of the 128-bit PRBS are allocated to the local data bus. For the sequential data pattern, the demo design uses only a 32-bit sequential data pattern generator to provide 16-bit DDR3 data. This 32-bit data pattern is allocated to each 32-bit wide local data bus slot. For example, a 16-bit DDR3 bus requires a 64-bit local data bus which has two identically sequenced 32-bit patterns allocated on two 32-bit slots. The write data generation is enabled and driven by the datain_rdy signal assertions.

2.2.4. Read Data Validation

The Read Data Validator checks the read data from the DDR3 memory module. To do this, it generates the expected data patterns using exactly the same data sequences as the Write Data Generator block. The expected data generation is enabled and driven by the read_data_valid signal assertions. The read data captured by read_data_valid is compared with the expected data generated by the Read Data Validator block. When there is a mismatch between both data patterns, the demo design will flag the error detection signal.

2.2.5. Control and Observation

The Control and Observation block includes the demo control input and result display functions. The demo control input uses five out of eight DIP switches available on the ECP5/ECP5-5G Versa Development Board. The demo result is displayed through seven LEDs on the board. See the following section for descriptions of the demo control input switches and the result display LEDs. A 14-segment LED display is also provided for a quick assessment of the operation. When the read and write operation is running and there is no data mismatch, the segments of the display blink in a clockwise pattern. The blink rate is dependent on the amount of data that is read. As soon as an error is detected, all 14 segments blink simultaneously.

3. ECP5/ECP5-5G Versa Development Board

This section describes the ECP5/ECP5-5G Versa Development Board as it relates to the DDR3 demo.

3.1. DDR3 Memory

The ECP5/ECP5-5G Versa Development Board has on-board 16-bit DDR3 memory. The DDR3 memory module on the board that is used for the DDR3 demo is a 96-pin unbuffered DDR3 SDRAM. The demo design uses up to 1GB of memory space with one chip select configuration.

3.2. Programming Cable Connections

The ECP5/ECP5-5G device on the ECP5/ECP5-5G Versa Development Board can be programmed over JTAG through the USB port. This path can both program the device and be used with the Reveal™ logic analyzer to trace internal signal paths. The J50 header needs to be configured to enable the USB-to-JTAG path used by this demo. The instructions to set up the ECP5/ECP5-5G Versa Development Board for use with this demo are discussed later in this document.

4. Port Assignments and Descriptions

Table 4.1 lists all the signals used by the DDR3 SDRAM Controller IP core in the demo design to control and interface to the on-board DDR3 SDRAM. For details, refer to Double Data Rate (DDR3) SDRAM Controller IP Core User's Guide (FPGA-IPUG-02047).

Table 4.2 lists all the interfaces which are available to the user to either dynamically configure the parameters of the design (input mode) or observe the running status of the demo (output mode).

Table 4.1. DDR3 Bus Interface

Port Name	Active	Direction	Description
em_ddr_reset_n	Low	Output	Asynchronous reset signal from the controller to the memory device. Asserted by the controller for the duration of power on reset or GSR_N
em_ddr_clk[CLKO_WIDTH-1:0]	N/A	Output	400 MHz memory clock generated by the controller
em_ ddr_clk_n[CLKO_WIDTH-1:0]	N/A	Output	400 MHz complimentary memory clock generated by the controller
em_ ddr_cke[CKE_WIDTH-1:0]	High	Output	Memory clock enable generated by the controller
em_ ddr_addr[ROW_WIDTH-1:0]	N/A	Output	Memory address bus, multiplexed row and column address for the memory
em_ ddr_ba[2:0]	N/A	Output	Memory bank address
em_ ddr_data[DATA_WIDTH-1:0]	N/A	In/Out	Memory bi-directional data bus
em_ ddr_dm[(DATA_WIDTH/8)-1:0]	High	Output	DDR3 memory write data mask
em_ ddr_dqs[DQS_WIDTH-1:0]	N/A	In/Out	Memory bi-directional data strobe
em_ ddr_dqs_n[DQS_WIDTH-1:0]	N/A	In/Out	Memory complementary bi-directional data strobe
em_ ddr_cs_n[CS_WIDTH-1:0]	Low	Output	Memory chip select
em_ ddr_cas_n	Low	Output	Memory column address strobe
em_ ddr_ras_n	Low	Output	Memory row address strobe
em_ ddr_we_n	Low	Output	Memory write enable
em_ ddr_odt[CS_WIDTH-1:0]	High	Output	Memory on-die termination control

Table 4.2. Demo User Interface Ports

Port Name	Active	Direction	Description
Clk_in	N/A	Input	Reference clock connected to a dedicated PLL clock input of the ECP5/ECP5-5G FPGA.
Reset_n	Low	Input	Asynchronous reset connected to the GSRN button (SW1). This resets the entire demo system including the DDR3 IP core when asserted.
seg[14:0]	N/A	Output	14-Segment LED Display. The segments of the 14-segment display (D23) blink in a clockwise pattern as long as no data mismatch has occurred. As soon as a data mismatch occurs, all the LED segments blink together in Alarm mode. A system reset must be applied to restart the transactions.
Dip_sw[4:0]	N/A	Input	User test configuration input. See the Control and Observation Port Description section of this document for further information.
Oled[6:0]	N/A	Output	Demo result LED indicator output. See the Control and Observation Port Description section of this document for further information.

4.1. Control and Observation Port Descriptions

The Control and Observation Ports include the user interface ports as described in Table 4.2. This section describes in detail the two main control (DIP switch) and observation (LED) ports. Table 4.3 describes the functionality of each DIP switch on SW3 and how design parameters can be changed by changing the position of the switches. The recommended default setting for the DIP switch is for all switches to be in the OFF position. The ON position is when the DIP switch level is towards ON which is printed on the DIP Switch case.

Table 4.3. SW3 DIP Switch Definitions

Signal Name	DIP Switch Number	Assigned Function Control	DIP Switch Setting	Description
dip_sw[0]	SW3-1	Burst Length Selection	OFF	Set Burst Length to BL8
			ON	Set Burst Length to BC4
dip_sw[1]	SW3-2	On-the-Fly (OTF) Mode	OFF	Fixed burst size mode. The core is set to BL8 or BC4 during initialization depending on the Burst Length Selection setting.
			ON	OTF mode. Dynamic burst length change is controlled by the Burst Length Selection switch.
dip_sw[2]	SW3-3	Command Burst Disable	OFF	Enable command burst mode.
			ON	Disable command burst mode. Demo works in the single command mode. Manual single command repetitions are performed instead of using the command burst mode.
dip_sw[3]	SW3-4	Maximum Command Size	OFF	Use maximum command burst size/repetition The DDR3 core performs a 32 command burst (Command Burst Enabled) or the demo logic generates 32 consecutive single commands (Command Burst Disabled).
			ON	Use user-specified command burst size Both the command burst and single command repetition modes use the burst size value (UsrCmdBrstCnt) defined in the ddr3_test_params.v file. The allowed values are 2, 4, 8, 16 or 32 with the default value set to 2.
dip_sw[4]	SW3-5	Data Mode	OFF	PRBS data patterns are used for the DDR3 demo. 128-bit pseudo random patterns are generated. In this demo (16-bit DDR3 SDRAM), the lower half [63:0] of the 128-bit PRBS data is used for the 64 bit local data bus.
			ON	Sequential data patterns. 32-bit sequential data pattern generators are used. For example, the 16-bit DDR3 demo has two 32-bit sequential patterns allocated to each 32-bit slot on a local data bus.

4.2. Output Status LEDs

Seven LEDs are used to indicate the demo progress and results. In Table 4.4, the Reference Designator column shows the diode reference designator printed on the ECP5/ECP5-5G Versa Development Board. Each LED indicates a particular status or condition of the DDR3 demo design, DDR3 controller core to be specific.

Table 4.4. Output LED Definitions

Signal Name	Reference Designator	Function	Status	Description
OLED[0]	D25	Heartbeat indicator	Blink	The board is alive, and the core is receiving the clock input
			OFF	The core is unable to receive the clock signal
OLED[1]	D24	DDR3 Transaction Indicator	Blink	DDR3 write-then-read operations are occurring. The more read data that comes in, the faster this LED blinks
			OFF	No valid read data is detected
OLED[2]	D22	Valid data indicator	Blink	Proper DDR3 read/write transactions are being performed with actual valid data.
			OFF	Received data is null (all '0' or '1').
	D21	Not used		
OLED[3]	D26	Error Indicator	Blink	The first data mis-match error is detected. A system reset must be applied to clear this indicator.
			OFF	No error detected
OLED[4]	D27	INIT done and core ready indicator	ON	The core and memory initialization are complete, and the core is ready to accept user commands.
			OFF	The core is not ready to accept new command
OLED[5]	D28	Write indicator	ON	The core's write operation is properly working by detecting the datain_rdy signal assertions
			OFF	The core is not ready to receive write data from the user
OLED[6]	D29	Read indicator	ON	The core's read operation is properly working by detecting the read_data_valid signal assertions.
			OFF	Indicates invalid data on read-data bus

Table 6.1 indicates the status of all LEDs during successful operation of the demo.

5. Demo Package Directory Structure

The bitstream folder contains the demo bitstream for the ECP5 Versa Development Board as well as for the ECP5-5G Versa Development Board. The DDR3_ project folder contains two subfolders:

- DDR3_ECP5 (Demo design for ECP5 Versa Development Board)
- DDR3_ECP5_5G (Demo design for ECP5-5G Versa Development Board)

The subfolder ddr3_ecp5_impl is the implementation folder for ECP5 Versa Development Kit and ddr3_ecp5_5G_impl is the implementation folder for ECP5-5G Versa Development Kit. The subfolder src contains all the source files other than IP core. The subfolder ddr3_ip_inst is the generated IP core using Clarity Designer.

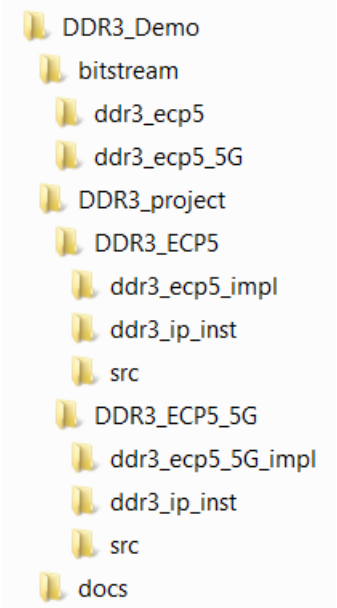

Figure 5.1. DDR3 Demo Package Directory Structure

6. Running the Demo

To run the demo:

1. Before the board is powered up:
   a. J50 should have pin #1 jumpered to pin #2, and pin #3 jumpered to pin #5. This puts ECP5/ECP5-5G in the JTAG scan chain as the only device.
   b. DIP switch SW3 should have all positions in OFF position.
2. Power up the board with 12 V power supply. Connect the board to a PC with a USB cable.
3. Launch the Diamond Programmer software.

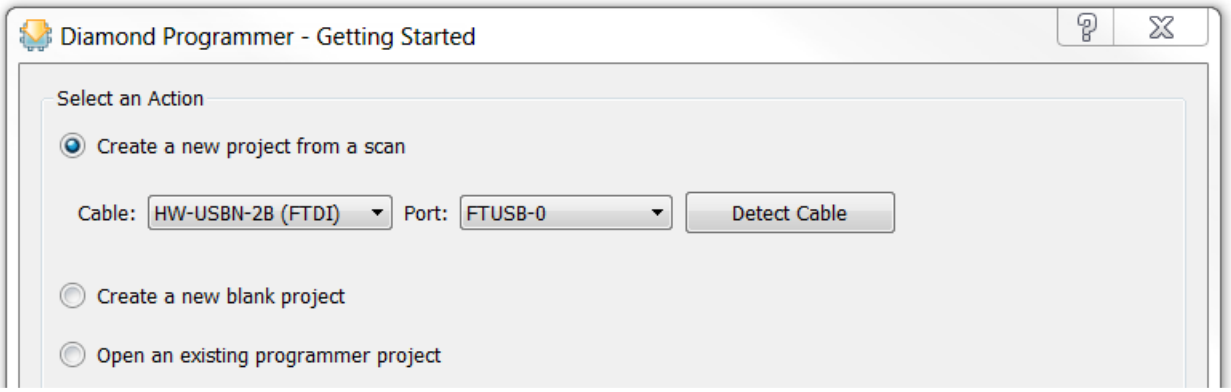

Figure 6.1. Getting Started

4. If the device is not detected, scan the JTAG chain by selecting the Scan button.
5. Select the **LFE5UM-45F** device.

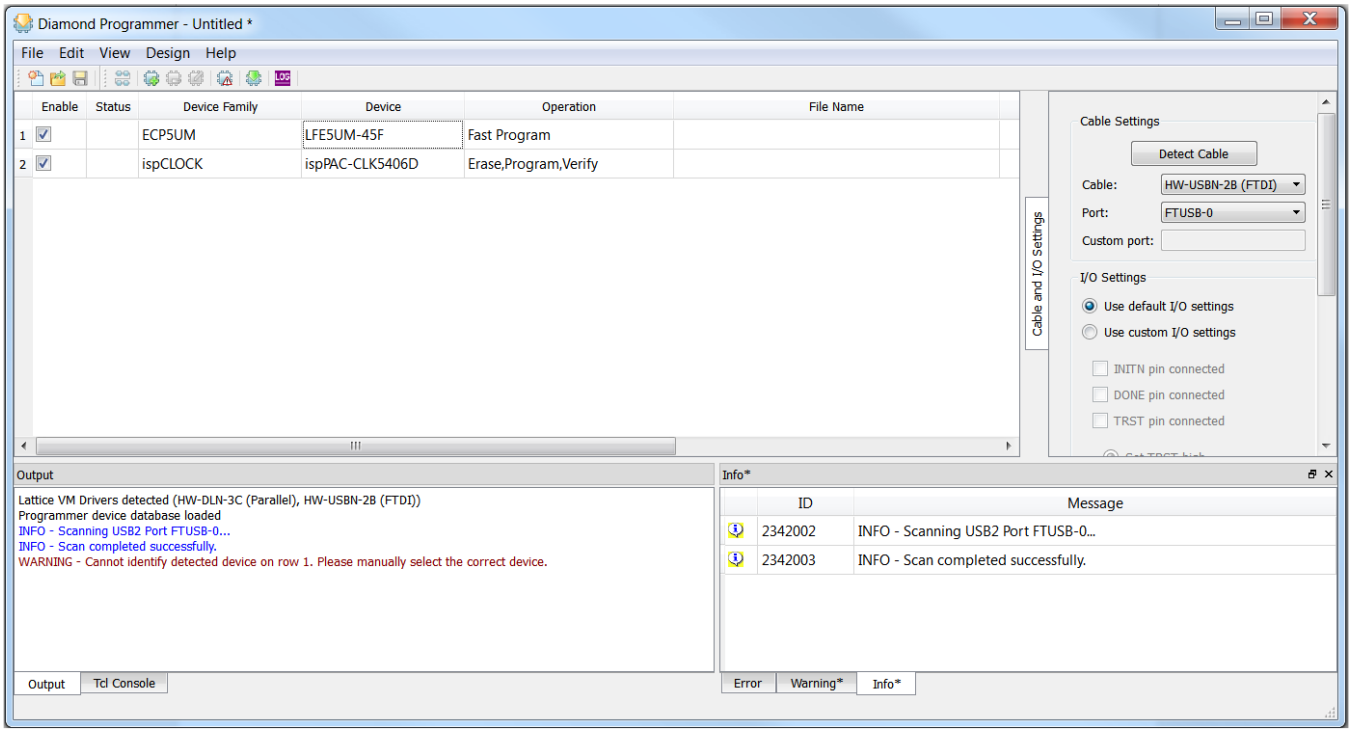

Figure 6.2. Selecting the Device

6. Select **Fast Program** and the bitstream **DDR3_demo\bitstream\ddr3_ecp5.bit** to be programmed, then start programming the device.

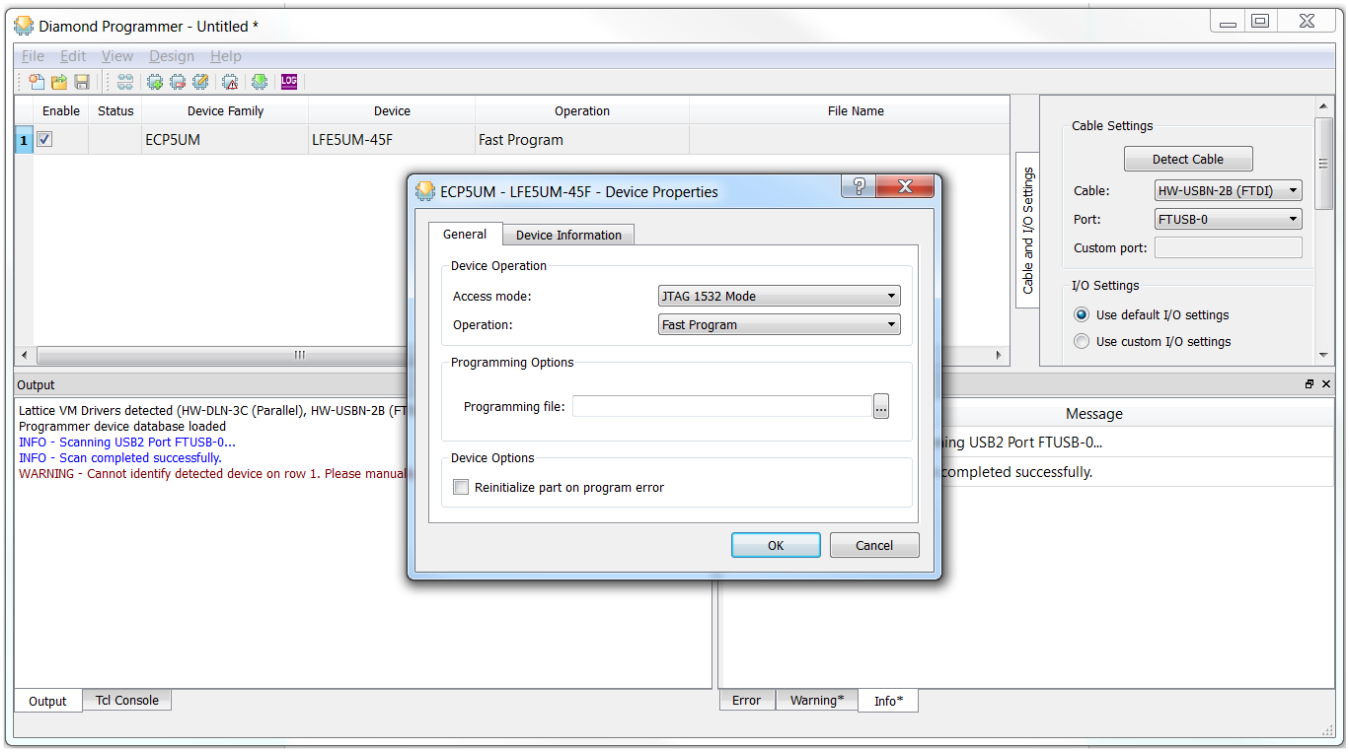

Figure 6.3. Device Properties

Status LEDs on the board should be illuminated or blinking once the FPGA programming is completed.

7. Refer to Table 6.1 to verify whether LEDs are blinking as mentioned. If the red LED-D26 (Error) blinks and all segments of 14-segment display blink together, press the GSRN button (SW1) to clear the error counter and reset the design.

Table 6.1. Expected LED Status from Successful Demo

Name	Expected Status	Remark
D23 (Segment LED)	Rotating clockwise and character “0” pulse	Character “0” pulse rate is about 45 beats per second with SW3 all OFF position
D25	Blink	Yellow LED with constant blinking rate
D24	Blink	Yellow LED
D22	Blink	Green LED
D21	OFF	
D26	OFF	
D27	ON	Red LED
D28	ON	Red LED
D29	ON	Red LED

7. Demo Design Dependencies per Development Board Revision

For the ECP5 Demo, the bitstream included with the demo design has been developed for the ECP5 Versa Development Board Revision B. The key updates to the Revision B development board with respect to the DDR3 demo include the following:

1. The ECP5 pinout with respect to the on-board DIP switches and LEDs has been updated for Revision B of the hardware. Specifically the SEG1 assignment in the demo project is location L18 for Revision B. SEG1 is assigned to location L19 for Revision A.
2. The demo bitstreams have been built with Diamond 3.8 for use with Revision B of the ECP5 Versa Development Board. The demo project must be rebuilt with Diamond 3.4 for use with Revision A.

8. References

- ECP5-5G Family Data Sheet (FPGA-DS-02012)
- Double Data Rate (DDR3) SDRAM Controller IP Core User Guide (FPGA-IPUG-02047)
- ECP5 Versa Development Board User Guide (FPGA-EB-02021)
- ECP5-5G Versa Development Board User Guide (FPGA-EB-02048)

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Revision 1.4, July 2022

Section	Change Summary
All	• Changed title from "DDR3 Demo for the ECP5 and ECP5-5G Versa Development Board" to "DDR3 Demo for the ECP5/ECP5-5G Versa Development Kit". • Updated document template.
Running the Demo	Merged steps 6 and 7.

Revision 1.3, October 2021

Section	Change Summary
All	• Changed document number from UG97 to FPGA-UG-02138. • Updated document numbers of referenced data sheet and user guides.
Disclaimer	Added Disclaimers section.

Revision 1.2, October 2016

Section	Change Summary
All	• Document title changed to DDR3 Demo for the ECP5™ and ECP5-5G™ Versa Development Boards User Guide. • Added support for ECP5-5G Versa Development Board. • Updated the demo package directory structure. • Updated Diamond version to 3.8.
References	Added EB103 to References section.

Revision 1.1, August 2015

Section	Change Summary
All	Added support for ECP5 Versa Development Board Rev B.
Technical Support Assistance	Updated Technical Support Assistance section.

Revision 1.0, April 2015

Section	Change Summary
All	Initial release.

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