LatticeMico Slave Passthrough

The LatticeMico slave passthrough provides a data path between the internal WISHBONE bus and the external WISHBONE slave devices.

Version

This document describes the 3.3 version of the LatticeMico slave passthrough.

Functional Description

The LatticeMico slave passthrough provides a data path between the internal WISHBONE bus and the external WISHBONE slave devices. It connects the output of the external WISHBONE slave to the input of the internal WISHBONE bus, and connects the output of the internal WISHBONE bus to the input of the external WISHBONE slave.

Configuration

The following sections describe the graphical user interface (UI) parameters and the I/O ports that you can use to configure and operate the LatticeMico slave passthrough.

UI Parameters

Table 1 shows the UI parameters available for configuring the LatticeMico SPI through the Mico System Builder (MSB) interface.

Table 1: LatticeMico Master Passthrough UI Parameters

Dialog Box Option	Description	Allowable Values	Default Value
Instance Name	Specifies the name of the slave passthrough instance.	Alphanumeric and underscores	slave_passthru
Base Address	Specifies the base address of the device. The minimum boundary alignment is 0X4.	0X80000000 – 0XFFFFFFF0	0X80000000
Size	Specifies the size of the slave passthrough, in bytes.		256
Data Bus Width	Specifies the data bus width for WISHBONE configuration.	8, 32	32

I/O Ports

Table 2 describes the input and output ports of the LatticeMico slave passthrough.

Table 2: LatticeMico Slave Passthrough I/O Port Descriptions

I/O Port	Active	Direction	Initial State	Description
WISHBONE Side Signals				
CLK_I	–	I	0	System clock signal
RST_I	High	I	0	System reset signal
S_CTI_I	–	I	0	Cycle-type identification signal
S_BTE_I	–	I	0	Burst-type extension signal
S_ADR_I	–	I	0	WISHBONE address bus signal
S_DAT_I	–	I	0	WISHBONE data bus input
S_SEL_I	High	I	0	Select output array signal, one bit for every byte
S_WE_I	High	I	0	Write enable signal
S_STB_I	High	I	0	Strobe signal indicating a valid data transfer
S_CYC_I	High	I	0	Signal indicating a valid bus cycle in progress
S_LOCK_I	High	I	0	When asserted, indicates that the current bus cycle is uninterruptible
S_DAT_O	–	O	0	WISHBONE data bus output

Table 2: LatticeMico Slave Passthrough I/O Port Descriptions (Continued)

I/O Port	Active	Direction	Initial State	Description
S_ACK_O	High	O	0	Signal indicating the normal termination
S_RTY_O	High	O	0	Indicates that the interface is not ready to accept or send data and that the cycle should be retried
S_EBR_O	High	O	0	Signal indicating abnormal cycle termination
INTR_O	High	O	0	WISHBONE interrupt signal
Slave Passthrough Interface				
clk	–	O	0	External slave clock
rst	High	O	0	External slave reset
slv_adr	–	O	0	External slave address bus signal
slv_master_data	–	O	0	External slave data bus input
slv_we	High	O	0	External slave write enable signal
slv_stb	High	O	0	External slave strobe signal indicating a valid data transfer
slv_cyc	High	O	0	External slave signal indicating a valid bus cycle in progress
slv_lock	High	O	0	When asserted, indicates that the current bus cycle is uninterruptible
slv_cti	–	O	0	External slave cycle type identification signal
slv_sel	High	O	0	Select output array signal, one bit for every byte
slv_bte	–	O	0	Burst-type extension signal
slv_slave_data	–	I	0	External slave data bus output
slv_ack	High	I	0	Signal indicating normal termination
slv_rty	High	I	0	Signal indicating retry termination
slv_err	High	I	0	Signal indicating error termination

Revision History

Component Version	Description
3.0 (7.0 SP2)	Initial release.
3.1	Support for 8/32-bit WISHBONE Data Bus.

Revision History (Continued)

Component Version	Description
3.2	Support added to LatticeMico32 and LatticeMico8 drivers that enable user-defined interrupt handling.
3.2	Updated document with new corporate logo.
3.3	Fixed parameter settings for 8-bit data bus. Component can be used in designs that do not include a processor.

.

Trademarks