LatticeMico Memory Passthrough

The LatticeMico memory passthrough provides a data path between the internal WISHBONE bus and the external WISHBONE memory devices.

Version

This document describes the 3.1 version of the LatticeMico memory passthrough.

Functional Description

The LatticeMico memory passthrough provides a data path between the internal WISHBONE bus and the external WISHBONE memory devices. It connects the output of the external WISHBONE memory to the input of the internal WISHBONE bus, and connects the output of the internal WISHBONE bus to the input of the external WISHBONE memory.

Configuration

The following sections describe the graphical user interface (UI) parameters and the I/O ports that you can use to configure and operate the LatticeMico memory passthrough.

UI Parameters

Table 1 shows the UI parameters available for configuring the LatticeMico Memory Passthrough through the Mico System Builder (MSB) interface.

Table 1: LatticeMico Memory Passthrough UI Parameters

Dialog Box Option	Description	Allowable Values	Default Value
Instance Name	Specifies the name of the memory passthrough instance.	Alphanumeric and underscores	memory_passthru
Base Address	Specifies the base address of the device. The minimum boundary alignment is 0X4.	0X00000000 – 0X7FFFFFFF	0X00000000
Size	Specifies the size of the memory passthrough, in bytes.		256
Data Bus Width	Specifies the data bus width for WISHBONE configuration.	8, 32	32

I/O Ports

Table 2 describes the input and output ports of the LatticeMico memory passthrough.

Table 2: LatticeMico Memory Passthrough I/O Port Descriptions

I/O Port	Active	Direction	Initial State	Description
WISHBONE Side Signals				
CLK_I	–	I	0	System clock signal
RST_I	High	I	0	System reset signal
MEM_CTI_I	–	I	0	Cycle-type identification signal
MEM_BTE_I	–	I	0	Burst-type extension signal
MEM_ADR_I	–	I	0	WISHBONE address bus signal
MEM_DAT_I	–	I	0	WISHBONE data bus input
MEM_SEL_I	High	I	0	Select output array signal, one bit for every byte
MEM_WE_I	High	I	0	Write enable signal
MEM_STB_I	High	I	0	Strobe signal indicating a valid data transfer
MEM_CYC_I	High	I	0	Signal indicating a valid bus cycle in progress
MEM_LOCK_I	High	I	0	When asserted, indicates that the current bus cycle is uninterruptible

Table 2: LatticeMico Memory Passthrough I/O Port Descriptions (Continued)

I/O Port	Active	Direction	Initial State	Description
MEM_DAT_O	–	O	0	WISHBONE data bus output
MEM_ACK_O	High	O	0	Signal indicating the normal termination
MEM_RTY_O	High	O	0	Indicates that the interface is not ready to accept or send data and that the cycle should be retried
MEM_EBR_O	High	O	0	Signal indicating abnormal cycle termination
Memory Passthrough Interface				
clk	–	O	0	External memory clock
rst	High	O	0	External memory reset
mem_adr	–	O	0	External memory address bus signal
mem_master_data	–	O	0	External memory data bus input
mem_we	High	O	0	External memory write enable signal
mem_stb	High	O	0	External memory strobe signal indicating a valid data transfer
mem_cyc	High	O	0	External memory signal indicating a valid bus cycle in progress
mem_lock	High	O	0	When asserted, indicates that the current bus cycle is uninterruptible
mem_cti	–	O	0	External memory cycle type identification signal
mem_sel	High	O	0	Select output array signal, one bit for every byte
mem_bte	–	O	0	Burst-type extension signal
mem_slave_data	–	I	0	External memory data bus output
mem_ack	High	I	0	Signal indicating normal termination
mem_rty	High	I	0	Signal indicating retry termination
mem_err	High	I	0	Signal indicating error termination

Revision History

Component Version	Description
3.0	Initial release.
3.0	Updated document with new corporate logo.
3.1	Fixed parameter settings for 8-bit data bus. Component can be used in designs that do not include a processor. Corrected base address in Table 1.

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Trademarks