LatticeMico Master Passthrough

The LatticeMico master passthrough provides a data path between the internal WISHBONE bus and the external WISHBONE master devices.

Version

This document describes the 3.3 version of the LatticeMico master passthrough.

Functional Description

The LatticeMico master passthrough provides a data path between the internal WISHBONE bus and the external WISHBONE master devices. It connects the output of the external WISHBONE master to the input of the internal WISHBONE bus, and connects the output of the internal WISHBONE bus to the input of the external WISHBONE master.

Configuration

The following sections describe the graphical user interface (UI) parameters and the I/O ports that you can use to configure and operate the LatticeMico master passthrough.

UI Parameters

Table 1 shows the UI parameters available for configuring the LatticeMico SPI through the Mico System Builder (MSB) interface.

Table 1: LatticeMico Master Passthrough UI Parameters

Dialog Box Option	Description	Allowable Values	Default Value
Instance Name	Specifies the name of the master passthrough instance.	Alphanumeric and underscores	master_passthru
Data Bus Width	Specifies the data bus width for WISHBONE configuration.	8, 32	32

I/O Ports

Table 2 describes the input and output ports of the LatticeMico master passthrough.

Table 2: LatticeMico Master Passthrough I/O Port Descriptions

I/O Port	Active	Direction	Initial State	Description
WISHBONE Side Signals				
CLK_I	–	I	0	System clock signal
RST_I	High	I	0	System reset signal
M_CTI_0	–	O	0	Cycle-type identification signal
M_BTE_O	–	O	0	Burst-type extension signal
M_ADR_O	–	O	0	WISHBONE address bus signal
M_DAT_O	–	O	0	WISHBONE data bus output
M_SEL_O	High	O	0	Select output array signal, one bit for every byte
M_WE_O	High	O	0	Write enable signal
M_STB_O	High	O	0	Strobe signal indicating a valid data transfer
M_CYC_O	High	O	0	Signal indicating a valid bus cycle in progress
M_LOCK_O	High	O	0	When asserted, indicates that the current bus cycle is uninterruptible
M_DAT_I	–	I	0	WISHBONE data bus input
M_ACK_I	High	I	0	Signal indicating normal termination
M_RTY_I	High	I	0	Indicates that the interface is not ready to accept or send data and that the cycle should be retried

Table 2: LatticeMico Master Passthrough I/O Port Descriptions (Continued)

I/O Port	Active	Direction	Initial State	Description
M_EBR_I	High	I	0	Signal indicating abnormal cycle termination
Master Passthrough Interface				
clk	–	O	0	External master clock
rst	High	O	0	External master reset
mstr_adr	–	I	0	External master address bus signal
mstr_dat_to_slv	–	I	0	External master data bus output
mstr_we	High	I	0	External master write enable signal
mstr_stb	High	I	0	External master strobe signal indicating a valid data transfer
mstr_cyc	High	I	0	External master signal indicating a valid bus cycle in progress
mstr_lock	High	I	0	When asserted, indicates that the current bus cycle is uninterruptible
mstr_cti	–	I	0	External master cycle type identification signal
mstr_sel	High	I	0	Select output array signal, one bit for every byte
mstr_bte	–	I	0	Burst-type extension signal
mstr_dat_from_slv	–	O	0	External master data bus input
mstr_ack_from_slv	High	O	0	Signal indicating normal termination
mstr_rty_from_slv	High	O	0	Signal indicating retry termination
mstr_err_from_slv	High	O	0	Signal indicating error termination

Revision History

Component Version	Description
3.0 (7.0 SP2)	Initial release.
3.1 (7.2 SP1	Removal of base address parameter.
3.2	Support for 8/32-bit WISHBONE Data Bus.
3.2	Updated document with new corporate logo.
3.3	Fixed parameter settings for 8-bit data bus. Component can be used in designs that do not include a processor.

Trademarks