ECP5 Product Family Qualification Summary

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1.0 INTRODUCTION

The ECP5 family of FPGA devices is optimized to deliver high performance features such as an enhanced DSP architecture, high speed SERDES and high speed source synchronous interfaces in an economical FPGA fabric. This combination is achieved through advances in device architecture and the use of 40nm technology making the devices suitable for high-volume, high-speed, low-cost applications.

The ECP5 device family covers look-up-table (LUT) capacity to 84K logic elements and supports up to 365 user I/Os. The ECP5 device family also offers up to 156 18 x 18 multipliers and a wide range of parallel I/O standards.

The ECP5 FPGA fabric is optimized high performance with low power and low cost in mind. The ECP5 devices utilize reconfigurable SRAM logic technology and provide popular building blocks such as LUT-based logic, distributed and embedded memory, Phase Locked Loops (PLLs), Delay Locked Loops (DLLs), pre-engineered source synchronous I/O support, enhanced sysDSP slices and advanced configuration support, including encryption and dual-boot capabilities.

The pre-engineered source synchronous logic implemented in the ECP5 device family supports a broad range of interface standards, including DDR2/3, LPDDR2/3, XGMII and 7:1 LVDS.

The ECP5 device family also features high speed SERDES with dedicated PCS functions. High jitter tolerance and low transmit jitter allow the SERDES plus PCS blocks to be configured to support an array of popular data protocols including PCI Express, SMPTE, Ethernet (XAUI, GbE, and SGMII) and CPRI. Transmit De-emphasis with pre- and post-cursors, and Receive Equalization settings make the SERDES suitable for transmission and reception over various forms of media.

The ECP5 devices also provide flexible, reliable and secure configuration options, such as dual-boot capability, bitstream encryption, and TransFR field upgrade features.

The Lattice Diamond™ design software allows large complex designs to be efficiently implemented using the ECP5 FPGA family. Synthesis library support for ECP5 devices is available for popular logic synthesis tools. The Diamond tools use the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the ECP5 device. The tools extract the timing from the routing and back-annotate it into the design for timing verification.

Lattice provides many pre-engineered IP (Intellectual Property) modules for the ECP5 family. By using these configurable soft core IPs as standardized blocks, designers are free to concentrate on the unique aspects of their design, increasing their productivity.

Table 1.0.1 ECP5 Product Family Attributes

PRODUCT NAME	LFE5UM/5G-25	LFE5UM/5G-45	LFEUM/5G-85	LFE5U-12/25	LFE5U-45	LFE5U-85
LUTs (K)	24	44	84	24	44	84
Packages I/O						
0.5 mm Spacing I/O Count / SERDES						
285 csfBGA (10x10 mm)	118 / 2	118 / 2	118 / 2	118 / 0	118 / 0	118 / 0
0.8 mm Spacing I/O Count / SERDES						
256 caBGA (14x14 mm)				197 / 0	197 / 0	
381 caBGA (17x17 mm)	197 / 2	203 / 4	205 / 4	197 / 0	203 / 0	205 / 0
554 caBGA (23x23 mm)		245 / 4	259 / 4		245 / 0	259 / 0
756 caBGA (27x27 mm)			365 / 4			365 / 0

2.0 LATTICE PRODUCT QUALIFICATION PROGRAM

Lattice Semiconductor Corp. maintains a comprehensive reliability qualification program to assure that each product achieves its reliability goals. After initial qualification, the continued high reliability of Lattice products is assured through ongoing monitor programs as described in Lattice Semiconductor's Reliability Monitor Program Procedure (Doc. #101667). All product qualification plans are generated in conformance with Lattice Semiconductor's Qualification Procedure (Doc. #100164) with failure analysis performed in conformance with Lattice Semiconductor's Failure Analysis Procedure (Doc. #100166). Both documents are referenced in Lattice Semiconductor's Quality Assurance Manual, which can be obtained upon request from a Lattice Semiconductor sales office. Figure 2.1 shows the Product Qualification Process Flow.

If failures occur during qualification, an 8D process is used to find root cause and eliminate the failure mode from the design, materials, or process. The effectiveness of any fix or change is validated through additional testing as required. Final testing results are reported in the qualification reports.

Failure rates in this reliability report are expressed in FITs. Due to the very low failure rate of integrated circuits, it is convenient to refer to failures in a population during a period of 10^9 device hours; one failure in 10^9 device hours is defined as one FIT.

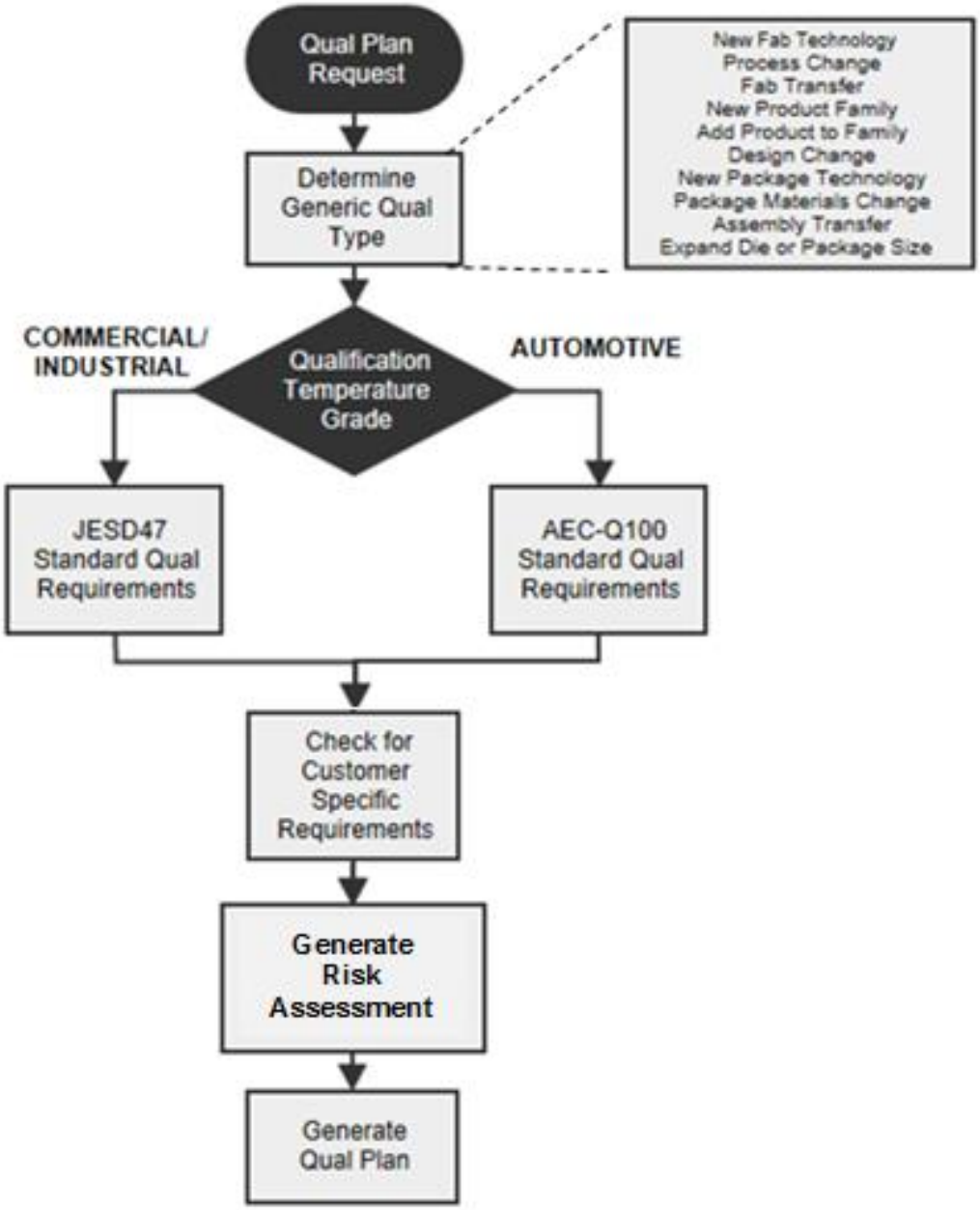
Product families are qualified based upon the requirements outlined in Table 2.0.2. In general, Lattice Semiconductor follows the current Joint Electron Device Engineering Council (JEDEC) and Military Standard testing methods. Lattice automotive products are qualified and characterized to the Automotive Electronics Council (AEC) testing requirements and methods. Product family qualification will include products with a wide range of circuit densities, package types, and package lead counts. Major changes to products, processes, or vendors require additional qualification before implementation.

The ECP5 family is the fourth generation FPGA product family. It is fabricated at United Microelectronics Corporation (UMC) and United Semiconductor Japan Corporation (USJC) using a 40nm SRAM only technology node (LP40-9M). The Lattice Semiconductor ECP5 FPGA product family qualification efforts are based on ECP5 devices in the family per the Lattice Semiconductor Qualification Procedure, Doc #100164.

Lattice Semiconductor maintains a regular reliability monitor program. The current Lattice Reliability Monitor Report can be found at Product Reliability Monitor Report.

Figure 2.0.1 Lattice Standard Product Qualification Process Flow

This diagram represents the standard qualification flow used by Lattice to qualify new Product Families. The target end market for the Product Family determines which flow options are used. The ECP5 Product Family was qualified using the Commercial / Industrial Qualification Option.



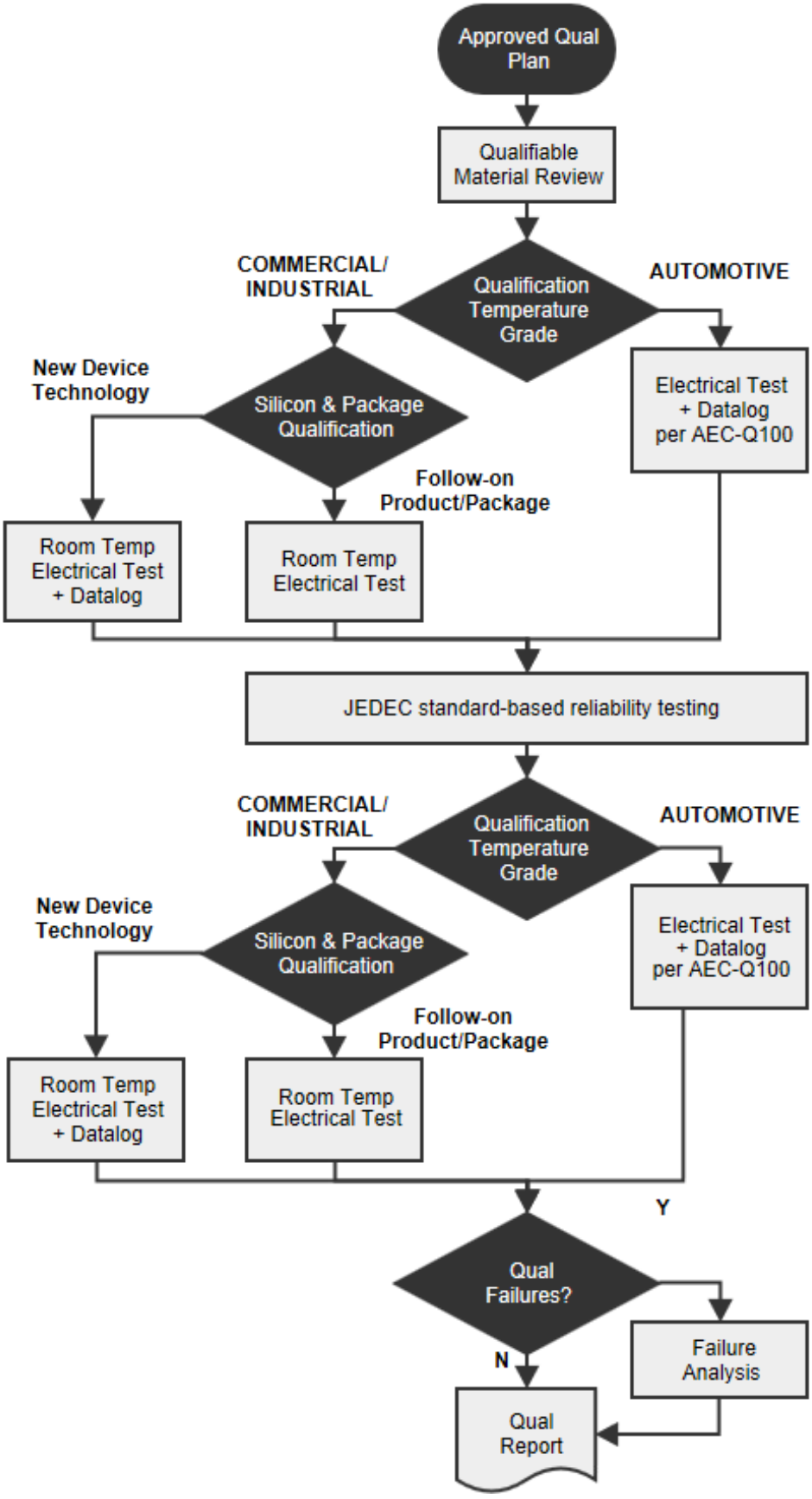

Approved Qual Plan
Qualifiable Material Review
COMMERCIAL/ INDUSTRIAL
Qualification Temperature Grade
AUTOMOTIVE
New Device Technology
Silicon & Package Qualification
Electrical Test + Datalog per AEC-Q100
Follow-on Product/Package
Room Temp Electrical Test + Datalog
Room Temp Electrical Test
JEDEC standard-based reliability testing
COMMERCIAL/ INDUSTRIAL
Qualification Temperature Grade
AUTOMOTIVE
New Device Technology
Silicon & Package Qualification
Electrical Test + Datalog per AEC-Q100
Follow-on Product/Package
Room Temp Electrical Test + Datalog
Room Temp Electrical Test
Y
Qual Failures?
N
Failure Analysis
Qual Report

Table 2.0.2 Typical Qualification Testing

TEST	STANDARD	TEST CONDITIONS
High Temperature Operating Life (HTOL)	JESD22-A108	≥125°C Tj and max operating supplies
Electrostatic Discharge - Human Body Model (HBM)	JS-001	25°C (Technology/Device dependent Performance Targets)
Electrostatic Discharge - Charged Device Model (CDM)	JESD22-C101	25°C (Technology/Device dependent Performance Targets)
Latch-Up (LU)	JESD78	Class II, +/-100mA trigger current and AMR operating supplies
Accelerated Soft Error Testing (ASER)	JESD89	25°C, Nominal operating supplies
Surface Mount Pre-conditioning (SMPC)	IPC/JEDEC J-STD-020	Per appropriate MSL level per J-STD-020
High Temp Storage Life (HTSL)	JESD22-A103	Condition B
Temperature Cycling (TC)	JESD22-A104	Condition B, soak mode 2 (typical)
Temperature Humidity Bias, THB (85/85) or	JESD22-A101	85°C, 85% RH, max operating supplies or
Biased Highly Accelerated Stress Test (HAST)	JESD22-A110	110°C, 85% RH, max operating supplies or
		130°C, 85% RH, max operating supplies
Unbiased Highly Accelerated Stress Test (uHAST)	JESD22-A118	110°C, 85% RH or 130°C, 85% RH

3.0 QUALIFICATION DATA FOR ECP5 PRODUCT FAMILY

The ECP5 family is the fourth generation FPGA product family and first nine-layer metal 40nm SRAM only Technology based product offering. The ECP5 product family is used as the primary technology qualification vehicle.

Product Family: ECP5

Packages offered: csfBGA and caBGA

Process Technology Node: 40nm

3.1 ECP5 Product Family Life Data

The High Temperature Operating Life (HTOL) test is used to thermally accelerate those wear out and failure mechanisms that would occur as a result of operating the device continuously in a system application. Consistent with JESD22-A108D "Temperature, Bias, and Operating Life", a pattern specifically designed to exercise the maximum amount of circuitry is programmed into the device and this pattern is continuously exercised at specified voltages as described in test conditions for each device type.

The Early Life Failure Rate (ELFR) test uses large samples sizes for a short duration (48hrs ≤ t ≤ 168 hrs) HTOL stress to determine the infant mortality rate of a device family.

ECP5 Life Test (HTOL) Conditions:

Stress Duration: 168, 500, 1000 hours

Stress Conditions: ECP5 (LFE5) max operating supplies, $T_{JUNCTION}$ = 125°C

Method: JESD22-A108D

Table 3.1.1 ECP5 Product Family Life Results

Product Name	Foundry	Package	Lot #	Qty	48 Hrs Result	168 Hrs Result	500 Hrs Result	1000 Hrs Result	Cumulative Hours
LFE5UM-25	UMC	381 caBGA	Lot #1	106	N/A	0	0	0	106,000
LFE5UM-45	UMC	381 caBGA	Lot #1	71	N/A	0	0	0	71,000
LFE5UM-45	UMC	381 caBGA	Lot #2	43	N/A	0	0	0	43,000
LFE5UM-45	USJC	285 csfBGA	Lot #3	77	N/A	0	0	0	77,000
LFE5UM-45	USJC	285 csfBGA	Lot #4	77	N/A	0	0	0	77,000
LFE5UM-45	USJC	285 csfBGA	Lot #5	77	N/A	0	0	0	77,000
LFE5UM-45	USJC	285 csfBGA	Lot #3	700	0	N/A	N/A	N/A	N/A
LFE5UM-45	USJC	285 csfBGA	Lot #4	700	0	N/A	N/A	N/A	N/A
LFE5UM-45	USJC	285 csfBGA	Lot #5	700	0	N/A	N/A	N/A	N/A
LFE5UM-85	UMC	381 caBGA	Lot #1a	24	N/A	0	0	0	24,000
LFE5UM-85	UMC	381 caBGA	Lot #1b	23	N/A	0	0	0	23,000
LFE5UM-85	UMC	381 caBGA	Lot #1c	24	N/A	0	0	0	24,000
LFE5UM-85	UMC	381 caBGA	Lot #2	106	N/A	0	0	0	106,000

ECP5 Cumulative Life Testing Device Hours = 628,000
ECP5 Cumulative Result / Sample Size = 0 / 628
ECP5 FIT Rate = 19 FIT; FIT Assumptions: CL=60%, AE=0.7eV, Tjref=55C

ECP5 ELFR (48 to 168 Hrs) Cumulative Result / Sample Size = 0 / 2,728
ECP5 HTOL (500 Hrs) Cumulative Result / Sample Size = 0 / 628
ECP5 HTOL (1000 Hrs) Cumulative Result / Sample Size = 0 / 628
Test Chip Cumulative Sample Size = 0 / 628

3.2 ECP5 Product Family – ESD and Latch Up Data

Electrostatic Discharge-Human Body Model

The ECP5 product family was tested per JS-001-2014 Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM) procedure.

All units were tested at room ambient prior to reliability stress and after reliability stress. No failures were observed within the passing classification.

Table 3.2.1 ECP5 ESD-HBM Data

Product Type	285 csfBGA	256caBGA	381 caBGA	554 caBGA	756 caBGA
LFE5UM-25	QBS	Package not offered	>1000V Class 1C	Package not offered	Package not offered
LFE5UM-45	>1000V Class 1C		QBS	>1000V Class 1C	
LFEUM-85	QBS		QBS	>1000V Class 1C	QBS
LFE5UM5G-25	QBS		QBS	Package not offered	Package not offered
LFE5UM5G-45	QBS		QBS	QBS	
LFEUM5G-85	QBS		QBS	QBS	QBS
LFE5U-12	QBS	QBS	QBS	Package not offered	Package not offered
LFE5U-25	QBS	QBS	QBS		
LFE5U-45	QBS	QBS	QBS	QBS	
LFE5U-85	QBS	Package not offered	QBS	QBS	QBS

HBM classification for Commercial/Industrial products, per JS-001-2014 and JS-001-2017 (285 csfBGA package only).

All HBM levels indicated are dual-polarity (±).

HBM worst-case performance is the package with the smallest RLC parasitics. All other packages for a given product are qualified-by-similarity (QBS).

Note that USJC foundry data was only collected on the LFE5UM-45/285csfBGA product/package combination. The USJC foundry change is only considered a fab site change since the process is identical to the UMC process.

Electrostatic Discharge-Charged Device Model

The ECP5 product family was tested per the JS-002-2014, Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components procedure.
All units were tested at room ambient prior to reliability stress and after reliability stress. No failures were observed within the passing classification.

Table 3.2.2 ECP5 ESD-CDM Data

Product Type	285 csfBGA	256caBGA	381 caBGA	554 caBGA	756 caBGA
LFE5UM-25	QBS	Package not offered	>500V Class C2a	Package not offered	Package not offered
LFE5UM-45	>500V Class C2a		QBS	>500V Class C2a	
LFEUM-85	QBS		QBS	QBS	>250V (SerDes pins) Class C1 >500V (all other pins) Class C2a
LFE5UM5G-25	QBS		QBS	Package not offered	Package not offered
LFE5UM5G-45	QBS		QBS	QBS	
LFEUM5G-85	QBS		QBS	QBS	QBS
LFE5U-12	QBS	QBS	QBS	Package not offered	Package not offered
LFE5U-25	QBS	QBS	QBS		
LFE5U-45	QBS	QBS	QBS	QBS	
LFE5U-85	QBS	Package not offered	QBS	QBS	>500V Class C2a

CDM classification for Commercial/Industrial products, per JS-002-2014.
All CDM levels indicated are dual-polarity (±).
CDM worst-case performance is the package with the largest bulk capacitance. All other packages for a given product are qualified-by-similarity (QBS).
Note that USJC foundry data was only collected on the LFE5UM-45/285csfBGA product/package combination. The USJC foundry change is only considered a fab site change since the process is identical to the UMC process.

Latch-Up

The ECP5 product family was tested per the JESD78D IC Latch-up Test procedure.

All units were tested at room ambient prior to reliability stress and after reliability stress. No failures were observed within the passing classification.

Table 3.2.3 ECP5 Latch-up I-Test Data

Product Type	285 csfBGA	256caBGA	381 caBGA	554 caBGA	756 caBGA
LFE5UM-25	QBS	Package not offered	>100mA @ 105°C Class II	Package not offered	Package not offered
LFE5UM-45	>100mA @ 105°C Class II		QBS	>100mA @ 105°C Class II	
LFEUM-85	QBS		QBS	>100mA @ 105°C Class II	QBS
LFE5UM5G-25	QBS		QBS	Package not offered	Package not offered
LFE5UM5G-45	QBS		QBS	QBS	
LFEUM5G-85	QBS		QBS	QBS	QBS
LFE5U-12	QBS	QBS	QBS	Package not offered	Package not offered
LFE5U-25	QBS	QBS	QBS		
LFE5U-45	QBS	QBS	QBS	QBS	
LFE5U-85	QBS	Package not offered	QBS	QBS	QBS

I-Test classification for Commercial/Industrial products, per JESD78D and JESD78E (285 csfBGA package only).
All I-Test levels indicated are dual-polarity (±).
I-Test worst-case performance is the package with access to the most IOs. All other packages for a given product are qualified-by-similarity (QBS).
Note that USJC foundry data was only collected on the LFE5UM-45/285csfBGA product/package combination. The USJC foundry change is only considered a fab site change since the process is identical to the UMC process.

Table 3.2.4 ECP5 Vsupply Over-voltage Test Data

Product Type	285 csfBGA	256caBGA	381 caBGA	554 caBGA	756 caBGA
LFE5UM-25	QBS	Package not offered	AMR operating supply @ 105°C Class II	Package not offered	Package not offered
LFE5UM-45	AMR operating supply @ 105°C Class II		QBS	AMR operating supply @ 105°C Class II	
LFEUM-85	QBS		QBS	AMR operating supply @ 105°C Class II	QBS
LFE5UM5G-25	QBS		QBS	Package not offered	Package not offered
LFE5UM5G-45	QBS		QBS	QBS	
LFEUM5G-85	QBS		QBS	QBS	QBS
LFE5U-12	QBS	QBS	QBS	Package not offered	Package not offered
LFE5U-25	QBS	QBS	QBS		
LFE5U-45	QBS	QBS	QBS	QBS	
LFE5U-85	QBS	Package not offered	QBS	QBS	QBS

Vsupply Over-voltage Test classification for Commercial/Industrial products, per JESD78D and JESD78E (285 csfBGA package only).
Vsupply Over-voltage Test worst-case performance is the package with access to the most individual power rails. All other packages for a given product are qualified-by-similarity (QBS).
Note that USJC foundry data was only collected on the LFE5UM-45/285csfBGA product/package combination. The USJC foundry change is only considered a fab site change since the process is identical to the UMC process.

3.3 ECP5 Product Family – Soft Error Rate Data

Soft Error Rate (SER) testing is conducted to characterize the sensitivity of SRAM memory elements to Atmospheric Neutron and Alpha Particle radiation. Charge induced by the impact of these particles can collect at sensitive nodes in the device and result in changes to the internal states of the device. While these changes do not cause physical damage to the device, they can cause errors in device operation.

Neutron SER – The normalized upset rate of Configuration RAM and Embedded Block RAM (EBR) memories due to neutron events. During testing, devices were configured with a memory pattern, exposed to an accelerated neutron environment, and the memory was read back from the device. Upset bits were identified through pattern comparison. Neutron testing results are normalized to the standard neutron flux for New York City at sea level: 14 n/cm^2/hr. The SER is represented in Failures in Time per million bits (FIT/Mb) to allow for translation across different device families and densities.

Alpha Particle SER – The normalized upset rate of Configuration RAM and Embedded Block RAM (EBR) memories due to alpha particle events. During testing, devices were configured with a memory pattern, exposed to a calibrated alpha source (Am-241), and the memory was read back from the device. Upset bits were identified through pattern comparison. Alpha particle testing results are normalized to a standard flux for Ultra Low Alpha (ULA) packaging materials: 0.001 alpha/cm^2/hr. The SER is represented in Failures in Time per million bits (FIT/Mb) to allow for translation across different device families and densities.

Table 3.3.1 40LP-SA (40nm) SER

Particle Type	Memory	SER (FIT/Mb)
Neutron	Configuration RAM	176.2
	EBR	262.9
Alpha Particle	Configuration RAM	152.8
	EBR	346.8

Note: Detailed SER reports are available upon request.

4.0 PACKAGE QUALIFICATION DATA FOR ECP5 PRODUCT FAMILY

The ECP5 product family is offered in csfBGA and caBGA packages. This report details the package qualification results of the initial ECP5 product introductions. Package qualification tests include Temperature Cycling (TC), Unbiased HAST (UHAST), Biased HAST (HAST) and High Temperature Storage (HTSL). Mechanical evaluation tests include Scanning Acoustic Tomography (SAT) and visual package inspection.

The generation and use of generic data is applied across a family of products or packages emanating from one base wafer foundry or assembly process is a Family Qualification, or Qualification-by-Similarity. For the package stresses HAST, UHAST and HTSL, these are considered generic for a given Package Technology. Surface Mount Pre-Conditioning (SMPC) is considered generic up to an evaluated Peak Reflow temperature, for a given Package Technology. The following table demonstrates the package qualification matrix.

Table 4.0.1 Product-Package Qualification-By-Similarity Matrix

Products	Stress Test	Advanced Semiconductor Engineering, Taiwan (ASEK)	Amkor Technology Korea (ATK)	Advanced Semiconductor Engineering, Malaysia (ASEM)			
		285 csfBGA		256 caBGA	381 caBGA	554 caBGA	756 caBGA
LFE5UM-25	SMPC	MSL3 260°C	Package not offered	Package not offered	MSL3 260°C	Package not offered	Package not offered
	TC	700 cycles			700 cycles		
	HAST/	264 hours			QBS		
	THB	1000 hours					
	UHAST	264 hours					
	HTSL	1000 hours					
LFE5UM-45	SMPC	MSL3 260°C	Package not offered		MSL3 260°C	MSL3 260°C	
	TC	700 cycles			700 cycles	700 cycles	
	HAST/	264 hours/			264 hours	QBS	
	THB	1000 hours					
	UHAST	264 hours			264 hours	QBS	
	HTSL	1000 hours			1000 hours	QBS	
LFE5UM-85	SMPC	MSL3 260°C	MSL3 260°C		MSL3 260°C	QBS	MSL3 260°C
	TC	700 cycles	700 cycles		700 cycles		700 cycles
	HAST/		264 hours		QBS		264 hours
	THB	1000 hours					
	UHAST	264 hours	264 hours		QBS	QBS	264 hours
	HTSL	1000 hours	1000 hours				1000 hours
LFE5UM 5G-25	SMPC	QBS	Package not offered		QBS	Package not offered	Package not offered
	TC						
	HAST						
	UHAST						
	HTSL						
LFE5UM 5G-45	SMPC	QBS	Package not offered		QBS	QBS	
	TC						
	HAST						
	UHAST						
	HTSL						
LFE5UM 5G-85	SMPC	QBS	QBS		QBS	QBS	QBS
	TC						
	HAST						
	UHAST						
	HTSL						
LFE5U-12	SMPC	QBS	Package not offered	QBS	QBS	Package not offered	Package not offered
	TC						
	HAST						
	UHAST						

Products	Stress Test	Advanced Semiconductor Engineering, Taiwan (ASEK)	Amkor Technology Korea (ATK)	Advanced Semiconductor Engineering, Malaysia (ASEM)			
		285 csfBGA		256 caBGA	381 caBGA	554 caBGA	756 caBGA
	HTSL						
LFE5U-25	SMPC	QBS	Package not offered	MSL3 260°C	QBS		
	TC			700 cycles			
	HAST/ THB			264 hours/ 1000 hours			
	UHAST			264 hours			
	HTSL			1000 hours			
LFE5U-45	SMPC	QBS	Package not offered	MSL3 260°C	QBS	QBS	
	TC			700 cycles			
	HAST			264 hours			
	UHAST			264 hours			
	HTSL			1000 hours			
LFE5U-85	SMPC	QBS	QBS	Package not offered	QBS	QBS	QBS
	TC						
	HAST						
	UHAST						
	HTSL						

4.1 Surface Mount Preconditioning Testing

The Surface Mount Preconditioning (SMPC) Test is used to model the surface mount assembly conditions during component solder processing. All devices stressed through Temperature Cycling, Unbiased HAST and Biased HAST were preconditioned. This preconditioning is consistent with JESD22-A113F "Preconditioning Procedures of Plastic Surface Mount Devices Prior to Reliability Testing", Moisture Sensitivity Level 3 (MSL3) package moisture sensitivity and dry-pack storage requirements.

Surface Mount Preconditioning (MSL3)

(5 Temperature Cycles Condition B, 24 hours bake @ 125°C, 30°C/60% RH, soak 192 hours, 260 °C Reflow Simulation, 3 passes) performed before all package tests.

MSL3 Packages: csfBGA, caBGA

Method: J-STD-020D/E and JESD22-A113F/G

Table 4.1.1 Surface Mount Precondition Data

Product Name	Foundry	Package	Assembly Site	Lot Number	Moisture Soak Level	3X Reflow Temperature	Qty	# of Fails
LFE5U-25	UMC	256 caBGA	ASEM	Lot #1	MSL3	260°C	400	0
LFE5U-25	UMC	256 caBGA	ASEM	Lot #2	MSL3	260°C	400	0
LFE5U-25	UMC	256 caBGA	ASEM	Lot #3	MSL3	260°C	400	0
LFE5U-25	UMC	256 caBGA	ASEM	Lot #1	MSL3	260°C	178	0[B]
LFE5U-25	UMC	256 caBGA	ASEM	Lot #2	MSL3	260°C	179	0[B]
LFE5U-25	USJC	256 caBGA	ASEM	Lot #4	MSL3	260°C	384	2[A]
LFE5U-45	UMC	256 caBGA	ASEM	Lot #1	MSL3	260°C	400	0
LFE5U-45	UMC	256 caBGA	ASEM	Lot #2	MSL3	260°C	400	0
LFE5U-45	UMC	256 caBGA	ASEM	Lot #3	MSL3	260°C	400	0
LFE5UM-25	UMC	381 caBGA	ASEM	Lot #1	MSL3	260°C	360	0
LFE5UM-45	UMC	381 caBGA	ASEM	Lot #1	MSL3	260°C	329	2[A]
LFE5UM-45	UMC	381 caBGA	ASEM	Lot #2	MSL3	260°C	329	0
LFE5UM-45	UMC	381 caBGA	ASEM	Lot #3	MSL3	260°C	329	2[A]
LFE5UM-45	UMC	381 caBGA	ASEM	Lot #4	MSL3	260°C	330	0
LFE5UM-45	UMC	381 caBGA	ASEM	Lot #5	MSL3	260°C	330	0
LFE5UM-45	UMC	381 caBGA	ASEM	Lot #6	MSL3	260°C	330	0
LFE5UM-45	USJC	381 caBGA	ASEM	Lot #1	MSL3	260°C	308	0
LFE5UM-85	UMC	381 caBGA	ASEM	Lot #1	MSL3	260°C	30	0
LFE5UM-85	UMC	381 caBGA	ASEM	Lot #2	MSL3	260°C	30	0
LFE5UM-85	UMC	381 caBGA	ASEM	Lot #3	MSL3	260°C	30	0
LFE5UM-85	UMC	381 caBGA	ASEM	Lot #4	MSL3	260°C	350	3[A]
LFE5UM-45	UMC	554 caBGA	ASEM	Lot #1	MSL3	260°C	84	0
LFE5UM-45	UMC	554 caBGA	ASEM	Lot #2	MSL3	260°C	85	0
LFE5UM-45	UMC	554 caBGA	ASEM	Lot #3	MSL3	260°C	85	1[A]
LFE5UM-45	UMC	554 caBGA	ASEM	Lot #4	MSL3	260°C	350	0
LFE5UM-45	USJC	554 caBGA	ASEM	Lot #1	MSL3	260°C	231	0
LFE5UM-85	UMC	756 caBGA	ASEM	Lot #1	MSL3	260°C	117	0
LFE5UM-85	UMC	756 caBGA	ASEM	Lot #2	MSL3	260°C	110	0
LFE5UM-85	UMC	756 caBGA	ASEM	Lot #3	MSL3	260°C	110	0

Product Name	Foundry	Package	Assembly Site	Lot Number	Moisture Soak Level	3X Reflow Temperature	Qty	# of Fails
LFE5UM-25	UMC	285 csfBGA	ASEK	Lot #1	MSL3	260°C	320	0
LFE5UM-25	UMC	285 csfBGA	ASEK	Lot #2	MSL3	260°C	320	0
LFE5UM-25	UMC	285 csfBGA	ASEK	Lot #3	MSL3	260°C	320	0
LFE5UM-25	USJC	285 csfBGA	ASEK	Lot #4	MSL3	260°C	84	0
LFE5UM-45	UMC	285 csfBGA	ASEK	Lot #1	MSL3	260°C	330	0
LFE5UM-45	UMC	285 csfBGA	ASEK	Lot #2	MSL3	260°C	330	0
LFE5UM-45	UMC	285 csfBGA	ASEK	Lot #3	MSL3	260°C	330	0
LFE5UM-45	USJC	285 csfBGA	ASEK	Lot #1	MSL3	260°C	385	0
LFE5UM-85	UMC	285 csfBGA	ATK	Lot #1	MSL3	260°C	400	0
LFE5UM-85	UMC	285 csfBGA	ATK	Lot #2	MSL3	260°C	400	0
LFE5UM-85	UMC	285 csfBGA	ATK	Lot #3	MSL3	260°C	400	0
LFE5U-85	UMC	285 csfBGA	ASEK	Lot #1	MSL3	260°C	216	0
LFE5U-85	UMC	285 csfBGA	ASEK	Lot #2	MSL3	260°C	215	0
LFE5U-85	UMC	285 csfBGA	ASEK	Lot #3	MSL3	260°C	216	0

A = Open contact fails due to lifted ball bonds. Chlorine contamination found on affected pad. CA/PA in place.
B = AuPCC+ wirebond conversion

Note: ASEM has on-going continuous improvements to eliminate the lifted ball bond issues observed to date. These improvements include contamination reduction, wire bond process optimization, high reliability Pd-coated copper wire adoption (ongoing conversion from late 2019 to mid-2020).

Cumulative SMPC Failure Rate ECP5 = 10 / 11,664

4.2 Temperature Cycling Data

The Temperature Cycling test is used to accelerate those failures resulting from mechanical stresses induced by differential thermal expansion of adjacent films, layers and metallurgical interfaces in the die and package. Devices are tested at 25°C after exposure to repeated cycling between -55°C and +125°C in an air environment consistent with JESD22-A104D "Temperature Cycling", Condition B temperature cycling requirements. Prior to Temperature Cycling testing, all devices are subjected to Surface Mount Preconditioning.

MSL3 Packages: csfBGA, caBGA

Stress Duration: 700 cycles

Stress Conditions: Temperature cycling between -55°C to 125°C

Method: JESD22-A104D/E Condition B

Table 4.2.1 Temperature Cycling Data

Product Name	Foundry	Package	Assembly Site	Lot Number	Stress Temperature	Stress Duration	Qty	# of Fails
LFE5U-25	UMC	256 caBGA	ASEM	Lot #1	-55°C to 125°C	700 cycles	79	0
LFE5U-25	UMC	256 caBGA	ASEM	Lot #2	-55°C to 125°C	700 cycles	80	0
LFE5U-25	UMC	256 caBGA	ASEM	Lot #3	-55°C to 125°C	700 cycles	80	0
LFE5U-25	UMC	256 caBGA	ASEM	Lot #1	-55°C to 125°C	700 cycles	25	0[B]
LFE5U-25	UMC	256 caBGA	ASEM	Lot #2	-55°C to 125°C	700 cycles	25	0[B]
LFE5U-25	USJC	256 caBGA	ASEM	Lot #4	-55°C to 125°C	700 cycles	94	0
LFE5U-45	UMC	256 caBGA	ASEM	Lot #1	-55°C to 125°C	700 cycles	80	0
LFE5U-45	UMC	256 caBGA	ASEM	Lot #2	-55°C to 125°C	700 cycles	80	0
LFE5U-45	UMC	256 caBGA	ASEM	Lot #3	-55°C to 125°C	700 cycles	80	0
LFE5UM-25	UMC	381 caBGA	ASEM	Lot #1	-55°C to 125°C	700 cycles	350	1[A]
LFE5UM-45	UMC	381 caBGA	ASEM	Lot #1	-55°C to 125°C	700 cycles	80	0
LFE5UM-45	UMC	381 caBGA	ASEM	Lot #2	-55°C to 125°C	700 cycles	79	0
LFE5UM-45	UMC	381 caBGA	ASEM	Lot #3	-55°C to 125°C	700 cycles	80	0
LFE5UM-45	USJC	381 caBGA	ASEM	Lot #4	-55°C to 125°C	700 cycles	77	0
LFE5UM-85	UMC	381 caBGA	ASEM	Lot #1	-55°C to 125°C	700 cycles	30	0
LFE5UM-85	UMC	381 caBGA	ASEM	Lot #2	-55°C to 125°C	700 cycles	30	0
LFE5UM-85	UMC	381 caBGA	ASEM	Lot #3	-55°C to 125°C	700 cycles	30	0
LFE5UM-85	UMC	381 caBGA	ASEM	Lot #3	-55°C to 125°C	700 cycles	347	1[A]
LFE5UM-45	UMC	554 caBGA	ASEM	Lot #1	-55°C to 125°C	700 cycles	80	0
LFE5UM-45	UMC	554 caBGA	ASEM	Lot #2	-55°C to 125°C	700 cycles	80	0
LFE5UM-45	UMC	554 caBGA	ASEM	Lot #3	-55°C to 125°C	700 cycles	80	0
LFE5UM-45	USJC	554 caBGA	ASEM	Lot #4	-55°C to 125°C	700 cycles	77	0
LFE5UM-85	UMC	756 caBGA	ASEM	Lot #1	-55°C to 125°C	700 cycles	30	0
LFE5UM-85	UMC	756 caBGA	ASEM	Lot #2	-55°C to 125°C	700 cycles	30	0
LFE5UM-85	UMC	756 caBGA	ASEM	Lot #3	-55°C to 125°C	700 cycles	30	0
LFE5UM-25	UMC	285 csfBGA	ASEK	Lot #1	-55°C to 125°C	700 cycles	80	0
LFE5UM-25	UMC	285 csfBGA	ASEK	Lot #2	-55°C to 125°C	700 cycles	80	0
LFE5UM-25	UMC	285 csfBGA	ASEK	Lot #3	-55°C to 125°C	700 cycles	80	0
LFE5UM-45	UMC	285 csfBGA	ASEK	Lot #1	-55°C to 125°C	700 cycles	90	0
LFE5UM-45	UMC	285 csfBGA	ASEK	Lot #2	-55°C to 125°C	700 cycles	90	0
LFE5UM-45	UMC	285 csfBGA	ASEK	Lot #3	-55°C to 125°C	700 cycles	90	0

Product Name	Foundry	Package	Assembly Site	Lot Number	Stress Temperature	Stress Duration	Qty	# of Fails
LFE5UM-45	USJC	285 csfBGA	ASEK	Lot #1	-55°C to 125°C	700 cycles	77	0
LFE5UM-85	UMC	285 csfBGA	ATK	Lot #1	-55°C to 125°C	700 cycles	80	0
LFE5UM-85	UMC	285 csfBGA	ATK	Lot #2	-55°C to 125°C	700 cycles	80	0
LFE5UM-85	UMC	285 csfBGA	ATK	Lot #3	-55°C to 125°C	700 cycles	80	0
LFE5U-85	UMC	285 csfBGA	ASEK	Lot #1	-55°C to 125°C	700 cycles	77	0
LFE5U-85	UMC	285 csfBGA	ASEK	Lot #2	-55°C to 125°C	700 cycles	77	0
LFE5U-85	UMC	285 csfBGA	ASEK	Lot #3	-55°C to 125°C	700 cycles	77	0

A = Open contact fails due to lifted ball bonds. Chlorine contamination found on affected pad. CA/PA in place.
B = AuPCC+ wirebond conversion

Note: ASEM has on-going continuous improvements to eliminate the lifted ball bond issues observed to date. These improvements include contamination reduction, wire bond process optimization, high reliability Pd-coated copper wire adoption (ongoing conversion from late 2019 to mid-2020).

Cumulative Temp Cycle Failure Rate ECP5 = 2 / 3,191

4.3 Unbiased HAST Data

Unbiased Highly Accelerated Stress Test (UHAST) testing uses both pressure and temperature to accelerate penetration of moisture into the package and to the die surface. The Unbiased HAST test is designed to detect ionic contaminants present within the package or on the die surface, which can cause chemical corrosion. Consistent with JESD22-A118A, "Accelerated Moisture Resistance - Unbiased HAST," the Unbiased HAST condition is 264 hours exposure at 110°C and 85% relative humidity. Prior to Unbiased HAST testing, all devices are subjected to Surface Mount Preconditioning.

MSL3 Packages: csfBGA, caBGA

Stress Duration: 264 Hours

Stress Conditions: 110°C/85% RH

Method: JESD22-A118A/B

Table 4.3.1 Unbiased HAST Data

Product Name	Foundry	Package	Assembly Site	Lot Number	Stress Temperature	Stress Duration	Qty	# of Fails
LFE5U-25	UMC	256 caBGA	ASEM	Lot #1	110°C	264 hours	80	0
LFE5U-25	UMC	256 caBGA	ASEM	Lot #2	110°C	264 hours	80	0
LFE5U-25	UMC	256 caBGA	ASEM	Lot #3	110°C	264 hours	80	0
LFE5U-25	USJC	256 caBGA	ASEM	Lot #4	110°C	264 hours	99	0
LFE5U-45	UMC	256 caBGA	ASEM	Lot #1	110°C	264 hours	79	0
LFE5U-45	UMC	256 caBGA	ASEM	Lot #2	110°C	264 hours	80	0
LFE5U-45	UMC	256 caBGA	ASEM	Lot #3	110°C	264 hours	80	0
LFE5UM-45	UMC	381 caBGA	ASEM	Lot #1	110°C	264 hours	80	0
LFE5UM-45	UMC	381 caBGA	ASEM	Lot #2	110°C	264 hours	80	0
LFE5UM-45	UMC	381 caBGA	ASEM	Lot #3	110°C	264 hours	80	0
LFE5UM-45	USJC	381 caBGA	ASEM	Lot #4	110°C	264 hours	77	0
LFE5UM-45	USJC	554 caBGA	ASEM	Lot #1	110°C	264 hours	77	0
LFE5UM-85	UMC	756 caBGA	ASEM	Lot #1	110°C	264 hours	30	0
LFE5UM-85	UMC	756 caBGA	ASEM	Lot #2	110°C	264 hours	25	0
LFE5UM-85	UMC	756 caBGA	ASEM	Lot #3	110°C	264 hours	25	0
LFE5UM-25	UMC	285 csfBGA	ASEK	Lot #1	110°C	264 hours	80	0
LFE5UM-25	UMC	285 csfBGA	ASEK	Lot #2	110°C	264 hours	80	0
LFE5UM-25	UMC	285 csfBGA	ASEK	Lot #3	110°C	264 hours	80	0
LFE5UM-45	UMC	285 csfBGA	ASEK	Lot #1	110°C	264 hours	80	0
LFE5UM-45	UMC	285 csfBGA	ASEK	Lot #2	110°C	264 hours	80	0
LFE5UM-45	UMC	285 csfBGA	ASEK	Lot #3	110°C	264 hours	80	0
LFE5UM-45	USJC	285 csfBGA	ASEK	Lot #1	110°C	264 hours	77	0
LFE5UM-85	UMC	285 csfBGA	ATK	Lot #1	110°C	264 hours	80	0
LFE5UM-85	UMC	285 csfBGA	ATK	Lot #2	110°C	264 hours	80	0
LFE5UM-85	UMC	285 csfBGA	ATK	Lot #3	110°C	264 hours	80	0
LFE5U-85	UMC	285 csfBGA	ASEK	Lot #1	110°C	264 hours	77	0
LFE5U-85	UMC	285 csfBGA	ASEK	Lot #2	110°C	264 hours	77	0
LFE5U-85	UMC	285 csfBGA	ASEK	Lot #3	110°C	264 hours	77	0

Cumulative Unbiased HAST failure Rate ECP5 = 0 / 2,080

4.4 Biased Highly Accelerated Temperature and Humidity Stress Test (BHAST) or Steady-State Temperature Humidity Bias Life Test (THB)

Highly Accelerated Stress Test (HAST) testing uses both pressure and temperature to accelerate penetration of moisture into the package and to the die surface. The BHAST test is used to accelerate threshold shifts in the MOS device associated with moisture diffusion into the gate oxide region as well as electrochemical corrosion mechanisms within the device package. Consistent with JEDEC JESD22-A110 “Highly-Accelerated Temperature and Humidity Stress Test”, the biased HAST conditions are either 96 hours exposure at 130°C and 85% relative humidity, or 264 hours exposure at 110°C and 85% relative humidity.

Steady-State Temperature Humidity Bias Life Test (THB) uses temperature, humidity and bias, minus the pressure, to accelerate the penetration of moisture through the external protective material or along the interface between the external protective material and the metallic conductors that pass through. The stress usually activates the same failure mechanism as BHAST but with a lower acceleration factor, hence, units are subjected to a longer stress time of 1000 hours at 85°C and 85% relative humidity, consistent with JEDEC JESD22-A101 “Steady-State Temperature Humidity Bias Life Test”.

MSL3 Packages: csfBGA, caBGA

Stress Conditions: Maximum Operating Supplies and 110°C and 85% RH (BHAST) or 85°C and 85% RH (THB)

Stress Duration: 264 hours or 1000 hours

Method: JESD22-A110D/E or JESD22-A101D

Table 4.4.1 BHAST/THB Data

Product Name	Foundry	Package	Assembly Site	Lot Number	Stress Temperature	Stress Duration	Qty	# of Fails
LFE5U-25	UMC	256 caBGA	ASEM	Lot #1	110°C	264 hours	78	0
LFE5U-25	UMC	256 caBGA	ASEM	Lot #2	110°C	264 hours	78	0
LFE5U-25	UMC	256 caBGA	ASEM	Lot #3	110°C	264 hours	78	1[A]
LFE5U-25	UMC	256 caBGA	ASEM	Lot #1	110°C	264 hours	77	0[B]
LFE5U-25	UMC	256 caBGA	ASEM	Lot #2	110°C	264 hours	77	0[B]
LFE5U-25	USJC	256 caBGA	ASEM	Lot #4	85°C	1000 hours	81	0
LFE5U-45	UMC	256 caBGA	ASEM	Lot #1	110°C	264 hours	80	0
LFE5U-45	UMC	256 caBGA	ASEM	Lot #2	110°C	264 hours	80	0
LFE5U-45	UMC	256 caBGA	ASEM	Lot #3	110°C	264 hours	80	0
LFE5UM-45	UMC	381 caBGA	ASEM	Lot #1	110°C	264 hours	84	0
LFE5UM-45	UMC	381 caBGA	ASEM	Lot #2	110°C	264 hours	84	0
LFE5UM-45	UMC	381 caBGA	ASEM	Lot #3	110°C	264 hours	84	0
LFE5UM-45	USJC	381 caBGA	ASEM	Lot #1	110°C	264 hours	77	0
LFE5UM-85	UMC	756 caBGA	ASEM	Lot #1	110°C	264 hours	27	0
LFE5UM-85	UMC	756 caBGA	ASEM	Lot #2	110°C	264 hours	25	0
LFE5UM-85	UMC	756 caBGA	ASEM	Lot #3	110°C	264 hours	24	0
LFE5UM-25	UMC	285 csfBGA	ASEK	Lot #1	110°C	264 hours	77	0
LFE5UM-25	UMC	285 csfBGA	ASEK	Lot #2	110°C	264 hours	77	0
LFE5UM-25	UMC	285 csfBGA	ASEK	Lot #3	110°C	264 hours	77	0

Product Name	Foundry	Package	Assembly Site	Lot Number	Stress Temperature	Stress Duration	Qty	# of Fails
LFE5UM-25	USJC	285 csfBGA	ASEK	Lot #1	85°C	1000 hours	84	0
LFE5UM-45	UMC	285 csfBGA	ASEK	Lot #1	110°C	264 hours	77	0
LFE5UM-45	UMC	285 csfBGA	ASEK	Lot #2	110°C	264 hours	77	0
LFE5UM-45	UMC	285 csfBGA	ASEK	Lot #3	110°C	264 hours	77	0
LFE5UM-45	UMC	285 csfBGA	ASEK	Lot #4	110°C	264 hours	77	0
LFE5UM-45	USJC	285 csfBGA	ASEK	Lot #1	85°C	1000 hours	77	0
LFE5UM-85	UMC	285 csfBGA	ATK	Lot #1	110°C	264 hours	77	0
LFE5UM-85	UMC	285 csfBGA	ATK	Lot #2	110°C	264 hours	77	0
LFE5UM-85	UMC	285 csfBGA	ATK	Lot #3	110°C	264 hours	77	0
LFE5U-85	UMC	285 csfBGA	ASEK	Lot #1	85°C	1000 hours	25	0
LFE5U-85	UMC	285 csfBGA	ASEK	Lot #2	85°C	1000 hours	25	0
LFE5U-85	UMC	285 csfBGA	ASEK	Lot #3	85°C	1000 hours	25	0

A = LI1810037: Open contact fails due to lifted ball bonds. High level of oxygen indicating presence of foreign material between ball bond and aluminum pad. CA/PA in place.
B = AuPCC+ wirebond conversion

Note: ASEM has on-going continuous improvements to eliminate the lifted ball bond issues observed to date. These improvements include contamination reduction, wire bond process optimization, high reliability Pd-coated copper wire adoption (ongoing conversion from late 2019 to mid-2020).

Cumulative HAST failure Rate ECP5 = 1 / 2,120

4.5 High Temperature Storage Life (HTSL)

The High Temperature Storage Life test is used to determine the effect of time and temperature, under storage conditions, for thermally activated failure mechanisms. Consistent with JESD22-A103D, the devices are subjected to high temperature storage Condition B: +150 (-0/+10) °C for 1000 hours. Prior to High Temperature Storage, all ECP5 devices are subjected to Surface Mount Preconditioning as mentioned in Table 4.1.1. This is a relatively new requirement consistent with JESD47F for Pb-free, wirebonded packages.

MSL3 Packages: csfBGA, caBGA
Stress Duration: 168, 500, 1000 hours
Temperature: 150°C (ambient)
Method: JESD22-A103D/E

Table 4.5.1 ECP5 High Temperature Storage Life Results

Product Name	Foundry	Package	Assembly Site	Lot Number	Stress Temperature	Stress Duration	Qty	# of Fails
LFE5U-25	UMC	256 caBGA	ASEM	Lot #1	150°C	1000 hours	80	0
LFE5U-25	UMC	256 caBGA	ASEM	Lot #2	150°C	1000 hours	80	0
LFE5U-25	UMC	256 caBGA	ASEM	Lot #3	150°C	1000 hours	80	1[B]
LFE5U-25	UMC	256 caBGA	ASEM	Lot #1	150°C	1000 hours	77	0[C]
LFE5U-25	UMC	256 caBGA	ASEM	Lot #2	150°C	1000 hours	77	0[C]
LFE5U-25	USJC	256 caBGA	ASEM	Lot #4	150°C	1000 hours	99	0
LFE5U-45	UMC	256 caBGA	ASEM	Lot #1	150°C	1000 hours	80	0
LFE5U-45	UMC	256 caBGA	ASEM	Lot #2	150°C	1000 hours	80	0
LFE5U-45	UMC	256 caBGA	ASEM	Lot #3	150°C	1000 hours	80	0
LFE5UM-45	UMC	381 caBGA	ASEM	Lot #1	150°C	1000 hours	80	0
LFE5UM-45	UMC	381 caBGA	ASEM	Lot #2	150°C	1000 hours	80	0
LFE5UM-45	UMC	381 caBGA	ASEM	Lot #3	150°C	1000 hours	80	1[A]
LFE5UM-45	USJC	381 caBGA	ASEM	Lot #1	150°C	1000 hours	77	0
LFE5UM-45	USJC	554 caBGA	ASEM	Lot #1	150°C	1000 hours	77	0
LFE5UM-85	UMC	756 caBGA	ASEM	Lot #1	150°C	1000 hours	30	0
LFE5UM-85	UMC	756 caBGA	ASEM	Lot #2	150°C	1000 hours	30	0
LFE5UM-85	UMC	756 caBGA	ASEM	Lot #3	150°C	1000 hours	30	1[A]
LFE5UM-25	UMC	285 csfBGA	ASEK	Lot #1	150°C	1000 hours	80	0
LFE5UM-25	UMC	285 csfBGA	ASEK	Lot #2	150°C	1000 hours	80	0
LFE5UM-25	UMC	285 csfBGA	ASEK	Lot #3	150°C	1000 hours	80	0
LFE5UM-45	UMC	285 csfBGA	ASEK	Lot #1	150°C	1000 hours	80	0
LFE5UM-45	UMC	285 csfBGA	ASEK	Lot #2	150°C	1000 hours	80	0
LFE5UM-45	UMC	285 csfBGA	ASEK	Lot #3	150°C	1000 hours	80	0
LFE5UM-45	USJC	285 csfBGA	ASEK	Lot #1	150°C	1000 hours	77	0
LFE5UM-85	UMC	285 csfBGA	ATK	Lot #1	150°C	1000 hours	80	0
LFE5UM-85	UMC	285 csfBGA	ATK	Lot #2	150°C	1000 hours	80	0
LFE5UM-85	UMC	285 csfBGA	ATK	Lot #3	150°C	1000 hours	80	0
LFE5U-85	UMC	285 csfBGA	ASEK	Lot #1	150°C	1000 hours	77	0
LFE5U-85	UMC	285 csfBGA	ASEK	Lot #2	150°C	1000 hours	77	0

Product Name	Foundry	Package	Assembly Site	Lot Number	Stress Temperature	Stress Duration	Qty	# of Fails
LFE5U-85	UMC	285 csfBGA	ASEK	Lot #3	150°C	1000 hours	77	0

A = Open contact fails due to lifted ball bonds. Chlorine contamination found on affected pad. CA/PA in place.
B = LI1803015: Open contact fails due to lifted ball bonds. High level of oxygen indicating presence of foreign material between ball bond and aluminum pad. CA/PA in place.
C = AuPCC+ wirebond conversion

Note: ASEM has on-going continuous improvements to eliminate the lifted ball bond issues observed to date. These improvements include contamination reduction, wire bond process optimization, high reliability Pd-coated copper wire adoption (ongoing conversion from late 2019 to mid-2020).

ECP5 Cumulative HTSL Failure Rate = 3 / 2,245

5.0 ADDITIONAL PACKAGE FAMILY DATA

Table 5.0.1 ECP5 Package Assembly Data: Saw-singulated BGA

Package Attributes / Assembly Sites		**ASEM**					
Fabrication Process Technology		UMC 40nm CMOS (LP40-9M)					
		USJC 40nm CMOS (LP40-9M)					
Package Assembly Site		**Malaysia**					
Package Type		**caBGA**					
Material Description		**LBGA/MBGA**					
Ball Counts		256		381		554	756
Device		LFE5U-12F LFE5U-45F	LFE5U-25F	LFE5U-12F LFE5U-25F LFE5UM-25F LFE5UM-45F	LFE5U-45F LFE5U-85F LFE5UM-85F LFE5UM5G-25F LFE5UM5G-45F LFE5UM5G-85F	LFE5U-45F LFE5U-85F LFE5UM-45F LFE5UM-85F LFE5UM5G-45F LFE5UM5G-85F	LFE5U-85F LFE5UM-85F LFE5UM5G-85F
Package Body (mm)		14x14		17x17		23x23	27x27
Wafer	Thickness (mil)	8.0 +/- 0.5					
Die Attach	Epoxy Vendor	Henkel					
	Epoxy Type	Ablebond 2100A					
	Epoxy Specific Formation	Silver					
Wire Bond	Wire Vendor	Nippon Micrometal					
	Wire Diameter (mil)	0.8					
	Wire Type	Pd-coated Cu Wire	Pd/Au-coated Cu Wire		Pd-coated Cu Wire		
	Wire Impurity	0.8-2.7%	0.6-2.97%		0.8-2.7%		
Mold	Compound Vendor	Sumitomo					
	Compound Type	EMEG750SE					
	Mold Thickness (mm)	0.8					
	Compound Specific Formation	RoHS & Ultra Low Alpha					
Top Marking (option)		Laser Mark					
Solder Ball Mount	Solder Ball Vendor	Senju					
	Solder Ball Size (mm)	0.45		0.4			
	Solder Ball Composition	SAC305					
Flux	Flux Vendor	Cooksoon Electronics					
	Flux Type	Alphametals WS9180-M7					
	Flux Part Number	2160000096					

Table 5.0.2 ECP5 Package Assembly Data: Flip Chip Cu Pillar BGA

Package Attributes / Assembly Sites		**ASEK**	**ATK**
Fabrication Process Technology		UMC 40nm CMOS (LP40-9M)	
		USJC 40nm CMOS (LP40-9M)	
Package Assembly Site		**Taiwan**	**Korea**
Package Type		**csfBGA**	
Material Description		**FCCSP**	
Ball Counts		285	
Device		LFE5U-12F LFE5U-25F LFE5U-45F LFE5U-85F LFE5UM-25F LFE5UM-45F LFE5UM-85F LFE5UM5G-25F LFE5UM5G-45F LFE5UM5G-85	LFE5U-85F LFE5UM-85F LFE5UM5G-85F
Package Body (mm)		10x10	
Wafer	Thickness (mil)	14	
	Diameter (mm)	300mm	
Bump/Cu Pillar	Process	**Bump on Pad (BoP)**	**Bump on RDL (BoRDL)**
	Pitch (um)	63	90
	Total Height (um)	60	
	Composition	Cu Pillar: 100% Solder Cap - SN1.8Ag	
Mold Compound	Composition	EME-G760 Type SW	G311SQ-B
Substrate	Technology	1-2-1 HDI	
	Finish	OSP	
Solder Ball	Composition	SAC125Ni	
	Diameter (mm)	0.3	
	Pitch (mm)	0.5	

6.0 REVISION HISTORY

Table 6.0.1 ECP5 Product Family Qualification Summary Revisions

Date	Revision	Change Summary
April 2015	A	New release using LFE5UM-45 and LFE5UM-85 qualification data.
July 2015	B	Update LFE5UM-45 and LFE5UM-85 Q2 data.
September 2015	C	Update LFE5UM-45 and LFE5UM-85 Q2 data; add 25H and 85H data.
August 2016	D	Correct typo in Table 3.1.1 to reflect correct process name.
November 2017	E	Update LFE5UM5G QBS data and 285csfBGA package qualification data.
June 2018	F	Update 85H 285csfBGA package qualification data.
October 2018	G	Update 25H/45H 256caBGA package qualification data.
December 2019	H	Add United Semiconductor Japan Corporation qualification data.
December 2019	I	Added note on continuous improvement activities at ASEM to resolve lifted ball bond failures.
May 2020	J	Qualification of alternate assembly site (ASEK)
September 2020	K	Added section: ECP5 Product Family – Soft Error Rate Data

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