



REVOLUTIONARY HARDWARE MANAGEMENT SOLUTIONS

A Lattice Semiconductor White Paper

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Revolutionary Hardware Management Solutions

Circuit Board Design Overview

A circuit board is typically divided into 2 functional blocks (Figure 1), the Payload Management section and the Hardware Management section. Eighty to ninety percent of the circuit board is typically allocated to payload management functionality, such as data/control planes and/or processors. The other ten to twenty percent of the circuit board is allocated to hardware management, including functions such as power management, temperature management and control/housekeeping.



Figure 1: Typical Circuit Board Functional Blocks

Although the hardware management section takes up only 10 to 20% of the board, the designing and debugging of the section can consume a disproportionately large percentage of the overall development time (30 to 40%). Lattice LPTM21 Platform Manager 2 and L-ASC10 (ASC = Analog Sense & Control) ICs simplify the development of the hardware management portion by cutting this time in half, while increasing the overall reliability of the board and reducing the Bill of Materials (BOM) and costs.

Hardware Management Implementation & Challenges

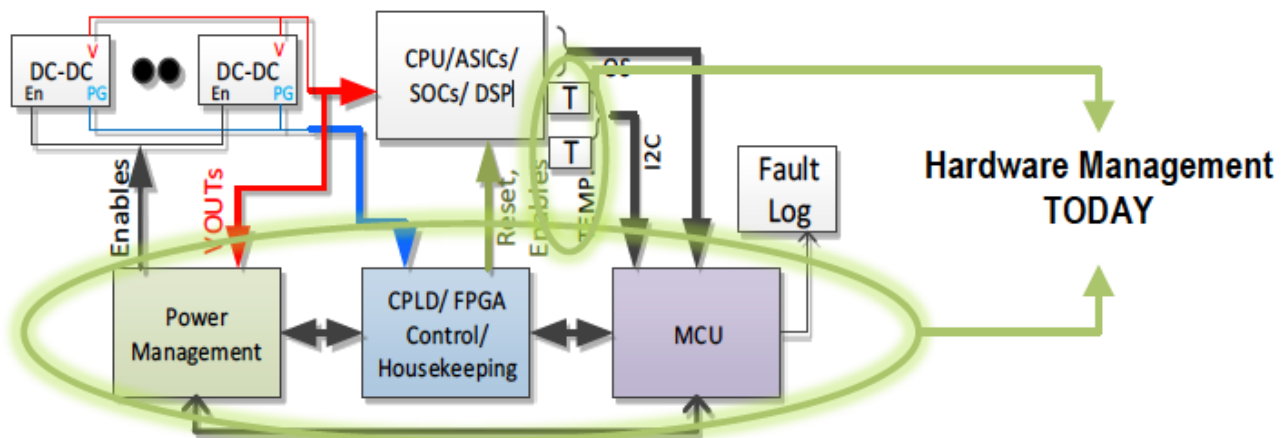


Figure 2 – Typical Hardware Management Architecture

Traditionally, system designers use power manager ICs to implement power supply sequencing, monitoring, trimming and margining. Control/housekeeping functions, including reset distribution, level translation, JTAG chain management and other board level glue logic are typically implemented in an on-board CPLD. Temperature management functions such as temperature monitoring and fan control are usually integrated into the on-board microcontroller firmware. The microcontroller also performs system-level functions such as fault logging, system interface, power control, management protocol and other operating system interface functions.

Disadvantages of the Traditional System Design Methodology

1. Increased Design and Debug Effort and Extended Time-to-Market

Typically, designers cut and paste the hardware management portion of the circuit board from one version to the next. However, the newer board payload hardware management functions often require different power, thermal and control/housekeeping functions. Designers still have to maintain some of the legacy functions from the older version of the board. Designers explore different approaches to transfer the new power and temperature management functions to the existing CPLD and/or microcontroller in order to minimize the number of components used on the board. Many times these approaches do not provide the most reliable solution.

For example, transferring power management functions to a microcontroller while maintaining the hardware requirements of fast system response to supply faults requires firmware to monitor each power rail at a higher frequency. This may reduce the microcontroller response time to other functions, for example management protocol and response. System designs may require a faster processor, or a processor with increased throughput to address this increased power management workload. This may call for redistribution of tasks between different design groups (hardware, firmware, etc.), which often results in increased design time.

Another shortcoming of microcontroller-based hardware management is that it cannot be simulated. As a result these hardware management functions can only be tested in a prototype board environment, reducing hardware management algorithm fault coverage and increasing system debug times.

In general, non-optimal hardware/firmware partitioning (forced by the limitations of the devices used to implement the hardware management functions) increases the complexity of the hardware management section, thereby significantly increasing its design and debug times.

2. Difficult to Scale/Cut and Paste Into New Designs

Designers prefer to cut and paste existing hardware management designs into a new revision of the board as is. This may not be possible, as newer functions required by the latest set of payload ICs are usually different from the older ones. As a result, designers are forced to rethink the partitioning of their hardware management functions.

In addition they may need to use additional analog ICs to either monitor power rails or device temperatures. Modifications to firmware are actively discouraged because of maintenance issues. Further complicating the use of the cut and paste methodology. As the board gets more complex (increased numbers of power rails, more power sequencing algorithms, the need for monitoring additional device temperatures, etc.), designers are forced to load additional functions into the CPLD or microcontroller.

In general non-optimal hardware/firmware partitioning forces designers to meet board specific hardware management functions with unique combinations of hardware/firmware solutions in addition to the use of different discrete devices. As a result, a single, standardized approach cannot be used for simple and complex boards.

3. Increased BOM and Costs

The use of different sets of ICs for each type of board increases the BOM by increasing the number of ICs used in a given system. As many ICs are used only in some of the boards, the components department will not be able to take advantage of economies of scale, increasing the overall cost of the system.

The traditional hardware management solution makes the hardware management designs more complex. The designs are more difficult to scale, more time consuming to design/debug, requiring more ICs and resulting in more expensive system solutions.

The following section describes a system design methodology that is seamlessly scalable, uses a PLD to implement the hardware management algorithm. This approach simplifies the firmware implementation, reduces design/debug time, increases board-/system-level reliability, and reduces component BOM and overall system cost.

Lattice's Revolutionary Hardware Management solutions

Lattice provides 2 devices that can be used to integrate the hardware management solution in a circuit board. They are the L-ASC10 Hardware Management Expander and the LPTM21 Platform Manager 2 – Hardware Management Controller. The L-ASC-10 (ASC) integrates rail voltage monitoring (10 channels), supply current monitoring (2 channels) and device/board temperature monitoring (3 channels). The ASC can also measure voltage, current and temperature using an on-chip ADC. The ASC and the MachXO2/3 (replaces the CPLD in the traditional solution) devices, together can integrate the circuit board hardware management functions.

The LPTM21 Platform Manager 2 device integrates the ASC functionality as well as a 1200 LUT FPGA. This is a single chip solution for the entire hardware management function. This single chip may be sufficient to meet the hardware management needs of some system boards.

Hardware management designs can be implemented by using the PowerAssist (a spreadsheet tool) and Lattice Diamond. These tools cut design time from days to hours.

A board using this Lattice hardware management solution can be debugged using the PowerDebug tool.

Lattice's hardware management solutions, design software and debug tools help address the disadvantages of traditional hardware management design. This is truly a “cut and paste” solution that can be used as a design standard from simple to complex boards.

The next section shows how Lattice's hardware management solution replaces the traditional hardware management design methodology, followed by a description of the device architecture and software tools.

Hardware Management Implementation Options

Lattice provides 2 options for implementing the hardware management solution in any circuit board as shown in Figure 3.

- Option #1: Hardware management functions can be added to the circuit board by using the L-ASC10 (Hardware Management Expander) in conjunction with the MachXO2 or MachXO3 (CPLD).
- Option #2: If a circuit board requires ~1000 LUT CPLD with I/Os less than 100 then one can use the single chip LPTM21 Platform Manager 2 device to implement the hardware management functions of that circuit board.

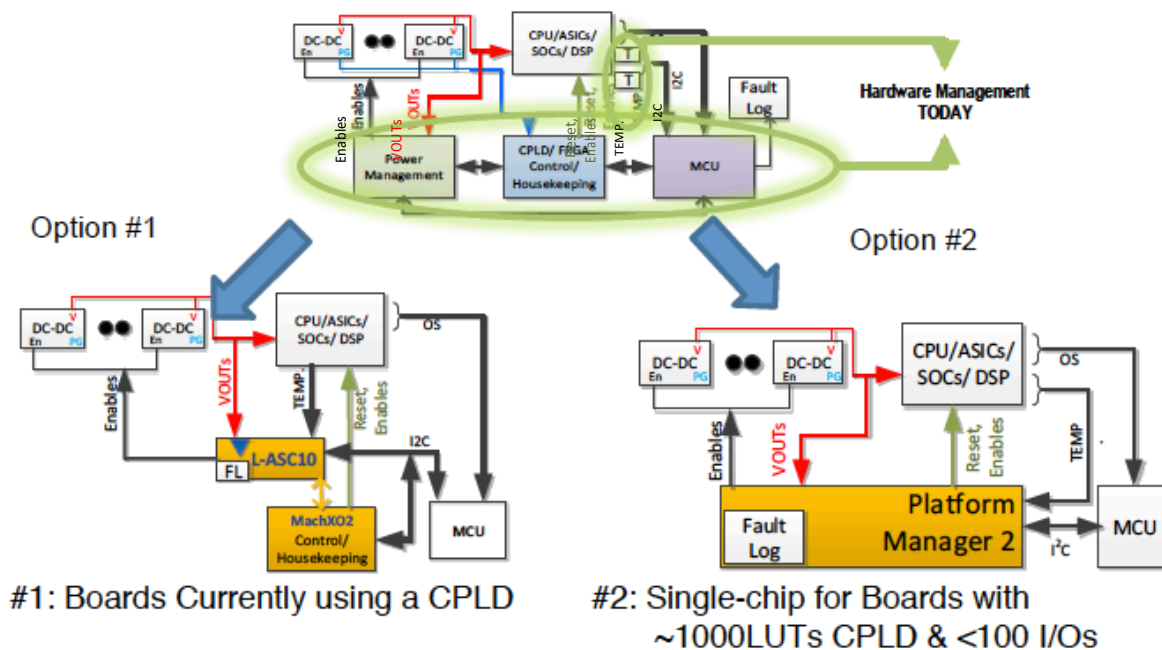


Figure 3 – Lattice Scalable, Low Cost, Standardized Hardware Management Solutions

Option #1

The ASC device together with the MachXO2/3 device integrate the hardware management functions. An algorithm implemented in the MachXO2/3 can monitor voltage rail status, supply current status and temperature status and sequence supplies through the L-ASC10. The MachXO2/3 can also control chip mounted or box mounted fans. This solution is scalable. For example, hardware management functions of boards with up to 20 rails can be integrated into the MachXO2/3 by adding 2 ASC devices to it. In general the hardware management designs can be scaled up to 80 rails by adding up to 8 ASC devices to the MachXO2/3. The logic and I/O requirements of the hardware management design can also be met by using the right size MachXO2/3. Lattice provides MachXO2/3 densities ranging from 256 LUTs to 9400 LUTs with I/Os ranging from 18 to 384. Designs with a wide range of complexities can standardize on the MachXO2/XO3 and ASCs as this solution uses the same design and debug environment. A detailed description of the ASC device features is provided later in this document.

Option #2

Lattice's single-chip LPTM21 Platform Manager 2 device can implement hardware management functions in boards that require around 1000 LUTs and less than 100 I/Os. Hardware management solution based on a single Platform Manager 2 device can handle up to 10 power rails. For system designs with more power rails, add additional ASC devices in conjunction with the Platform Manager 2 device. Designers can manage up to 40 rails using the LPTM21 Platform Manager 2 device by adding 3 companion ASC devices externally. A detailed description of the Platform Manager 2 device can be found later in this document.

The hardware management discussion in the remaining portion of this document is based on MachXO2 device and the ASC device, and is also applicable to designs using the Platform Manager 2 device.

Lattice's Hardware Management Advantages

Significantly Reduced Hardware Management Design/ Debug Time

Lattice ASC and MachXO2/3 devices make it very convenient to implement hardware management designs. Because the solution is seamlessly scalable, designers can simply cut and paste the solution from one board to another and implement board specific functions in the MachXO2/3. The microcontroller firmware performs only the higher system level functions. The MachXO2/3 performs all of the low-level, real-time, board specific hardware management functions.

For example, the firmware can issue a command "Turn Payload Supplies On" without needing to know about the number of rails on a given board. This command can be common to all the boards in the system. The firmware implements only the higher level system functions, and uses common commands across most boards, allowing usage across many boards with little or minor modifications, reducing firmware design time.

Another contributor to increased development time in hardware management design is power management. Power management designs are often implemented using power manager devices from different vendors and their associated GUI design software and/or analog discrete circuits. In most cases, the GUI-based software assumes that all sequenced supplies (DC-DC converters) are monitored by a single device. Often, due to cost or other reasons, it is

not possible to monitor all supplies that are sequenced. Designers are forced to implement sequencing of these supplies using other means. The need for power up and power down sequencing further complicates the power management circuitry, increasing the power management development time. The Lattice solution simplifies this by using a simple spreadsheet tool (PowerAssist) to implement the board specific power management functional specifications. This approach is more flexible and time efficient as the tool automatically generates the power management algorithm from the power management specifications. Using PowerAssist design time can be cut from days to hours.

The control/housekeeping and temperature management functions are implemented using the familiar design methodology for a digital designer, HDL. The digital designer can import the power management design and add it to the control/housekeeping and thermal management designs with one command. All functions are integrated into a single MachXO2/3.

The Lattice solution enables optimal hardware and firmware partitioning as it supports implementing all real-time hardware management functions in hardware (MachXO2/3) and higher level, less time-critical functions in firmware (external microcontroller).

Functions implemented in the MachXO2/3 and ASC can be simulated within the Diamond design environment to ensure that the hardware management functions are verified before transferring them to the actual board hardware. This increases first time success and reduces the time-to-debug.

Lattice also provides the PowerDebug tool which facilitates the measurement of temperatures, voltages and currents on the user board. It also provides additional functions, such as single stepping the power sequence and injecting board level power faults. These capabilities reduce board debug time significantly.

Increased reliability

The hardware management in a circuit board is analogous to the nervous system. Accurate fault identification, coupled with faster response time is required to ensure reliability of the system as it:

- Prevents the payload ICs from operating outside of their power and thermal specifications
- Minimizes fault propagation – Fault due to one section appearing as fault elsewhere

The ASC device enables the hardware management algorithms implemented within the MachXO2/3 device to monitor all power and thermal faults in parallel, with a high degree of accuracy (accuracy = 0.2% typ.). The ASC and MachXO2/3 devices provide a fully integrated hardware management solution with a fault response time less than 100 μ s. In contrast, traditional solutions have partitioned functions such as fault monitoring and responding to faults across multiple sections. In the traditional solution, each section uses different fault monitoring methods; voltage monitoring by the power manager, PowerGood signal monitoring by the CPLD and sequential voltage measurement by the microcontroller firmware. As a result, each of the hardware management blocks responds for supply faults at different points in time. The inaccurate and slow response to faults cannot prevent devices operating outside of their power and thermal specifications and reduces the overall reliability of the system.

This delay in fault response can cause faulty operation in other parts of the board. For example, if the voltage of a DDR memory is lower than the specified level, and if the processor is not reset immediately, the processor could read a wrong instruction from the memory and jump to an unexpected routine causing flash corruption or runt packet transmission. It is almost impossible to link the processor mis-execution of code to a dip in the DDR memory supply voltage. The combined MachXO2/3 and ASC based solution significantly minimizes such fault propagation by monitoring the voltage rails accurately and quickly activating a reset signal. The occurrence of such an intermittent supply fault can also be recorded as a fault log in the non-volatile memory for future debugging purposes.

The Lattice hardware management solution is highly scalable as the response time of the MachXO2/3 is unaffected with an increase in the number of power rails or temperature sensors in the system. As a result, the fault management algorithm is able to control both simple and complex boards alike. In contrast, the response time of the traditional solution degrades as the number of power supplies and other sensory inputs increase.

The Lattice solution supports logic simulation, which ensures that the behavior of the hardware management logic is checked for all types of fault handling conditions. The hardware management function can be simulated in its entirety using the Aldec Active-HDL simulator included in the Lattice Diamond software. In addition, the PowerDebug software supports circuit board behavior checkout. Both of these tools ensure that the board operates reliably.

Reduced BOM and Cost

The Platform Manager 2 and the ASC devices integrate most of the common, system-level voltage, current and temperature monitoring functions. There is no need for other voltage and temperature monitoring ICs. The Lattice solution easily performs all hardware management functions for the full range of circuit board complexity. This reduces the number of ICs used in a system. Because the solution is scalable, from simple boards to complex boards, the overall cost of the system is reduced.

The same set of design and debug tools can be used in boards with a wide range of complexities by using appropriately sized MachXO2/3s and the requisite number of ASC devices. To enable standardization on one MachXO2/3 family, Lattice MachXO2/3s cover a wide range of logic density and I/O combinations as shown in the table shown on the next page.

Features			MachXO2™								
Device			LCMXO2-256	LCMXO2-640	LCMXO2-640U	LCMXO2-1200	LCMXO2-1200U	LCMXO2-2000	LCMXO2-2000U	LCMXO2-4000	LCMXO2-7000
LUTs			256	640	640	1280	1280	2112	2112	4320	6864
EBR SRAM	# of Blocks		0	2	7	7	8	8	10	10	26
kbits			0	18	64	64	74	74	92	92	240
Distrib. RAM	kbits		2	5	5	10	10	16	16	34	54
UFM	kbits		0	24	64	64	80	80	96	96	256
sysDSP™ Blocks	18x18 Blocks										
	Multipliers										
PLL + DLL					1+2				2+2		
DDR Support					DDR 266, DDR2 266, LPDDR266						
Configuration Memory			Internal Flash								
Dual Boot ³			✓								
Bit-stream Encryption											
Embedded Function Blocks			I²C (2), SPI (1), Timer (1)								
Core Vcc	1.2 V		ZE & HE								
	1.8 - 3.3 V										
	2.5 - 3.3 V		HC								
Temp.	C		✓								
	I		✓								
	AEC-Q100										
0.4 mm Spacing											
WLCSP	25	2.5 x 2.5 mm				18			18		
	49 ²	3.2 x 3.2 mm						38			
ucBGA	64	4 x 4 mm	44								
0.5 mm Spacing											
QFN	32	5 x 5 mm	21				21				
	48	7 x 7 mm	40	40							
	84	7 x 7 mm								68	
csBGA	100	8 x 8 mm									
	132	8 x 8 mm	55	79		104		104		104	
	184 ¹	8 x 8 mm								150 ¹	
	132	8 x 8 mm									
TQFP	100	14 x 14 mm	55	78		79		79			
	144	20 x 20 mm			107	107		111		114	114
0.8 mm Spacing											
caBGA	256	14 x 14 mm						206		206	206
	332	17 x 17 mm								274	278
1.0 mm Spacing											
ftBGA	256	17 x 17 mm					206	206		206	206
	324	19 x 19 mm									
fpBGA	484	23 x 23 mm							278	278	334
	672	27 x 27 mm									

1) Contact your Lattice sales representative for the support of the 184-ball csBGA package, available with the HE option only.

2) Package is only available for E=1.2 V devices.

3) Dual Boot supported with external boot Flash.

Table 1A – MachXO2 Family

Features			MachXO3LF™					
Device			LCMXO3LF-640	LCMXO3LF-1300	LCMXO3LF-2100	LCMXO3LF-4300	LCMXO3LF-6900	LCMXO3LF-9400
LUTs			640	1300	2100	4300	6900	9400
EBR SRAM	# of Blocks		2	7	8	10	26	48
kbits			18	64	74	92	240	432
Distrib. RAM	kbits		5	10	16	34	54	75
UFM	kbits		24	64	80	96	256	456
Configuration Memory			Flash					
Dual Boot ⁴			✓					
Embedded Function Blocks			I ² C (2), SPI (1), Timer (1)					
Core Vcc	1.2 V		E					
	2.5 - 3.3 V		C					
Temp.	C		✓					
	I		✓					
0.4 mm Spacing			I/O Count					
WLCSP	36 ¹	2.5 x 2.5 mm		28				
	49 ¹	3.2 x 3.2 mm			38			
	81 ¹	3.8 x 3.8 mm				63		
0.5 mm Spacing			I/O Count					
csfBGA	121 ¹	6 x 6 mm	100					
	256 ¹	9 x 9 mm		206				
	324 ¹	10 x 10 mm			281			
0.8 mm Spacing			I/O Count					
caBGA	256	14 x 14 mm		206 ²				206 ³
	324	15 x 15 mm			279 ²			
	400	17 x 17 mm				335 ²	335 ³	
	484	19 x 19 mm					384 ³	

1) Package is only available for E=1.2 V devices.

2) Package is only available for C=2.5 V/3.3 V devices.

3) Package is available for both E=1.2 V and C=2.5 V/3.3 V devices.

4) Dual Boot supported with external boot Flash.

Table 1B – Mach XO3 Family

Analog Sense and Control (L-ASC10) Device Architecture

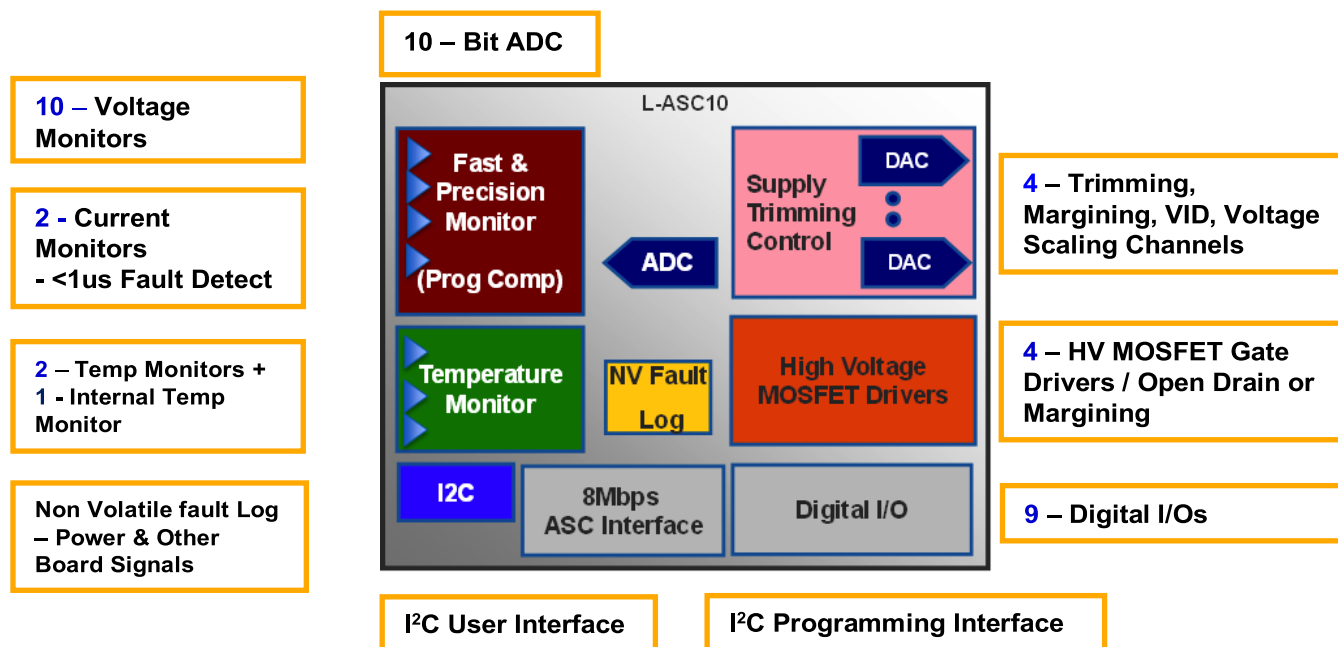


Figure 4: Analog Sense and Control (ASC) Device Architecture

The Analog Sense and Control IC (ASC), (hardware management expander), is used to scale the number of rails and temperature channels as required by a system design. The ASC chip contains 20 high precision (Accuracy = 0.2% Typ) programmable voltage threshold comparators that determines over and under voltage faults on 10 rails simultaneously. There are two current monitoring circuits, each with a programmable gain amplifier followed by two programmable threshold comparators. There is also a fast current fault detector that can capture current faults in less than a microsecond. The temperature monitor interfaces directly with temperature sense diodes to measure the temperature of a board-mounted device, or the temperature of a board at a given location. The temperature monitoring circuit also includes programmable threshold comparators.

The DAC can be used to trim and margin supplies and also implement functions such as VID (Voltage Identification Digital) – which controls the supply voltage using a digital code – and voltage scaling. The MOSFET drivers are used to steer a single voltage rail to multiple locations to meet the sequencing requirements of a device without using additional DC-DC converters.

Platform Manager 2 Detailed architecture

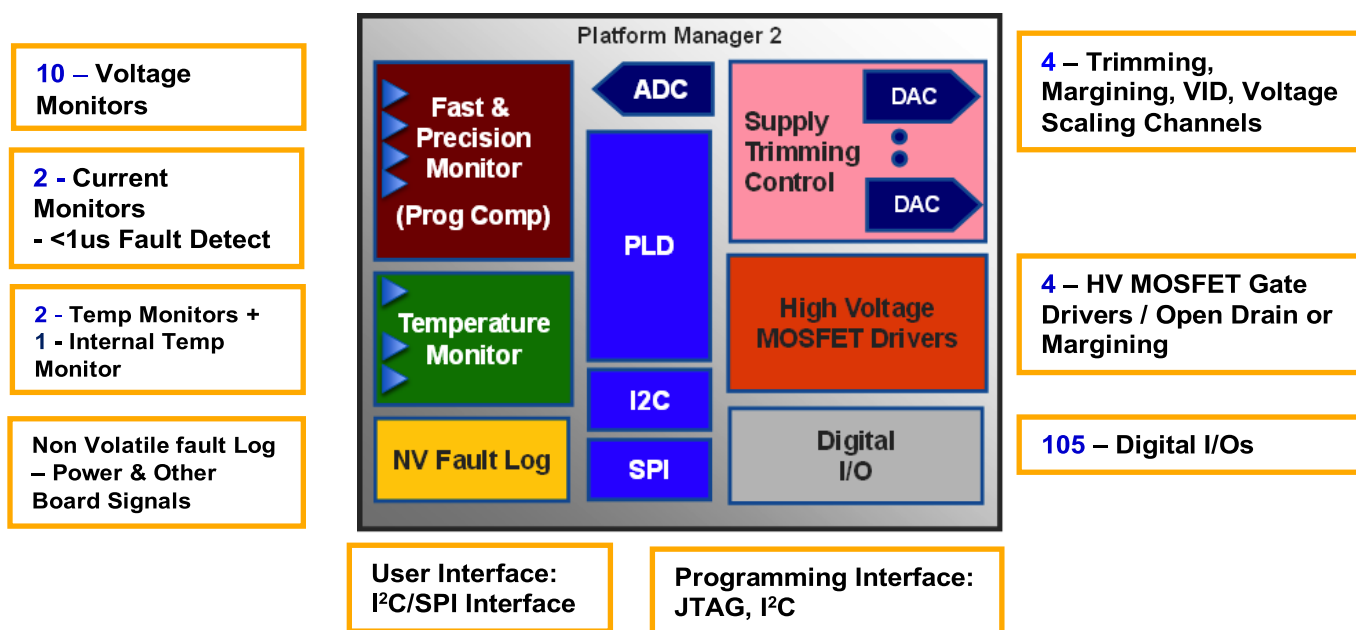


Figure 5 – Platform Manager 2 Architecture

The analog blocks of the Platform Manager 2 are identical to that of the ASC device. The on-chip 1200 LUT FPGA is used to implement the hardware management algorithm. The fault log section consists of a non-volatile memory that can be used to log voltage current and temperature faults. Table 2 outlines the key features of both the ASC and LPTM21 devices.

Table 2 - Platform Manager 2 and L-ASC10 Product Family

Ordering Part Number	L-ASC10-01SG48I	LPTM21-1AFTG237I/C
Voltage Monitoring Inputs	10	10
Current Monitoring Inputs	2	2
Temperature Monitoring Inputs	2	2
Number of Trimming Channels	4	4
MOSFET Drives	4	4
Open-drain 5V Tolerant I/O	9	10
On-Chip Non-Volatile Fault Log	✓	✓
Number of LUTs	-	1280
Distributed RAM (Kbits)	-	10
EBR SRAM (kBits)	-	64
Number of EBR Blocks (9 kBits)	-	7
User Flash Memory (kBits)	-	64
Number of PLLs	-	1
Communication I/F	I2C	I2C/JTAG
Programming Interface	I2C	I2C/JTAG
Operating Voltage	3.3	2.8V to 12V
Insystem Update Support	Yes	
Package Options	Digital I/Os	
48-pin QFN (7 X 7)	9	
237-Ball ftBGA (1mm) (17X17)		95

The ASC device transmits the voltage rail, supply current and temperature status to the MachXO2/3 device through an 8 Mbps serial link. Figure 6 shows how the ASC devices are connected to the MachXO2/3 device – or even with an LPTM21 Platform Manager 2 device – to expand the hardware management functions from a board with 10 rails to a board with up to 80 rails.

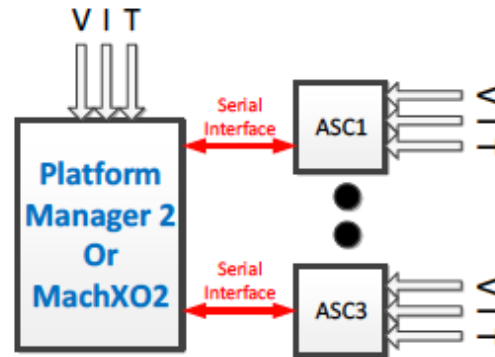


Figure 6 – Scalable H/W Management Architecture with Platform Manager 2 or MachXO2

The hardware management algorithm, from simple to complex boards, resides within the MachXO2/3 or within the FPGA section of the LPTM21 Platform Manager 2 device.

Application: Standard Hardware Management solution using MachXO2 and ASC(s)

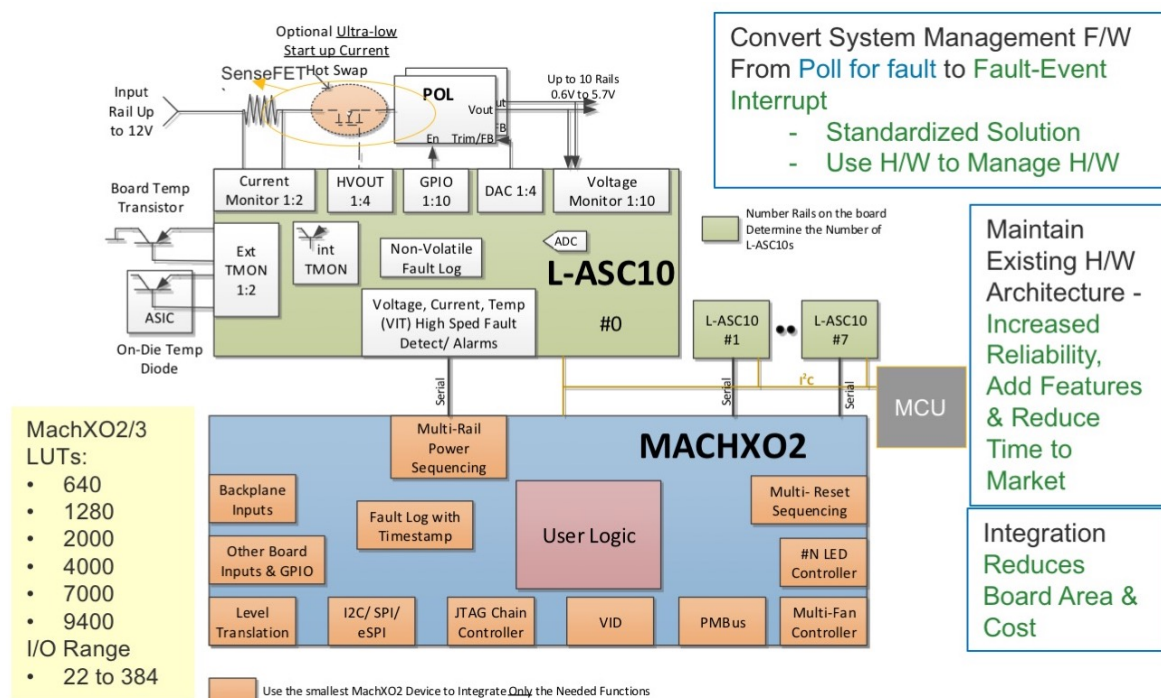


Figure 7: Hardware Management with the MachXO2 and ASC

The hardware management block diagram using Lattice ASC and MachXO2 devices (Figure 7) shows the ASC sensing the voltage, current and temperature status, and transferring them to the MachXO2 through a serial bus. The algorithm in the MachXO2 uses this status information to implement power management, temperature management and some of the control/housekeeping functions. The MachXO2 controls the GPIO and HVOUT pins of the ASC devices through the serial bus for power sequencing and DC-DC voltage control. Additional ASCs can be used to scale the power management algorithm.

An external microcontroller can measure the voltage, current and temperature values through the I²C Bus. The Microcontroller can also control the hardware management algorithm through the I²C Bus or through any other hardware bus by simply implementing the communication IP in the MachXO2 device.

This block diagram shows many of the hardware management functionalities integrated into the MachXO2 device – the same diagram applies for designs using the MachXO3LF. However, these functions are implemented as soft IP and can be used on an as-needed basis, enabling the size of the MachXO2/3 device to be determined completely by the functions needed in a given board. Users can also determine the MachXO2/3 package depending on the number of I/Os needed for that board.

The following sections show how the hardware management block diagram shown in Figure 7 can implement all of the main hardware management functions.

Power management

The power management algorithm in the MachXO2/3 monitors the rail voltage and controls sequencing of DC-DC converters connected to the ASC devices through the serial bus between the ASC and MachXO2/3. Up to 10 DC-DC converters can be managed through each ASC. Additional ASC devices are needed to manage more than 10 power rails. The power management algorithm can also trim and margin supplies through the ASC trim pins.

Scalable voltage monitoring and responding to faults:

Programmable threshold comparators in the ASC device monitor the voltage rails and transfer fault status to the power management algorithm in the MachXO2/3. The power management algorithm can use these supply faults from any of the ASCs and initiate responses in any/all of the power, temperature management or control/housekeeping sections immediately. If a supply is not monitored by the ASC, the power management algorithm can use the PowerGood signal from any of the un-monitored DC-DC converters to generate an appropriate response.

Scalable, flexible power up/down sequencing:

The power management algorithm can control sequencing of any DC-DC converter connected to any of the ASCs. The algorithm can also control the sequencing of the DC-DC converters connected directly to the MachXO2/3 pins. The sequencing of all supplies is controlled by a single algorithm that is centrally located in the MachXO2/3. The architecture is flexible and can handle any type (time driven, event driven, power up/down sequence order) of power on/off sequencing.

Trimming, margining, voltage scaling, VID:

The power management algorithm can manage the output voltages of the DC-DC converters connected to the ASC trim pins. The ASC device, through its on-chip closed loop control mechanism, maintains the output voltage of the DC-DC converter precisely (<10mV) at the voltage level specified by the power management algorithm.

Fault logging due to power fault:

The power management algorithm in the MachXO2/3 can capture an unexpected status into the on-chip flash memory, along with a time stamp, for further analysis at a later time. There are 2 types of fault logs supported by the MachXO2/3 and ASC devices. The fault log memory in each ASC can record all status information within that ASC device along with the reason for the fault log encoded in a byte. The fault log recorded within the MachXO2/3 device can consolidate the status information from all the ASCs along with a time stamp and any other system level information encoded in 4 bytes. The MachXO2/3 device can store hundreds of fault log records.

PMBus Support:

The PMBus adapter function can be integrated into the MachXO2/3 device. This lets a user implement power sequencing of DC-DC converters with PMBus (DPOLs) and those without the PMBus interface (APOLs) using a common algorithm stored in the MachXO2/3 device. The PMBus Master can monitor all the rail voltages and control the power management network using standard PMBus commands. This simplifies the PMBus mixed mode design. The architecture helps overcome some PMBus issues, including the ability to implement event and time based sequencing without involving the PMBus master. The architecture enables the design to take advantage of the PMBus standardized telemetry functions of both analog and digital point-of-load supplies, while eliminating the shortcoming of the PMBus standard's sequence and voltage scaling control features. The PMBus implementation does not need to be changed from one board to the next except to configure the board specific digital point-of-load supplies.

Voltage and Current Measurement:

The external microcontroller connected to the I²C Bus can measure supply voltages and currents through the I²C Bus using the ASC's integrated ADC. The microcontroller can perform measurements at any time without affecting the power management function performed by the algorithm in the MachXO2/3.

Temperature Management

The temperature management algorithm can be implemented in the MachXO2/3, the microcontroller or both. The temperature algorithm in the MachXO2/3 can use the ASC's on-chip programmable threshold comparator output. The temperature algorithm implemented in the microcontroller can use the temperature measured by the ASC's on-chip ADC (received over the I²C Bus).

Temperature management algorithm in MachXO2/3:

It is beneficial to include the temperature management algorithm within the MachXO2/3 device if the temperature management function is for devices mounted on the board or the box encapsulating the board. The MachXO2/3 device can integrate as many fans as needed using 2 I/Os and ~100 LUTs per fan. However, if the algorithm was implemented in

a microcontroller, designers have to use either a microcontroller with an integrated fan controller driver or use external fan controller ICs. Consequently, the solution can result in increased costs, or an increased BOM, or both.

Temperature management in the external microcontroller:

It is beneficial to use the microcontroller to perform temperature measurements through the ASC's I²C Bus, if the temperature management function resides outside of the board. An example application is a shelf/rack with multiple plug-in boards. The shelf manager, one of the plug-in boards, controls the fan tray mounted over the shelf. The microcontroller in this case measures temperature from different locations on the plug-in boards and transfers the measurement to the shelf manager. Even when the temperature management is implemented in a microcontroller, there is no need to use traditional temperature sense ICs, as the temperature sense and measurement interface are already integrated into the ASC device. The ASC device integrates three temperature measurement channels. The hardware management solution using MachXO2/3 and ASC can reduce overall BOM and costs.

Reducing the device power to control temperature

Some applications resort to graceful degradation of overall system performance, through voltage and frequency scaling, to control the ambient/device temperature, as opposed to shutting the system down under an over temperature condition. In such applications, an optimized temperature management algorithm in the MachXO2/3 can automatically reduce the device operating voltage and operating clock frequency and increase it when the fault clears. If the temperature fault condition persists after the throttling of the power dissipation, the temperature management algorithm can initiate power down sequencing and prevent fire hazards due to an overheated circuit board/device.

Fault log due to temperature fault:

It is beneficial to log the status of all sensors (voltage, current, temperature and other control functions) in a board in one non-volatile memory location. Complete information of all sensory input status helps to reduce board repair time at a later date. The algorithm in the MachXO2/3 can initiate a fault log due a thermal fault in addition to the supply rail fault using the ASC's on-chip programmable threshold comparator status output. The fault log feature can be used independently of the location of the temperature management algorithm.

Control/Housekeeping

Designers can integrate common control/housekeeping functions by importing HDL and assigning pins in the MachXO2/3 as they did before. Because the control/housekeeping function is integrated along with the power and thermal management functions within the same MachXO2 device, it is very easy to implement control plane response to a fault detected in other blocks. The response is very fast and is based on accurate fault monitoring capabilities of the ASC device. In contrast, the traditional solution requires that the CPLD monitor power status using the PowerGood signals generated by the DC-DC converter and the temperature status generated by the temperature sense ICs. This increases the number of I/Os in the CPLD and increases cost.

Fault log due to control/housekeeping fault:

The time required to fix/debug faulty boards can be reduced significantly by indicating the cause of the board shutdown. Often, it is not enough if the logged status includes only the power and temperature sense status. If the fault log contains additional information, such as an unexpected board extraction event or clock fade event or SEU event which caused the board shutdown, the board repair personnel could go directly to that portion of the circuit board instead of getting side tracked by an unconnected status map. It reduces “No Fault Found” cases.

All the functions described in the preceding application section can also be implemented within the LPTM21 Platform Manager 2 device. The only limitation to using this device is that the total logic needed for this application should be less than 1200 LUTs, and the number of I/O needed should be less than 100. Such applications can take advantage of this single chip solution to implement the entire hardware management of the board.

Design Tools

Hardware management designs can be implemented using two tools from Lattice; PowerAssist and Lattice Diamond. Further, board designs can be debugged using Lattice’s PowerDebug tool

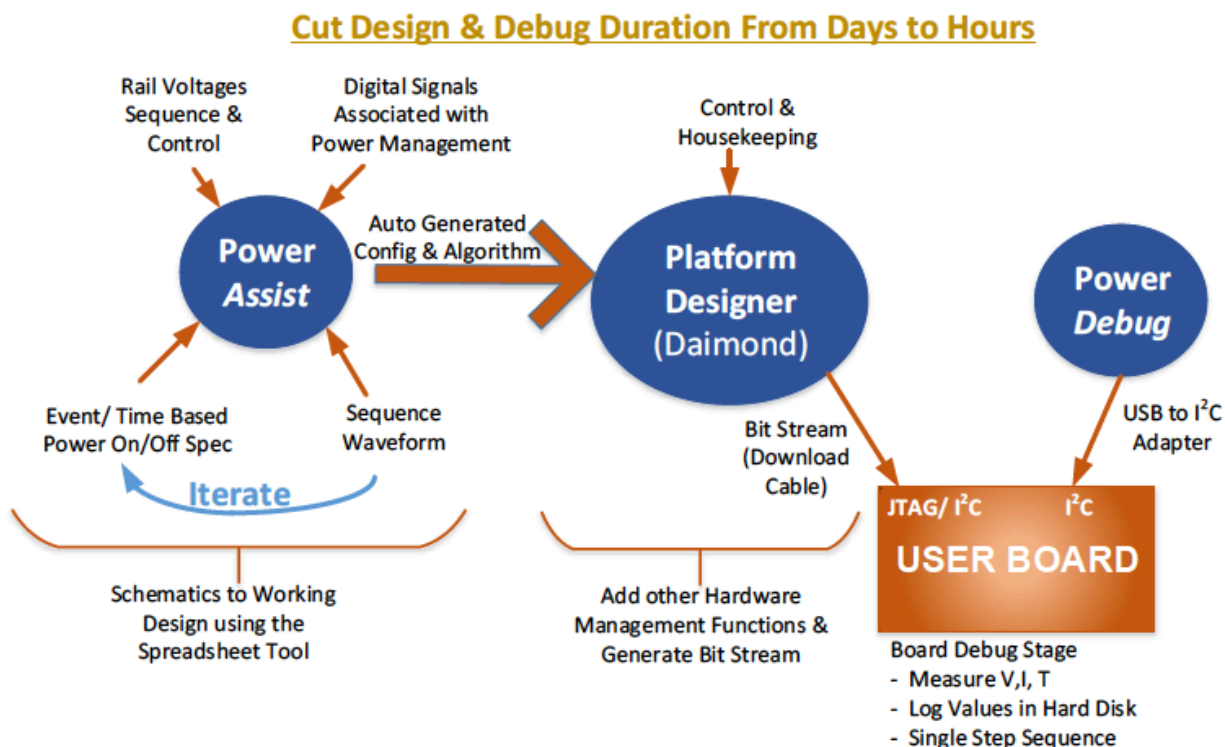


Figure 8: Platform Manager 2 Design Environment

The power management algorithm for traditional power manger ICs requires the use of proprietary GUI interface software. These tools assume that all supplies on the board are monitored and or controlled by these power management ICs. Typically, board designers do not monitor all the rails on the board. This means that the sequencing of those supplies should be handled separately using other methods. Furthermore, if the design uses multiple power manager ICs, the sequencing algorithm must be partitioned. These design considerations complicate the power management design.

The PowerAssist tool addresses almost all types of power networks uniformly, including monitored, unmonitored, sequenced and un-sequenced supplies. There is no need to partition the sequencing algorithm. PowerAssist lets power designers specify the board power network, digital signals controlling power network, power-on and power-off sequencing in a spreadsheet. Designers can verify power up/down sequencing using waveforms within this spreadsheet environment and click on a button to auto-generate the code for board sequencing and monitoring. No coding by the power engineers is needed. There is no need to partition the power sequencing between power manager devices. This process of auto-code generation from the specifications, significantly reduces the time-to-market for the power management design.

The board digital designers can then import the design and add their control/housekeeping algorithm implemented in HDL. This design tool is named Platform Designer, which is integrated into the Lattice Diamond software. The IPs needed to implement the power management functions (such as the IP to drive the serial interface between the MachXO2/3 and the ASC, fault log IP, VID IP) are automatically customized and added to the user design. The board designer can treat the entire power management algorithm as a black box, and add it to the control/housekeeping section. Alternatively, the board designer is free to implement the entire power management function in HDL. Lattice Diamond is a popular software tool used for implementing control/housekeeping functions. The board designers are able to use a familiar method to implement the sections of the hardware management as needed.

The resulting design can be simulated end-to-end (from power management including automatically generated IPs to control/ housekeeping and thermal management) using the standard test bench method. The power management simulation boundary starts at the ASCs. The simulation model includes the ASC model as well as the bus transfer model used by the ASC to communicate with the MachXO2/3 devices. This increases the chances of first time success in hardware.

The PowerDebug, a PC-based software tool, helps measure the voltage, current and temperature of a working board. It is possible to log the value of all voltages, currents and temperatures into a PC hard disk for detailed analysis. The PowerDebug tool also helps inject faults into the board being debugged to ensure the hardware management algorithm is able to handle all supply faults, increasing the reliability of the board while reducing board debug time.

Power supply sequencing in complex boards typically require special attention. If there is coupling between any two power domains, some of the ICs may not power up sequence or worse, the device may gradually fail because of these leakages. PowerDebug software enables single stepping of supplies in the user board and is controlled by the PC. The user can turn on the board partially and measure all the residual voltages on the board, which helps identify leakage paths and further reduces time-to-market.

Evaluation tools

Designs in ASC/LPTM21 can be tested in hardware using the Platform Manager 2 evaluation board and ASC break out board. The PowerDebug tool can be used to demonstrate various Platform Manager 2 features as well as debug user algorithms.

Platform Manager 2 Evaluation Board

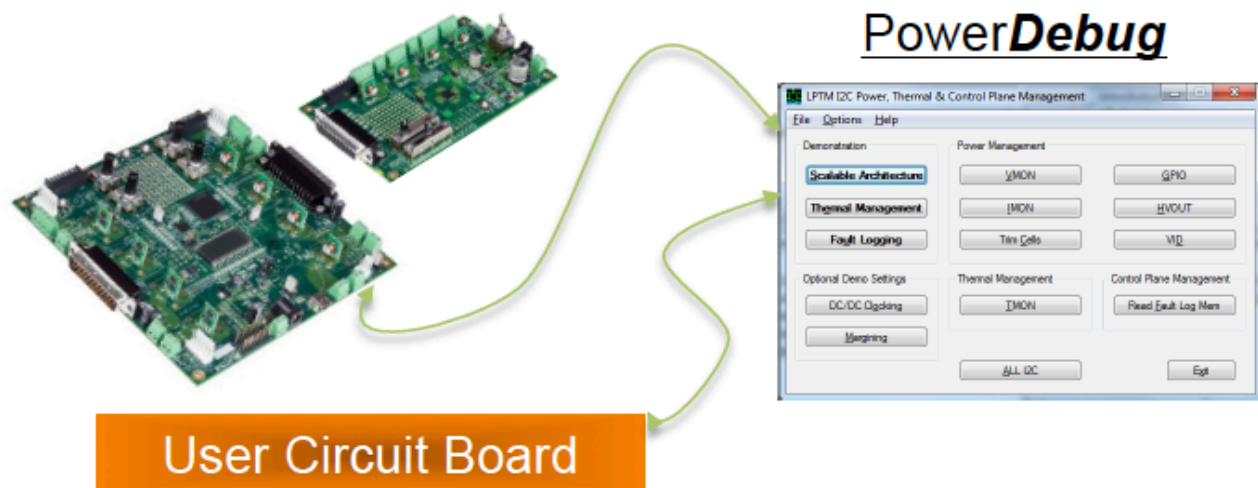


Figure 9 –Platform Manager 2 and ASC evaluation boards & PowerDebug software tool

Accelerate your MachXO3 designs with our new development kit:
www.latticesemi.com/Products/DevelopmentBoardsAndKits/MachXO39400DevBoard