SEU Demo for the ECP5™ Versa Development Board User Guide

UG92 Version 1.1, August 2015

Introduction

This document provides technical information and instructions for using the SEU (Single Event Upset) demo design. This demo demonstrates the functionality of the SED (Soft Error Detection) using the ECP5 Versa Development Board. The ECP5 Versa Evaluation Board, USB cable, power supply and demo files are included in the ECP5 Versa Development Kit. This document provides a description of the demo design as well as instructions for running the demo.

This demo design makes use of Lattice Diamond® software feature of SEI (Soft Error Injection) to induce SRAM bit-flipping. This bit-flipping is then detected by the FPGA SED running on the board.

Demo Package

The demo package includes the following:

- Verilog source code for the demo logic design
- Lattice Diamond project file and preference file for the demo project
- SEU demo bitstream
- SEI bitstream for soft error injection

Hardware Requirements

- ECP5 Versa Development Board
- 12 V DC power supply for the ECP5 Versa Development Board
- USB cable for programming the ECP5 device

Software Requirements

- Lattice Diamond design software, version 3.5 or later
- Programmer software for bitstream downloading

Demo Design Overview

This demo design consists of two major parts: SED module and the user logic. The SED module performs read and error detection of SRAM content. The user logic includes soft error indication and a function block that rotates the LEDs on board. The status of the demo is indicated with on-board LEDs. A SEI bitstream is used to induce SRAM error. This SEI bitstream is generated with SEI editor under Tools tab in Diamond.

Figure 1. ECP5 Versa Board

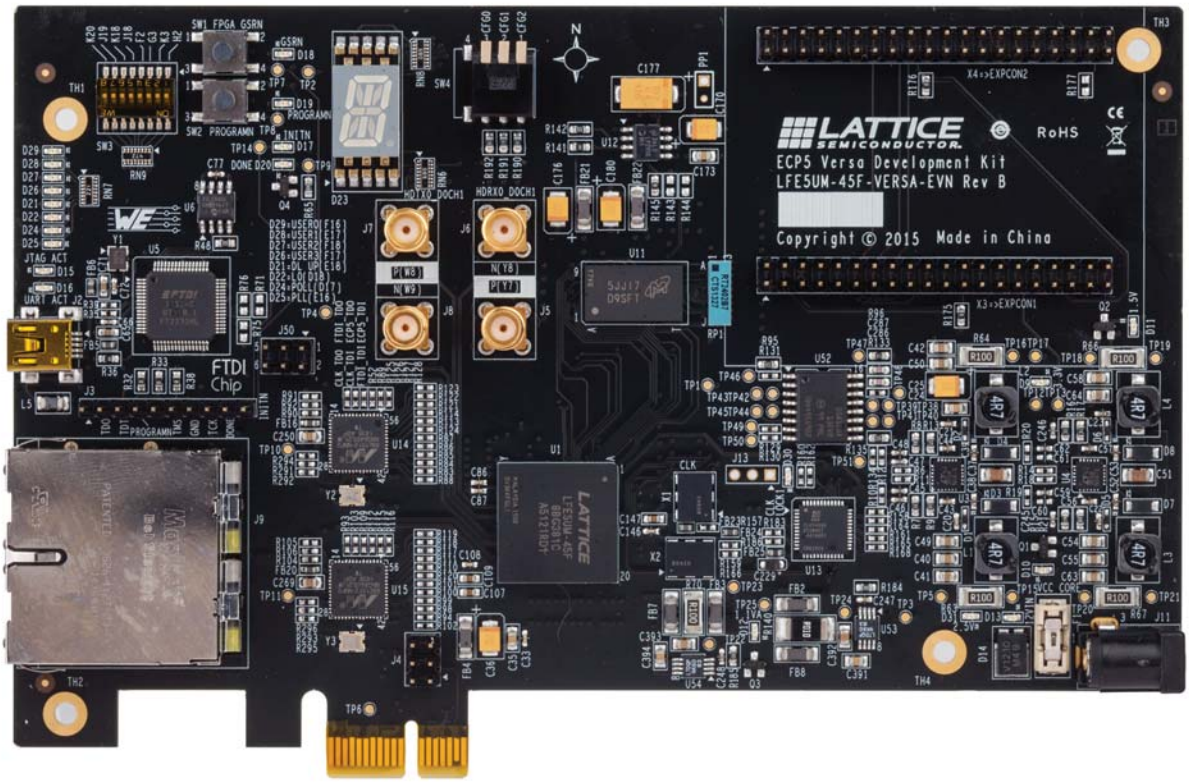
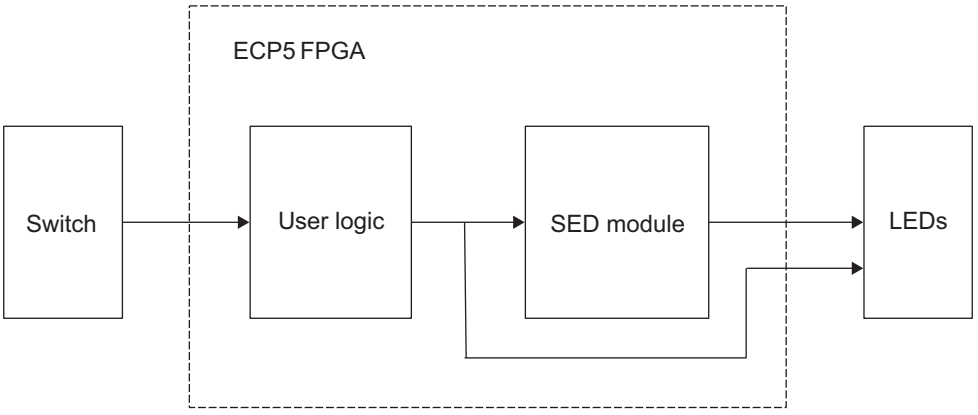


Figure 2. SEU Demo Design Block Diagram



Port Assignments and Descriptions

Table 1. FPGA Demo Design Ports

Port Name	Direction	Description
clk	Input	Clock for user logic
reset_n	Input	GSRN button on board. Asynchronous reset for FPGA
sw[1:0]	Input	DIP switch on board
led[7:0]	Output	LEDs on board
sed_err	Output	SED error indication

Table 2. DIP Switch Definitions

SW3 On Board	Position Definition	Description
#8	1: towards board edge	SED enable
#7	1: towards board edge	SED start

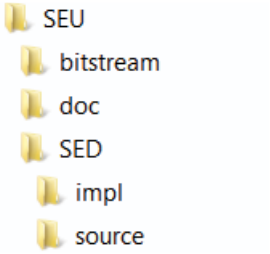
Table 3. LED Definitions

LED On Board	Description
D29, D28, D27, D26, D21, D22, D24, D25	Rotating from D29 to D25. Indicate the user logic is running
Dot on segment LED D23	Indicate SED error

Demo Package Directory Structure

The demo bitstreams are located in SEU\bitstream. The Diamond project is located in SEU\SED\impl.

Figure 3. SEU Demo Package Directory Structure



Running the Demo

To run the demo:

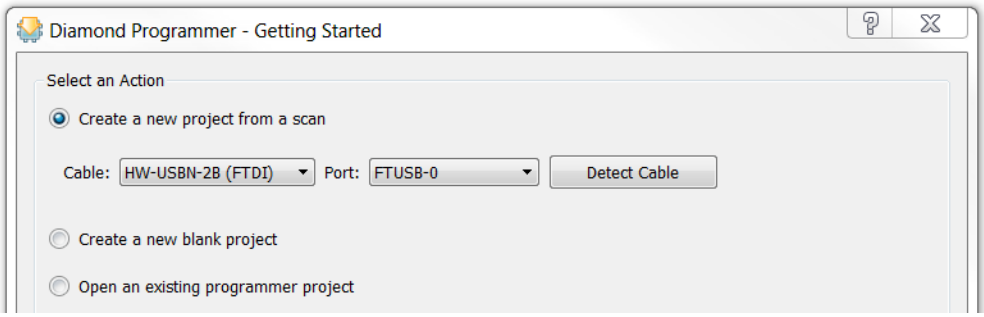
1. Before the board is powered up:

   J50 should have pin #1 jumpered to pin #2, and pin #3 jumpered to pin #5. This puts ECP5 in the JTAG scan chain as the only device.

   DIP Switch SW4 should have all positions UP (corresponding to a 111 setting). DIP switch SW3 should have all positions set to ON.

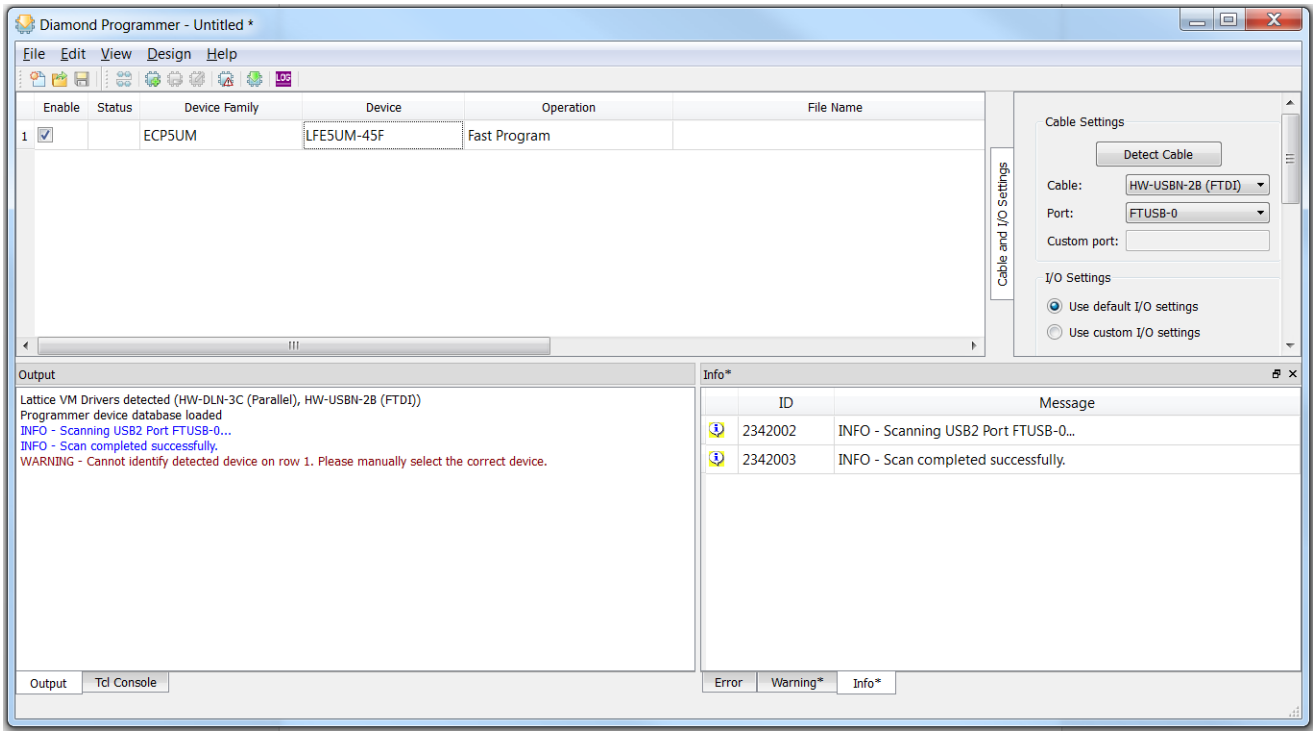
2. Power up the board with 12 V power supply. Connect the board to a PC with a USB cable.
3. Launch the Programmer software.

Figure 4. Getting Started



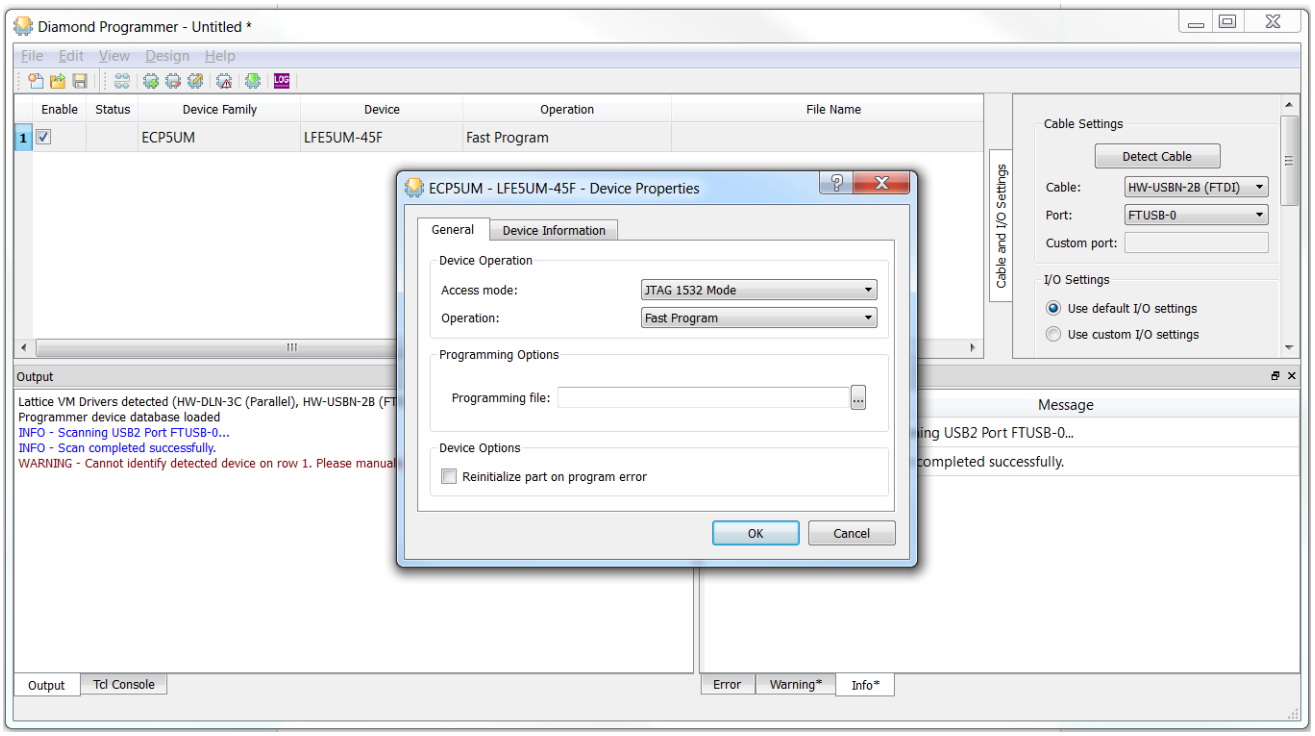
4. Scan the JTAG chain by selecting the **Scan Chain** button if the device is not detected.
5. Select the **LFE5UM-45F** device.

Figure 5. Selecting the Device



6. Select **Fast Program** and the original bitstream **SEU\bitstream\LED.bit** to be programmed then start programming.

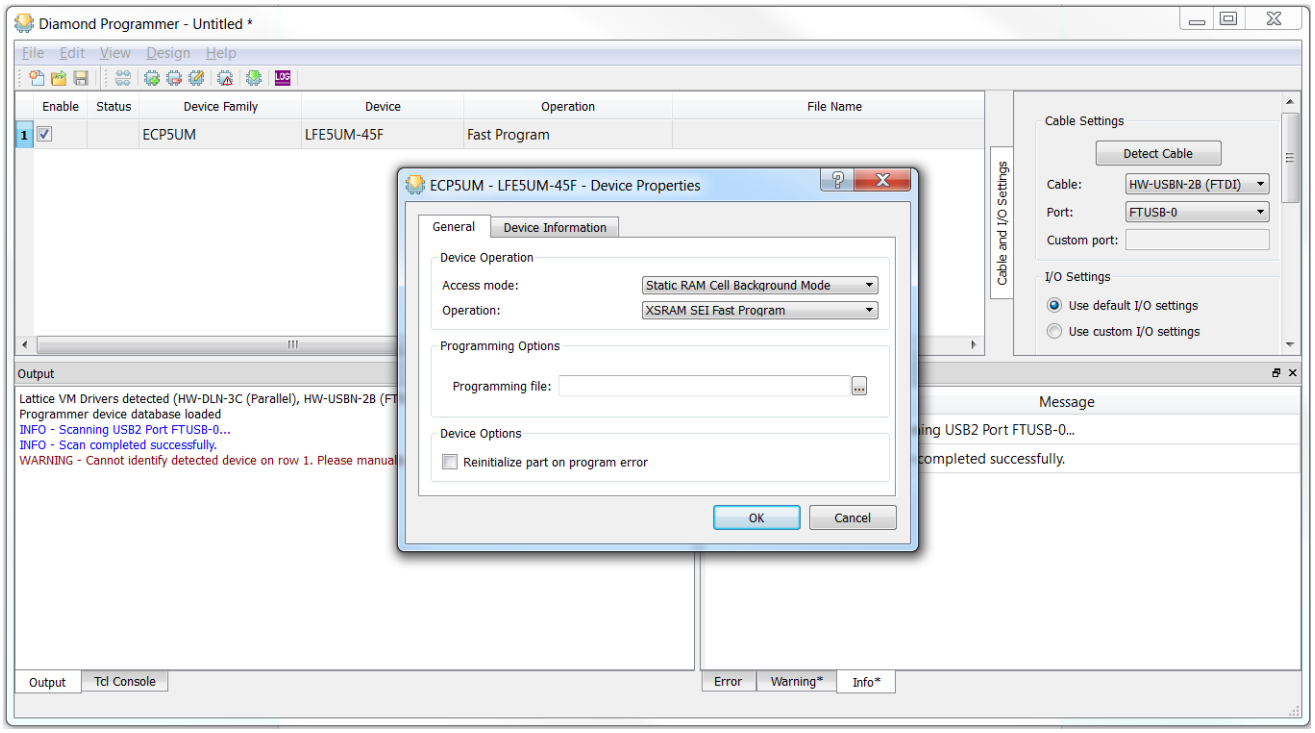
Figure 6. Device Properties



Rotating LEDs are seen on board once the FPGA programming is completed.

7. Set SW3 pin #8 then #7 positions to OFF, there should be no SED error indication (dot on segment LED D23 is not lit).
8. Set SW3 pin #8 then #7 positions to ON.
9. Select **Static RAM Cell Background Mode** and X**SRAM SEI Fast Program** in Programmer. Specify the SEI bitstream SEU\bitstream\SED_sei_0.bit then start programming.

Figure 7. Selecting Access Mode and Operation



10. The LEDs D29 to D25 should keep rotating when the SEI bitstream is being programmed. This indicates that there is no interruption to the currently running bitstream on the device. The DONE LED (D20) will cycle off briefly at the end of the programming operation.
11. Set SW3 pin #8 then #7 positions to OFF, there should be SED error indication (dot on segment LED D23 is lit).
12. Repeat Step 6 or Step 9 to program the original bitstream SEU\bitstream\LED.bit to eliminate the SED error.

Developer Notes

To develop your own FPGA design to make use of the SEI flow:

1. SED module needs to be included in the FPGA design. This is a hard module and does not use any fabric logic.
2. When a bitstream is generated, BACKGROUND_RECONFIG should be set to ON in Diamond.
3. SEI feature in Diamond software is enabled with a software license. The developer needs to request a license for SEI feature. Otherwise, the SEI feature is not available in Diamond.

Demo Design Dependencies per Development Board Revision

The bitstream included with the demo design has been developed for the ECP5 Versa Development Board Revision B. The key updates to the Revision B development board with respect to the SEU demo include the following:

1. Revision B uses SW4 to set the configuration mode for ECP5. Revision A uses a resistor population scheme to set the configuration mode. Working with the SEU demo on the Revision A board requires that R182, R188, R189, R190, R191, and R192 are populated.
2. The ECP5 pinout with respect to the on-board DIP switches and LEDs has been updated for Revision B of the hardware. Specifically the SW[1] assignment in the demo project is location K19 for Revision B. SW[1] is assigned to location J19 for Revision A.
3. The demo bitstreams have been built with Diamond 3.5 for use with Revision B of the ECP5 Versa Development Board. The demo project must be rebuilt with Diamond 3.4 for use with Revision A.

References

- EB98, ECP5 Versa Development Board User Guide

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Date	Version	Change Summary
August 2015	1.1	Document update to support ECP5 Versa Development Board Rev B.
April 2015	1.0	Initial release.