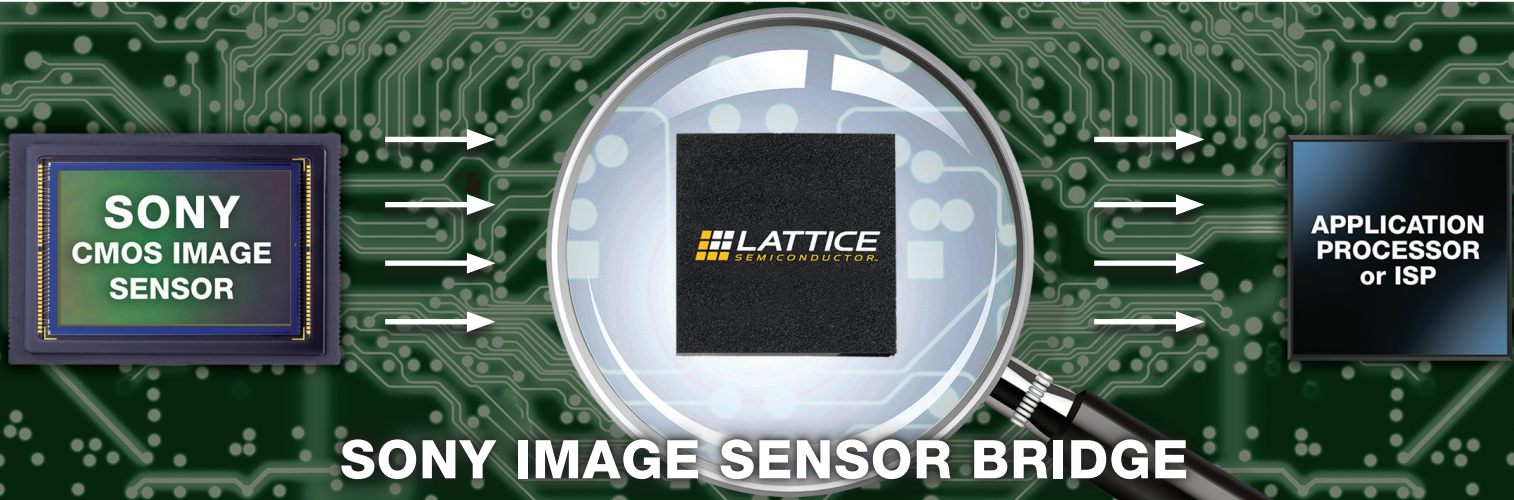


The Integration Enabler

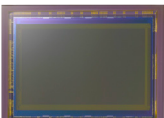


Lattice FPGAs offer you the freedom to connect between Sony's broad line of CMOS image sensors and various industry standard applications processors (APs) or image signal processors (ISPs), thus giving you the ability to design your next camera-based sub-systems without compromise. You get the needed flexibility without busting your space, power or cost constraints.

Don't get caught between emerging standards and fixed interface protocols.



Sony sub-LVDS Image Sensor Bridge Interfaces already available in multiple configurations

	Sony CIS Bridge Examples					
	Sony sub-LVDS Interface	Sony IMX Example	AP/ISP Interface	AP/ISP Max Bus Width	Max AP/ISP Data Bit Bus Speed	Smallest Package Size
	4 data	IMX136	Parallel	12 bits	162 Mhz	49 wlcsfp
	4 data	IMX172	CSI-2	4 data lanes	900 Mbps	49 wlcsfp
		IMX236	CSI-2	4 data lanes	900 Mbps	49 wlcsfp
	8 data	IMX178	CSI-2	4 data lanes	900 Mbps	81 wlcsfp
	10 data	IMX226	CSI-2	4 - 8 data lanes	900 Mbps	121 fcBGA

Lattice's low power, low cost XO2, XO3L and ECP5 offered in amazingly small packages! (see reverse for details)

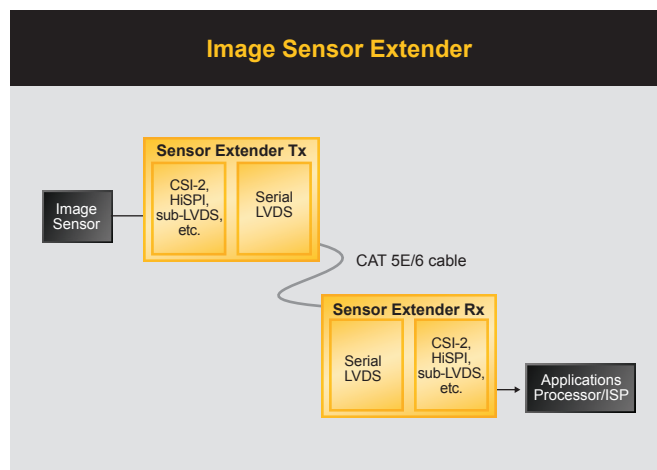
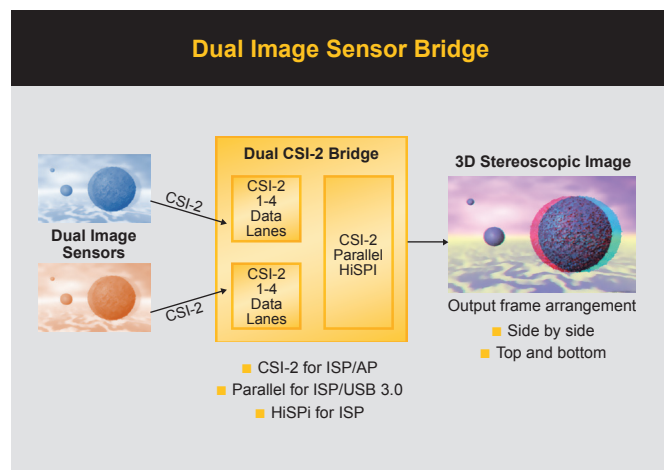
	49 WLCSP	81 WLCSP	121 fcBGA	132 csBGA
				
	3.2 x 3.2 mm 0.4 mm pitch	3.8 x 3.7 mm 0.4 mm pitch	6.0 x 6.0 mm 0.5 mm pitch	8.0 x 8.0 mm 0.5 mm pitch

The Integration ENABLER

SONY IMAGE SENSOR BRIDGE



A variety of bridging possibilities available!



Choose from Lattice's array of integration solutions and speed your design to market.

XO2 Series (smallest package option only shown)		49 WLCSP (3.2 x 3.2 mm) 0.4 mm pitch	132 csBGA (8 x 8 mm) 0.5 mm pitch	256 csBGA (14 x 14 mm) 0.8 mm pitch
	LUTs	2000	4000	7000
	D-Phy speed/lane (Mbps)	420	750	750
	D-PHY interfaces Rx/Tx	1/1	2/1	2/2
	MachXO2	XO2-2000ZE	XO2-4000	XO2-7000

XO3L Series (smallest package option only shown)		49 WLCSP (3.2 x 3.1 mm) 0.4 mm pitch	81 WLCSP (3.7 x 3.8 mm) 0.4 mm pitch	121 csfBGA (6 x 6 mm) 0.5 mm pitch	121 csfBGA (6 x 6 mm) 0.5 mm pitch	256 csfBGA (9 x 9 mm) 0.5 mm pitch
	LUTs	2100	4300	1300	2100	6900
	D-Phy speed/lane (Mbps)	900	900	900	900	900
	D-PHY interfaces Rx/Tx	1/1	2/2	2/1	2/2	2/2
	MachXO3L	XO3L-2100	XO3L-4300	XO3L-1300	XO3L-2100	XO3L-6900

ECP5 Series (smallest package option only shown)		285 csfBGA (10x10 mm) 0.5 mm pitch	285 csfBGA (10x10 mm) 0.5 mm pitch	285 csfBGA (10x10 mm) 0.5 mm pitch
	LUTs	24000	45000	84000
	D-Phy speed/lane (Mbps)	800	800	800
	D-PHY interfaces Rx/Tx	2/2	2/2	2/2
	ECP5	LFE5U-25*	LFE5U-45*	LFE5U-85*

* Available in mass production in early 2015

Get more information at: www.latticesemi.com/sonysublvds

Applications Support

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