ENABLING PROGRAMMABLE CONNECTIVITY SOLUTIONS FOR COMPACT, HIGH VOLUME APPLICATIONS

A Lattice Semiconductor White Paper

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Introduction

A new generation of compact, low power and low cost SERializer/DESerializer (SERDES) enhanced field programmable gate arrays (FPGAs) are increasingly being used with application specific integrated circuits (ASICs) and application specific standard products (ASSPs) by equipment designers to rapidly build flexible systems that meet tight cost, power and form factor constraints of many emerging high volume applications. These SERDES-enhanced FPGAs break the rule that FPGAs must be high density, power hungry and expensive having been optimized for low cost, small form factor and low power consumption, making them ideal for delivering programmable connectivity solutions to complement ASICs and ASSPs.

To take advantage of SERDES-enhanced FPGAs' unique capabilities, designers must understand a bit about how they work, as well as some of their thermal, electrical and signal integrity requirements. The material presented here is intended to familiarize you with this new breed of devices, the benefits they offer and introduce the design practices needed to successfully use them. Using FPGA family with embedded SERDES, it can introduce several important issues which can affect the performance of the SERDES-based device, and practical solutions which you can apply to your design. Most of the issues covered here will apply to the 3.25 Gbps SERDES transceiver cores found in many SERDES-enhanced FPGAs currently on the market, but it will also discuss some of the unique features Lattice has added to the ECP5™ platform to its improve performance and design flexibility.

The FPGA+SERDES Advantage

Originally developed for high-performance packet processing and routing elements in carrier-class networking equipment, FPGAs equipped with embedded SERDES transceivers have been available for over a decade. These large, powerful devices were fabricated using the architectures and processes designated for the manufacturers' "flagship" product lines, and cost hundreds, or even thousands of dollars each. Since

then, manufacturers have used a decade's worth of advances in sub-micron semiconductor processes to address the needs of emerging, more cost-competitive markets.

These value-priced low- and moderate-density FPGAs deliver most of the performance and features available in previous generations of top-tier products and are available in a wide range of capacities. Offering low power consumption, competitive pricing and compact packaging options, this new generation of FPGAs allows designers to choose the amount of programmable elements and application-specific hardware cores they need to meet their product's requirements. As a result, the total solution cost of FPGA-based designs is approaching parity with conventional designs for many applications.

In addition, strategic use of FPGAs can free designers from many of the obstacles they'd face in a traditional development cycle. By offering much lower development costs, and shorter schedules, and eliminating the inflexibility and supply chain issues associated with merchant silicon (ASSPs), FPGAs make it possible for designers to respond rapidly to emerging market opportunities.

Applications

Combining low-power multi-Gigabit SERDES transceiver cores with a price-optimized FPGA architecture creates a versatile solution platform for applications which make extensive use of SERDES-based interfaces such as Ethernet (XAUI, GbE, SGMII), PCIe (PCI Express) SRIO (Serial RapidIO) and Common Public Radio Interface (CPRI). These include small-cell wireless infrastructure, microservers, broadband access, industrial video and other high-volume applications where low cost, low-power, and small form-factors are key design constraints.

Many of the early applications to embrace SERDES-enhanced FPGAs have been innovative RF, baseband and backhaul products which address the needs of wireless network operators. Virtually every carrier throughout the world is making massive investments to upgrade their infrastructure as they struggle to keep pace with the

explosive growth in demand for mobile data and video traffic. In addition to upgrading their existing base stations to support high-capacity 3GPP/4G wireless standards, many operators are embracing a new Heterogeneous Network (HetNet) architecture in which the traditional macro infrastructure is supplemented by a new class of low power nodes (LPNs) such as small cells, low power remote radio heads, and relays (Fig.1).

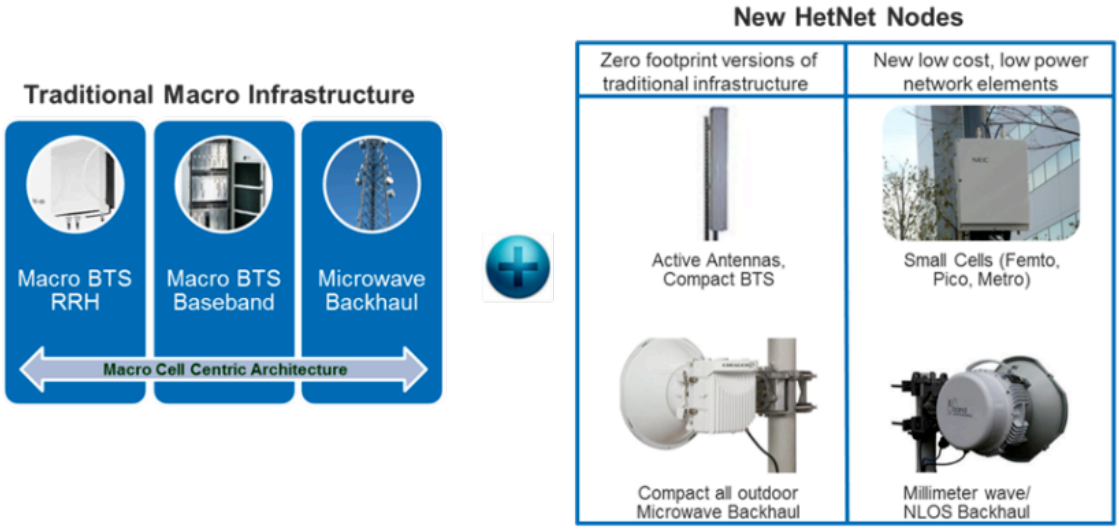

Fig.1: Today's evolving wireless Heterogeneous Networks (HetNets) combine "zero footprint" versions of traditional macro architecture with a variety of new low power, low cost network elements.

These compact, low-power (typically between 100 mW and 10 W) wireless nodes can add capacity in high-traffic areas or extend wireless coverage into buildings, public spaces, and urban canyons which are beyond the reach of conventional base stations. This requires LPNs to be highly configurable in order to support multiple air interface standards and RF frequencies, compact and rugged enough to blend into the urban landscape, and inexpensive enough to justify widespread deployment.

Indoor Pico cells (~1 W) almost always benefit from using an FPGA which combine high speed logic with SERDES and flexible I/O interfaces, as well as DSP capability in a small footprint package (Fig.2). Their programmable logic elements can be used to implement limited digital front end (DFE) functionality such as crest factor reduction

(CFR). In pico-cell designs which use a baseband SoC, the FPGA's SERDES capabilities can provide the CPRI connectivity needed to connect it to the radio's AFE. In DSP-based pico-cell designs, the FPGA can be used as a companion element for the signal processor and its I/O elements can be used to implement the LVDS/JESD204B interfaces which used to connect the data converters at the DSP's inputs and outputs with the radio's AFE.

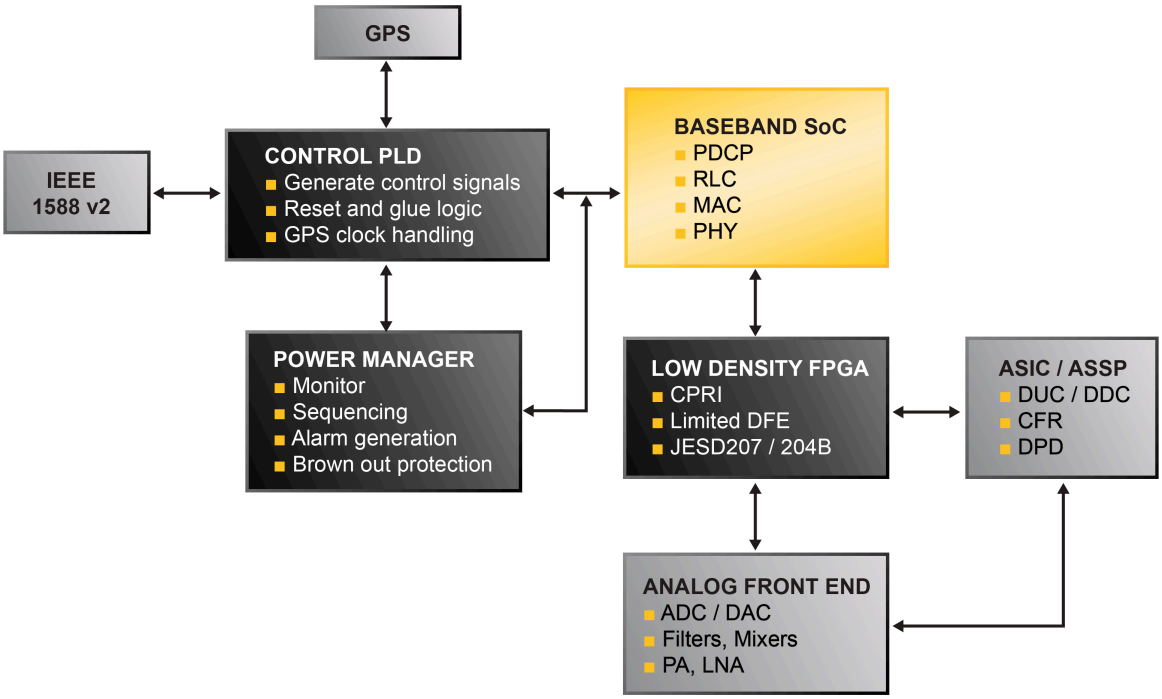

Fig.2: Block diagram of typical functional blocks in a Pico/Metro cell. (Courtesy Lattice Semiconductor)

Metro cells have transmit power levels of ~5-10 W and typically require a full DFE solution including power amplifier (PA) linearization techniques such as digital pre-distortion (DPD). From a cost and power consumption stand point, it makes sense to harden the computationally intensive data path functions (DUC/DDC/CFR/DPD) in an ASIC/ASSP, while retaining the programmable connectivity functions (CPRI, JESD204B, LVDS etc.) in a low density SERDES-enhanced FPGA.

In any of these LPN products, FPGAs with SERDES capabilities can be used to implement data path bridging and interfacing and the packet-based network interfaces (GbE, 10GbE/XAUI, XGMII) commonly used to connect small-cell clusters with the backhaul infrastructure. They can also be used to implement the XGMII interface and most of the digital functionality in smart SFP (small form-factor pluggable) transceiver products, commonly used in broadband access equipment.

Outside of communications, these devices offer low cost, low power PCI Express side-band connectivity for micro-servers. For industrial video cameras, SERDES-Enhanced FPGAs can be used to implement the entire image processing functionality in a device that consumes under 2 W.

Overview of the ECP5 SERDES Transceiver

Like most SERDES-Enhanced FPGAs on the market today, Lattice Semiconductor's ECP5™ FPGA family uses embedded SERDES transceivers which provide the baseline functionality required to support most commonly-used high-speed serial interfaces. The ECP5 series includes devices with varying amounts of programmable logic elements (up to 85k LUTs) and up to four transceivers. The transceivers are implemented as pairs within a Dual Channel Unit (DCU) containing a single shared reference clock input and Tx PLL. Each SERDES channel can be configured independently to perform high-speed, full-duplex serial data transfers at data rates from 270 Mbps to 3.2 Gbps (Fig.3).

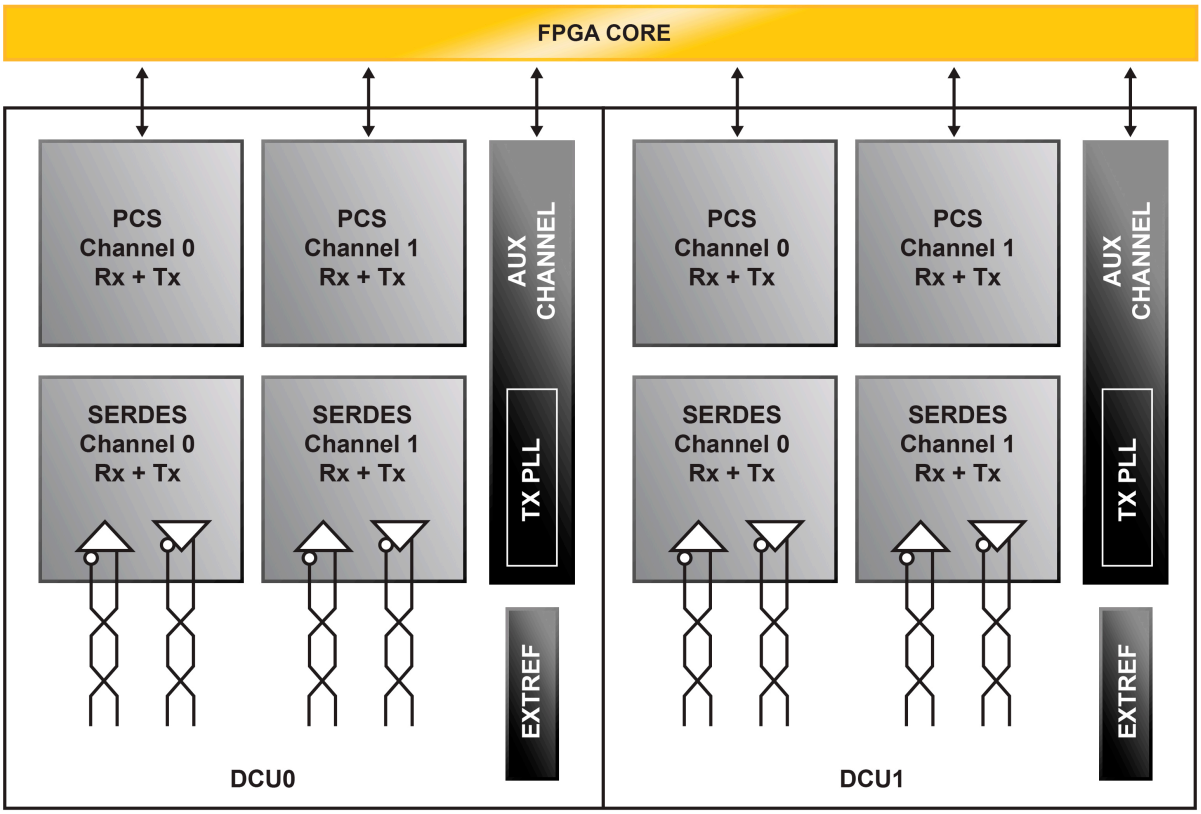

Fig.3: Block diagram of the dual-channel SERDES element used in the ECP5 FPGA series. (Courtesy of Lattice Semiconductor)

The Physical Coding Sublayer (PCS) logic in each channel can be configured to support several types of Ethernet interfaces and several other common networking and system interconnect standards. Since transceiver power consumption varies according to how it is configured and which features are used, no single number could be considered accurate. But, as a first-order approximation, it's safe to say that in most simple configurations, a single channel 3.25 Gpbs SERDES consumes less than 0.25 W. Quad-channel SERDES elements which support similar functions often consume under 0.5 W. Different combinations of protocols within a DCU are permitted subject to certain conditions as specified in the ECP5 SERDES Usage Guide[1].

Soft IP can be used in conjunction with the SERDES channels to support protocol level function for high-speed serial data links such as PCIe, CPRI, SD-SDI, HD-SDI and 3G-SDI. For custom applications, the user can use his own protocol level logic, giving users full flexibility to design their own high-speed data interface. The PCS also provides bypass modes that allow a direct 8-bit or 10-bit interface from the SERDES to the FPGA logic, allowing user to implementing his own data coding. (Fig.4).

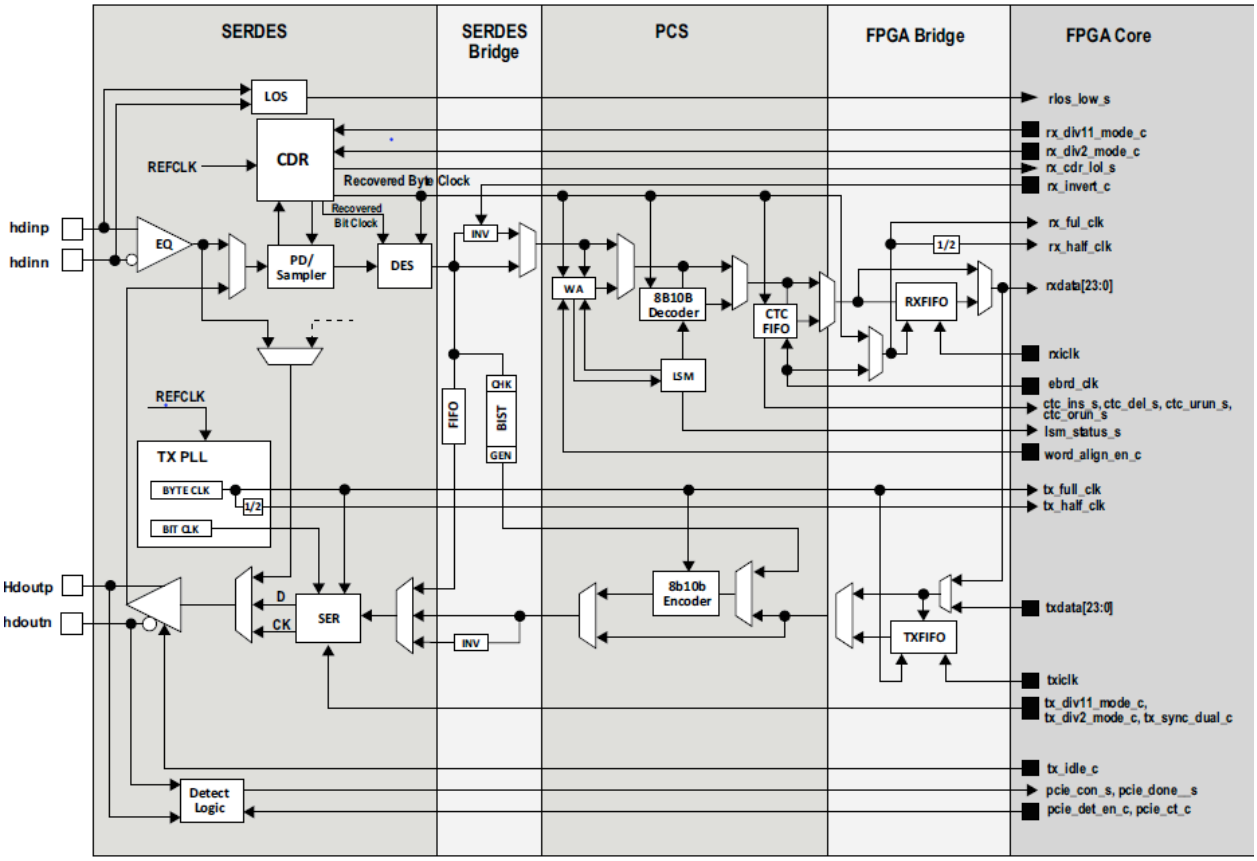

Fig.4: A detailed block diagram of a LFE5UM's SERDES/PCS channel.

Equalization

In order to compensate for the inter-symbol interference (ISI), attenuation, reflection, and other phenomena which SERDES signals encounter as they traverse printed circuit boards or cables, the transceiver uses a combination of transmitter and receiver equalization techniques which can be programmed via the device's configuration

registers. The transmitter's high speed line driver has adjustable amplitude settings and termination resistance values which can be optimized for attenuation due to the length of the channel, and adjusting termination resistance to match the channel trace impedance to minimize signal reflection. It can also perform transmit equalization using adjustable pre/post-cursor de-emphasis settings which reduces inter-symbol interference (ISI) caused by interactions between the bit being transmitted and the energy from the previously-transmitted bit still present in the transmission line.

The receiver includes a linear equalizer (LEQ) which is used to selectively amplify the frequency components in the data rate range which tend to be more heavily attenuated more over long runs across a PCB or backplane. Compensating for this frequency-dependent attenuation helps mitigate the inter-symbol Interference (ISI) which would otherwise occur in the receive signal. The receiver offers four levels of equalization which can be selected according to each channel's transmission characteristics.

Operating Modes

The SERDES transceivers in most modern FPGAs include Physical Coding Sublayer (PCS) logic which can support several application-specific protocols.

- **Generic 8b10b Mode:** This mode of the SERDES/PCS block is intended for applications requiring 8b10b encoding/decoding without the need for additional protocol-specific data manipulation at speeds of up to 3.2 Gbps. In this mode, the transceiver maintains synchronization using 8b10b encoded comma characters periodically embedded within the serial data stream.
- **Gigabit Ethernet and SGMII Modes:** These modes establish a data path between the Serial I/O interface and the GMII/SGMII interface of the IEEE 802.3-2002 1000 BASE-X Gigabit Ethernet standard. The PCS IP core includes a Gigabit Ethernet state machine which handles most of the GbE protocol but must implement the auto-negotiation function using a portion of the FPGA's logic elements.

- **XAUI Mode** – A XAUI link state machine within the SERDES/PCS block supports full compatibility from Serial I/O to the XGMII interface of the IEEE 802.3-2002 XAUI standard for 10 Gigabit Ethernet.
- **PCI Express 1.1 (2.5 Gpbs) Mode** – This mode makes use of the PCS block's IEEE 802.3ae-2002-compliant Link Synchronization State Machine (LSSM). It can control up to four SERDES channels, enabling support for x1, x2, and x4 PCI Express applications. The transceiver supports transmitting Electrical Idle, detecting Electrical Idle, and perform Receiver Detect function that are used for LSSM linkup.
- **Serial RapidIO (SRIO) mode** –Supports 1x and 4x Serial RapidIO applications at data rates of 3.125 Gbps, 2.5 Gbps and 1.25 Gbps.
- **Other Modes** – The SERDES/PCS block also includes provisions for supporting several other important serial interfaces including; Common Public Radio Interface (CPRI), all three SDI (SMPTE) modes (SD-SDI, HD-SDI and 3G-SDI0), and Serial Digital Video.

Design Issues

Many of the challenges of using SERDES-enhanced FPGAs arise from the characteristics of the Ball Grid Array (BGA) packages frequently used in the space-constrained applications where many of these devices are used. Although the guidelines presented here were developed for the high pin count and fine pitch of the ECP5 family's packages, the problems and tips for avoiding them presented here apply to any SERDES-based device using a BGA package as well as non-BGA options (such as TQFP, QFN) with high contact density.

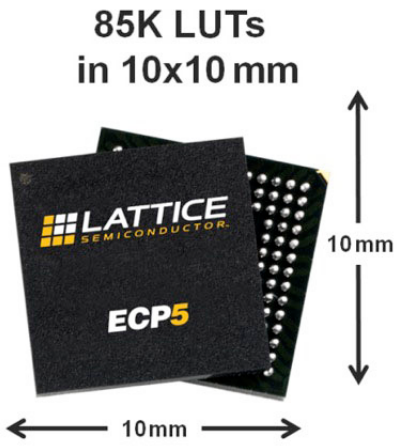

Fig.5: The fine pitch contact geometries of modern BGA packages pose special design and PCB layout challenges for high-speed SERDES channels.

A key challenge in adopting fine-pitch (0.8 mm or less) BGA packages is the design of a route fanout pattern that maximizes I/O utilization while minimizing fabrication cost. At these contact densities, it becomes difficult to route traces out from inner balls without additional PCB routing layer, or sacrifices some balls. In addition, high-speed signals, such as SERDES or DDR3/LPDDR3 signals, require even closer attention to maintaining a uniform gap for controlling trace impedance, and matching lengths between paired traces for group of signals on Source Synchronous bus, insuring provisions for a proper ground plane and isolation layers in the PC board and other issues which maintain signal integrity.

Fine pitch packages offer advantages and disadvantages alike. Finer pitch means that the trace and space limits will have to be adjusted down to match the BGA. Many times a design can get away with small traces underneath the BGA then fan out with a slightly larger trace width. The PCB fabrication facility will need to be aware of your design objectives and check for the smallest trace dimensions supported. Smaller traces take more time to inspect, check and align etc. Etching needs to be closely monitored when trace and space rules reach their lower limit. The combination of fanout traces, escape vias, and escape traces that allow routing out from under the BGA pin array to the perimeter of the device are collectively referred to as the “BGA breakout” (Fig.6). The

fanout pattern will arrange the breakout via, layer, and stack-up to maximize the number of I/Os that can be routed[2].

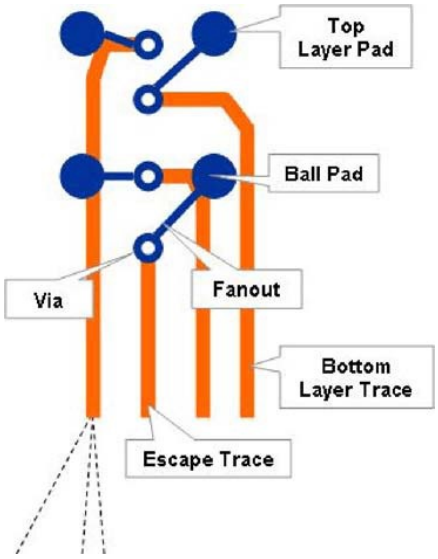

Fig.6: BGA breakout routing features

Example: Breakout and Routing for a 285-ball csfBGA BGA

The example presented in Fig.7 is an ECP5 FPGA in a 10x10 mm, 0.5 mm pitch, 285-ball csfBGA package (LFE5UM-25F-MG285) placed in a 4-layer PCB stack up with maximum I/O utilization. It utilizes 4-mil traces and 4-mil via drills for BGA escape routing. Two internal layers are used as reference planes. Blind and buried vias are not necessary in this example, which would reduce the cost.

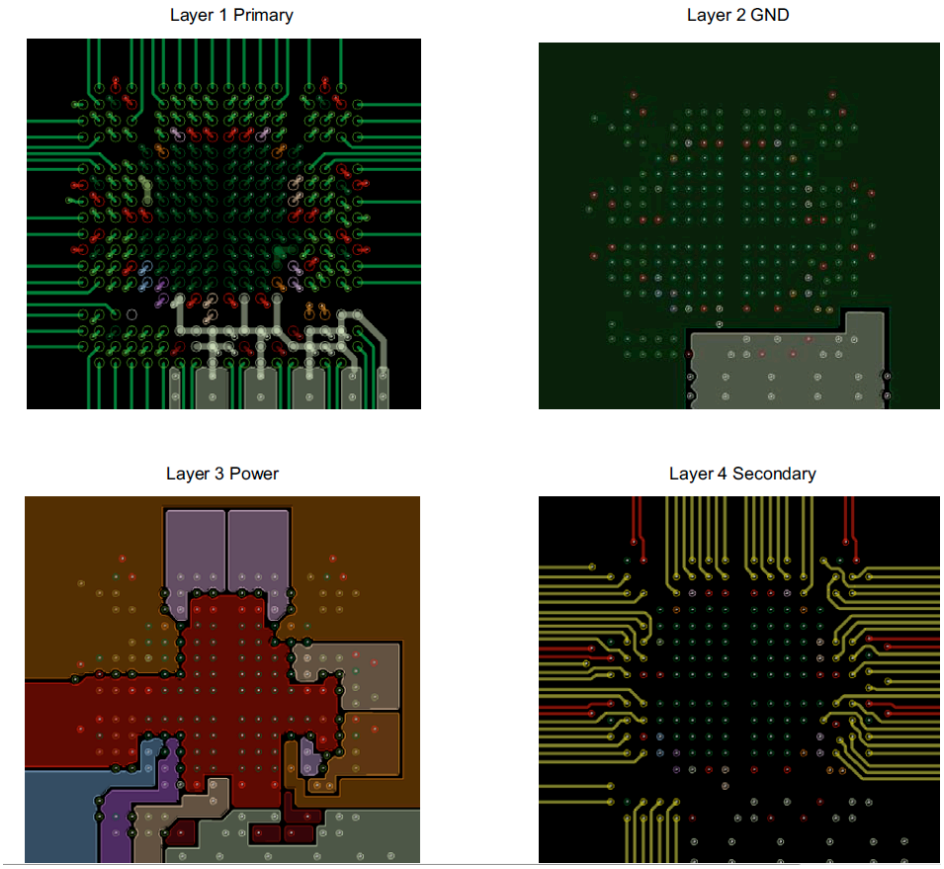

Fig.7: Screen shots of CAM artwork for a 4-layer PCB for a 285-ball csfBGA. From Lattice TN 1074 "PCB Layout Recommendations for BGA Packages"[2] (Courtesy Lattice Semiconductor)

As we've demonstrated, many signal integrity and routing issues can be mitigated with careful PCB board layout. But as contact counts increase, it becomes difficult to route traces out from inner balls without additional PCB routing layer, or sacrificing some balls**.** At the 0.8 mm ball pitch used in the ECP5's caBGA packaging, ball assignments without paying special considerations may make this difficult or impossible to make large improvements.

To address this issue, Lattice created a package design for the caBGA554 and caBGA756 form factors in 0.8mm ball pitch with a new package ball break-out scheme which allows traces to be brought from inner row balls. The package design also selectively "depopulates" unneeded ball positions to open up real estate for easier routing. In addition, careful assignment of signal/power/ground balls provides better

skew matching, lower cross-talk among busses of high-speed signals, as well as power/ground ball assignment that allows under the DUT, low inductive decoupling capacitors for supply pins.

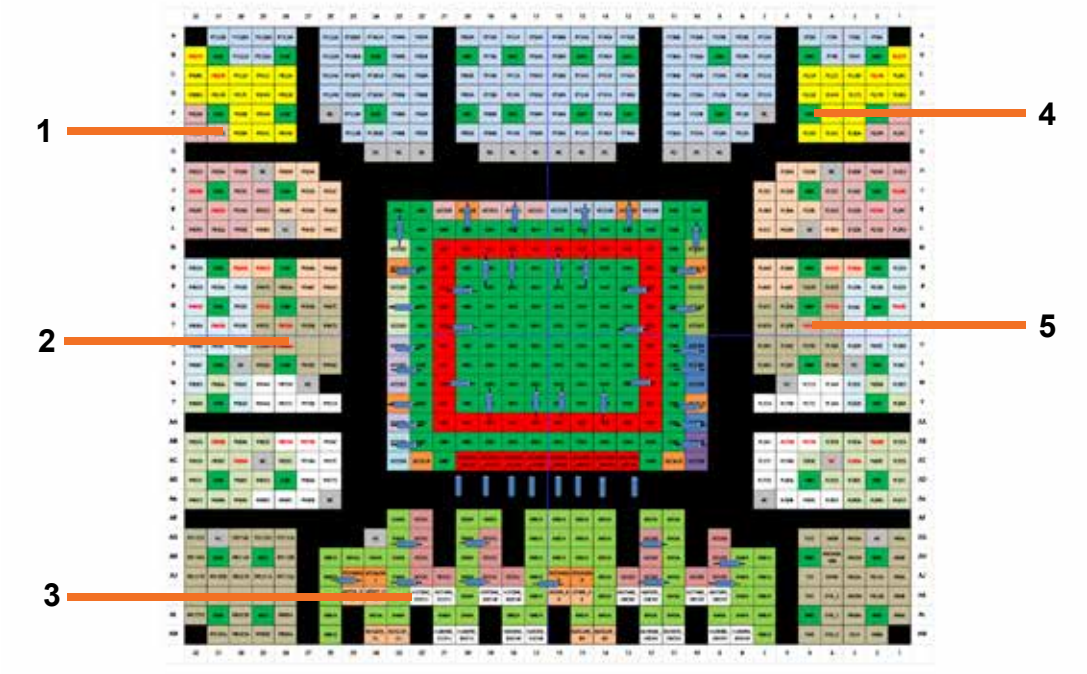

Fig.8: Ball Map of an improved caBGA756 package – annotated to highlight new features which improve trace routing and signal integrity.

The ball diagram shown in Fig.8 illustrates several of the features introduced in this new packaging system to improve board PCB trace routability, high speed & SERDES signal integrity, and power ground at-pin decoupling:

1. Strategic portions of the package's balls have been "de-populated" to create open channels for PCB trace routing.
2. The package's Power/Ground ball assignment provides enough space for a maximum-sized low L de-coupling cap under the DUT
3. All SERDES signal and power pins are well isolated from other signal pins to reduce cross-talk.

4. The package makes liberal use of distributed GNDs to insure short current return paths and minimize current induced noise on I/O pins.
5. DQS pair pins are assigned next to distributed GNDs to further minimize noise on these pins.

Although this generation of SERDES-Enhanced FPGAs has achieved significant reductions in power consumption, cooling can still be an issue, especially in products which are routinely deployed in outdoor environments. For this reason, the new packaging design also maximizes the number of ground vias located in close proximity to the FPGA chip itself to provide maximum conductive heat dissipation to the PCB under device.

The example board shown in the top image in Fig.9 illustrates a design which takes full advantage of the benefits of ball de-population while using only 2 signal PCB layers (even with thru-hole vias).

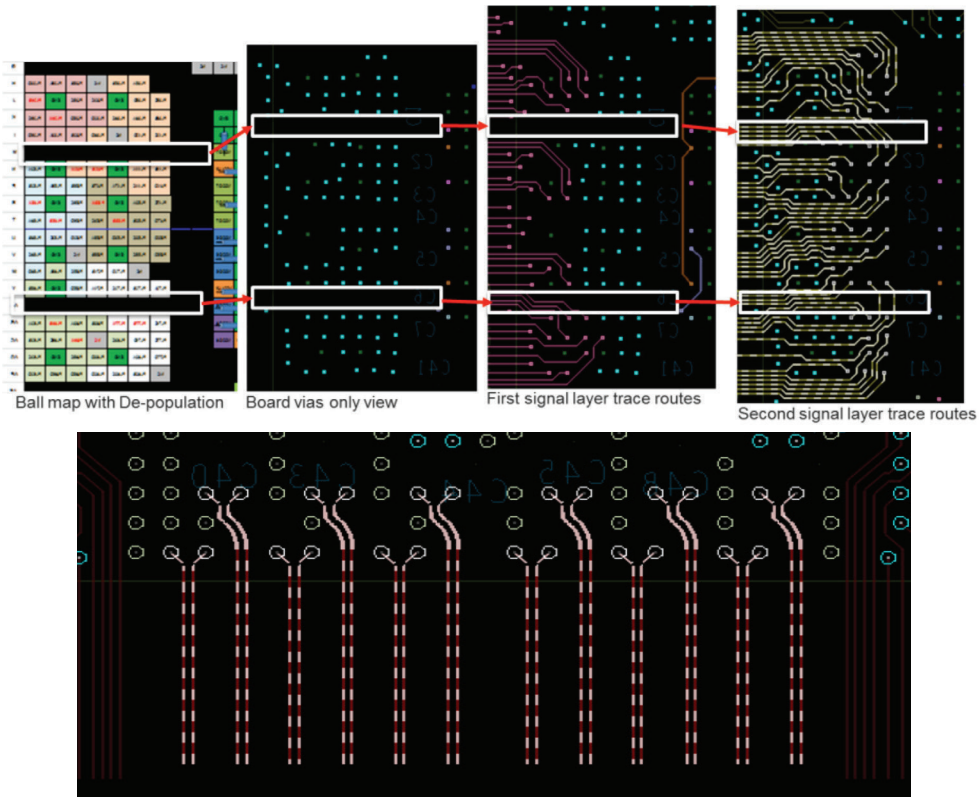

Fig.9: Top - Depopulation of BGA balls enables simpler, cleaner trace routing using fewer PCB layers. Bottom - Unobstructed routing of SERDES signal traces allows greater

Top image of Fig.10 shows when a row of balls on the package is de-populated, it removes vias that are needed for those balls. This creates unobstructed area on both signal routing layers. This offers more flexibility on the signal routes to break out to the edge of the package (left edge of the image in Fig.10).

Of greater interest however, is the routing for the SERDES signals. The image at the bottom of Fig.10 shows how the de-population of selected groups of balls enables unobstructed routing of the FPGA's high speed SERDES signals. Each pair of SERDES signal traces is closely matched in terms of length and maintains accurate trace-to-trace spacing to insure stringent control over impedance. Spacing for pair to pair, and pair to FPGA signals, is also closely controlled to minimize cross talk.

Summary

By combining programmable logic with high-speed serial data transceivers, SERDES enhanced FPGAs can support a wide range of networking and system interfaces while providing programmable logic elements which can supplement, and in some cases, eliminate ASICs and ASSPs used in conventional designs. Their programmable capabilities help enable rapid development cycles and make it possible to create easily-upgradeable products and configurable platforms which can support multiple networking and communication standards.

As with any SERDES device, they also bring several challenges to the design process, mainly in the area of packaging, PCB layout, and signal integrity. But a combination of good design practices and new packaging technologies can be used to insure SERDES-Enhanced FPGAs are able to achieve their full potential and deliver all the advantages we've discussed here when you use them in your next project.

References

[1] TN1261 - ECP5 SERDES/PCS Usage Guide

[2] TN1074 - PCB Layout Recommendations for BGA Packages

[3] Lattice provides BGA breakout and routing examples for various fine pitch packages. Details are available at the Lattice Support Center

[4] DS1044 - ECP5™ Family Data Sheet