

Introduction

High performance systems require precise power supplies to compensate for manufacturing and environmental variations. Voltage Identification (VID) is a technique to correct and adjust the power supply voltage using digital control bits.

Platform Manager™ 2 provides VID functionality that enables the user to dynamically select the desired output of a DC-DC converter or linear regulator by specifying a digital identification code.

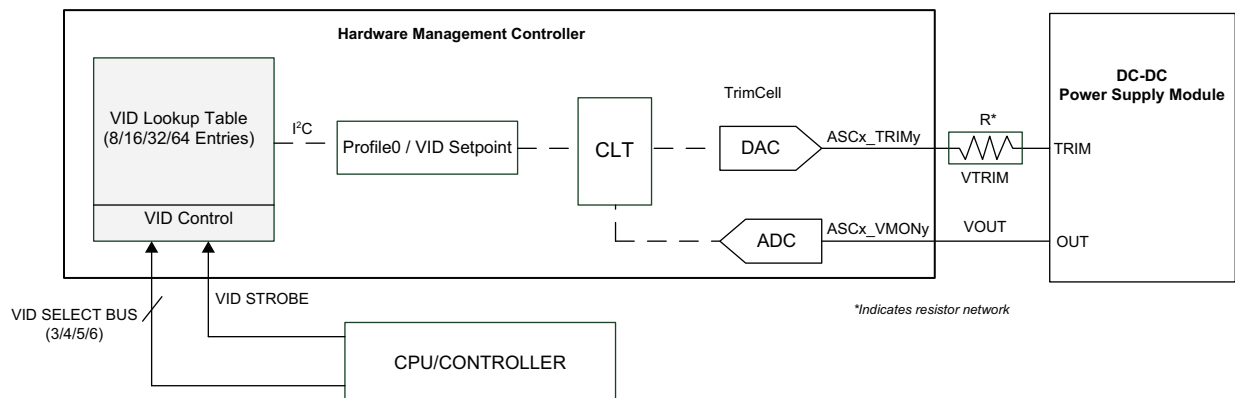
Lattice Diamond® software includes the Platform Designer tool which is used to configure the Platform Manager 2 VID function. The tool has user friendly utilities to create VID tables (target voltage settings), assign VID codes and control signals.

This document describes the built-in hardware and the software support for implementing the VID function with Hardware Management Controllers based on Platform Manager 2 designs. Platform Manager 2 designs can be built using the following Lattice devices; LPTM21 alone or with L-ASC10™(s), MachXO2™ with L-ASC10(s), MachXO3™ with L-ASC10(s), or ECP5™ with L-ASC10(s). The L-ASC10 is a hardware management expander and up to eight of them can be included in a single Platform Manager 2 design. The LPTM21 device has a single L-ASC10 device built in.

Overview-VID Control Mechanism

A typical arrangement of a DC-to-DC converter being controlled through the VID function of Hardware Management Controller is shown in Figure 1.

Figure 1. DC-DC Converter Control Through VID



For the VID operation, the output voltage (VOUT) of the DC-DC converter is adjusted by supplying trimming voltage (VTRIM) at its TRIM input pin. As shown in Figure 1, the DC-DC converter is connected by a resistor network to the Hardware Management Controller. The DC-DC output is monitored on ASCx_VMONy input and DC-DC Trim input is controlled by ASCx_TRIMy DAC output from the L-ASC10 of Hardware Management Controller. The VID control function (which resides within the FPGA) communicates over I²C with the TrimCell hardware inside the L-ASC10 device. The TrimCell has a VID Setpoint register, Closed Loop Trim circuit (CLT) and DAC output which provides VTRIM to the DC-DC converter. An external CPU or controller is typically used to select the desired DC-DC output voltage by providing the VID control function with a digital code.

After establishing the hardware connection, the following is the sequence of action for the VID operation:

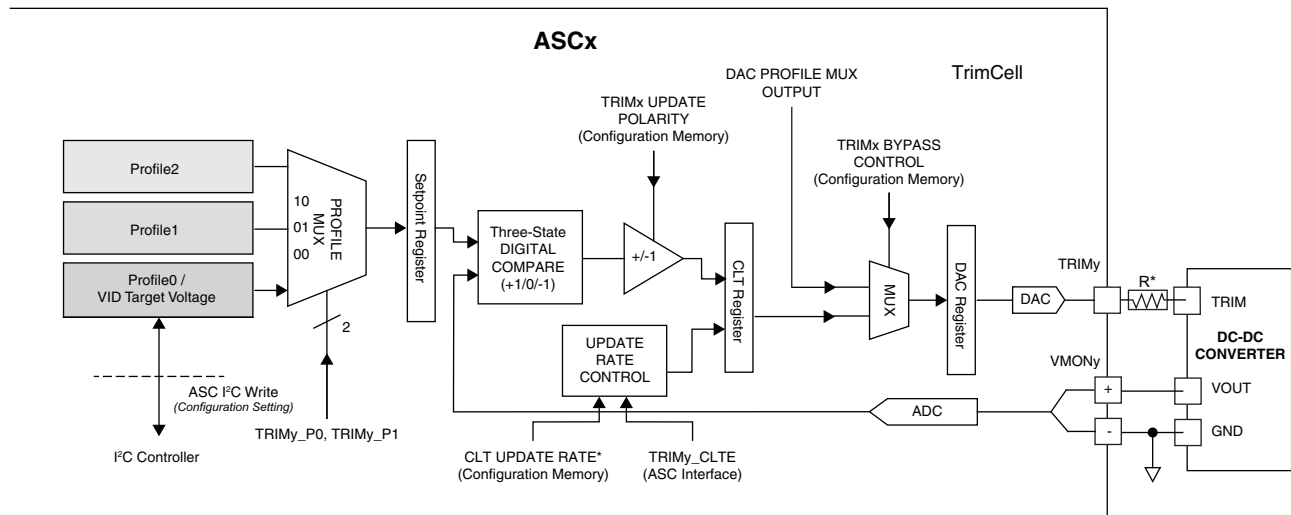
1. The Platform Designer tool is used to configure and connect the VID module and create a VID Lookup Table, which is a set of target voltages for the power supply module.
2. The CPU/Controller provides the Voltage Identification Code (VID) on the VID select bus. The VID code is decoded by the VID module and determines the target voltage from the VID Lookup Table.
3. The CPU/Controller also provides a VID Strobe signal. The VID strobe signal loads the selected target voltage from the table to the VID setpoint register inside TrimCell.
4. The VOUT of the power supply module is read by CLT logic circuit after ADC conversion. The CLT logic compares resultant ADC value with the VID Setpoint and adjusts the 8-bit DAC output, which provides the trimming voltage required to set the output voltage.
5. The CLT continuously monitors the VOUT and adjusts the VTRIM so that the VOUT equals the VID target voltage.

Another VID target Setpoint voltage from the VID Lookup Table can be selected by the CPU/Controller after changing VID code and providing VID strobe signal. The CLT repeats the action of comparing and adjusts the DAC for this new VID target voltage output. The TrimCell which provides the trimming voltage for the VID operation is explained in next section.

TrimCell

The block diagram of a TrimCell inside an L-ASC10 which implements the VID function is shown in Figure 2.

Figure 2. TrimCell Internal Block Diagram



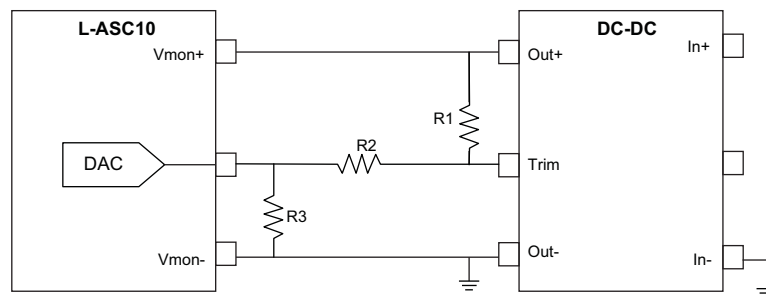
Each TrimCell consists of a programmable Voltage Setpoint Register, closed loop trim control logic and one DAC at the output. Profile0, Profile1 and Profile2 are 12-bit setpoints, which are written in the EEPROM memory during programming. The active profile for each TrimCell is independently chosen based on profile select signals TRIMy_P0 / TRIMy_P1. The closed Loop Trim Logic controls the DAC which provides the analog voltage output at the TRIMy pin of the device. The full scale output voltage of the 8-bit DAC is equal to bi-polar zero voltage (Vbpz) +/-320 mV, the Vbpz may be set to 0.6 V, 0.8 V, 1.0 V or 1.25 V. Each ASC has four TrimCells with outputs TRIM1, TRIM2, TRIM3 and TRIM4 available for VID operation. Thus, each L-ASC10 can support four different VID channels connected to four DC-DC converters.

The Platform Designer software tool is used to define Profile0 which also functions as the VID Setpoint. The software tool is also used to configure profile select signals TRIMy_P0 / TRIMy_P1, the closed loop trim enable TRIMy_CLTE, choose Trim configuration mode and DAC output enable TRIMy_OE signal. The VID operation uses I²C interface to overwrite the VID setpoint (Profile0) depending upon the VID code, the ASC I2C Write Feature (used by the VID module) is also configured through Platform Designer. For further details on the TrimCell refer to [L-ASC10 Data Sheet](#) and [Platform Manager 2 Data Sheet](#).

Interfacing Hardware Management Controller to DC-DC Converters

VID implementation requires interfacing the L-ASC10 of the Hardware Management controller to the DC-DC converter with a resistor network. Figure 3 shows an example resistor network between the L-ASC10 and the DC-DC converter. The values of these resistors depend on the type of DC-DC converter used and its operating voltage range.

Figure 3. Typical Interface Between L-ASC10 and a DC-DC Converter

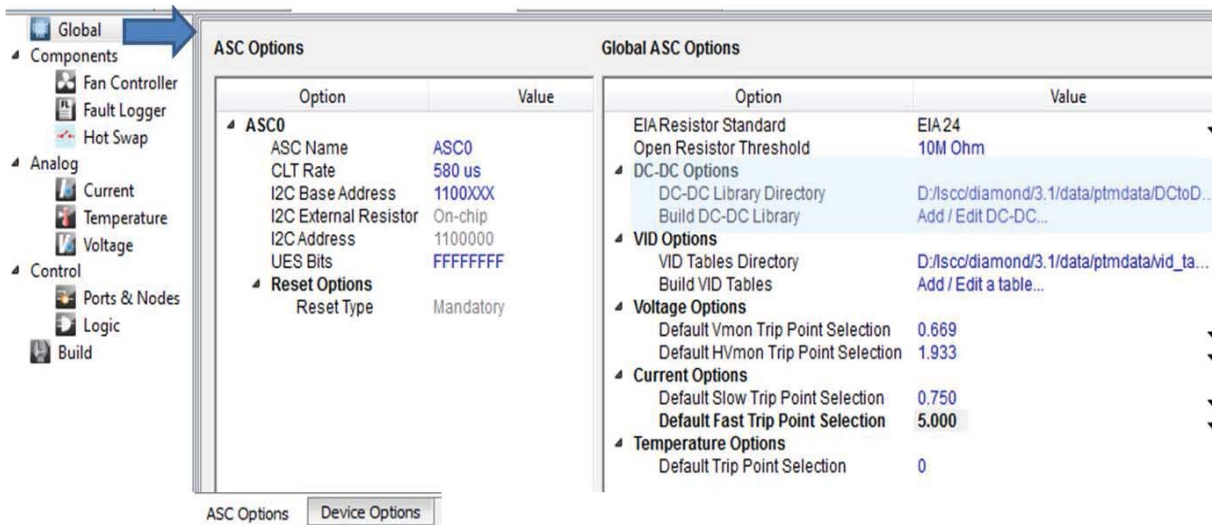


The calculation to determine the values of the resistors R1, R2, and R3 is performed automatically in the Platform Designer tool. Prior to performing the calculation, the Platform Designer tool is used first to create a DC-DC converter model and then associate the DC-DC model with the TrimCell.

This section describes interface within the Platform Designer tool to build DC-DC converter model and maintain a library for the models.

As highlighted in Figure 4, from the main window, select  **Global** view and select the ASC Options tab. On the right side, under the Global ASC Options section, select **DC-DC Options**.

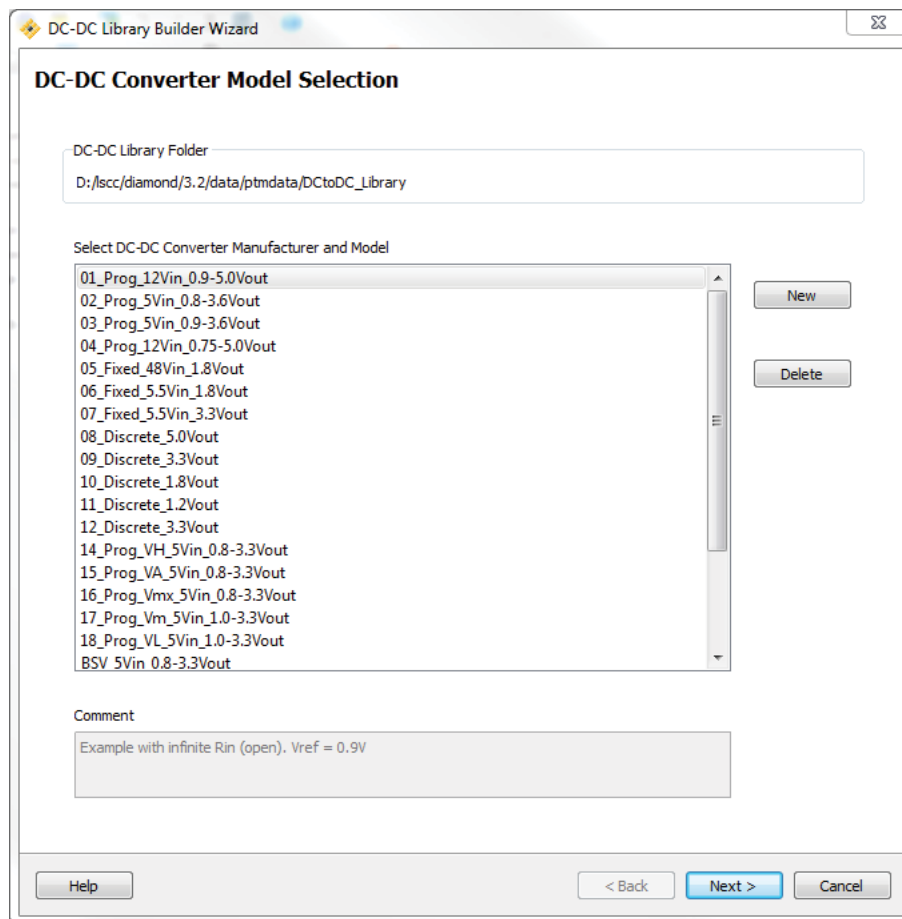
Figure 4. DC-DC Options in Platform Designer Tool



DC-DC Options provides two features:

- **DC-DC Library Directory** – This option is used to select a destination folder or directory to maintain the library of the DC-DC converter models that you create. When you click the **Value** field for this feature, you can browse to the desired location and select a destination folder to place your DC-DC converter model. The selected location is displayed along with this option as highlighted in Figure 4.
- **Build DC-DC Library** – When you click the **Value** field for this option, the DC-DC Library Builder Wizard is opened. In this window, the Select DC-DC Converter Manufacturer and Model list displays the existing DC-DC converter models in the location displayed under DC-DC Library Folder as shown in Figure 5.

Figure 5. DC-DC Library Builder Wizard



The DC-DC Library Builder Wizard provides three options regarding DC-DC models in the library: Add new, edit existing, and delete. The wizard has following buttons:

- **New** – Click to build and name a new DC-DC converter model. When this button is clicked, a new DC-DC model with a unique default name appears on the list. This default name can then be changed manually.
- **Next** – Click to edit the selected DC-DC converter model. When this button is clicked, you are given options to associate a type of DC-DC converter with the selected model.
- **Delete** – Click to delete a selected DC-DC converter model from the list.
- **Cancel** – Click to close the DC-DC Library Builder Wizard window without saving any changes made.
- **Back** – Click to view previous menu page.

The DC-DC converter model is built depending upon the type of DC-DC Power supply model used in VID application. For the complete procedure in creating a new DC-DC converter model, refer to refer to AN6074, [Interfacing the Trim Output of Power Manager II Devices to DC-DC Converters](#).

The procedure to use the DC-DC converter model for VID implementation is described in next section.

VID Implementation

VID requirements may vary depending upon application and system used. For the VID implementation using Lattice Hardware Management Controller there are six major steps to be performed using Platform Designer tool. These steps are outlined below and then covered in more detail in subsequent sections.

Step 1: Define the VID Setpoint, the target voltage output for the DC-DC converter. Select  **Voltage** view and in the Voltage tab, enter the VID Setpoint in the *Nominal Voltage (Profile0)* field.

Step 2: Use the DC-DC converter model to calculate the value of Trim Resistors. Select  **Voltage** view and in the Trim/Margin tab, perform the following tasks:

- Select a model for the DC-DC converter
- Configure the TrimCell Target Voltages to span the desired range of VID operation
- Calculate the value of Trim resistors

Step 3: For the VID application, create a table of target voltages and determine VID codes. Select  **Global** view and select the ASC Options tab. Under Global ASC Options, use VID Options to create and edit VID tables. Select  **Ports & Nodes** view to assign VID codes for the application.

Step 4: Associate VID tables, VID codes and control signals for the application. Select  **Voltage** view and open the VID tab. Apply the VID settings to activate the VID module required for the application.

Step 5: Enable the VID module to communicate using I²C for VID operation. Select  **Global** view. In the Device Options tab, select options to enable the ASC I2C Write Feature as required by the VID module.

Step 6: The complete VID operation can be controlled through user-defined code. Select  **Logic** view which provides Sequence and Supervisory Instructions to activate and control the TrimCell and VID settings for VID operation.

The Platform Designer tool provides separate windows and editors to perform the above settings and configuration. Depending upon VID implementation, the tool automatically instantiates the VID module using built-in resources (LUTs, Distributed RAM). Refer to the [Platform Designer User Guide](#) for complete information on the software tool. Specific details related to the VID utility are explained in following section.

Step 1 – Define VID Setpoint and Select VID Channel

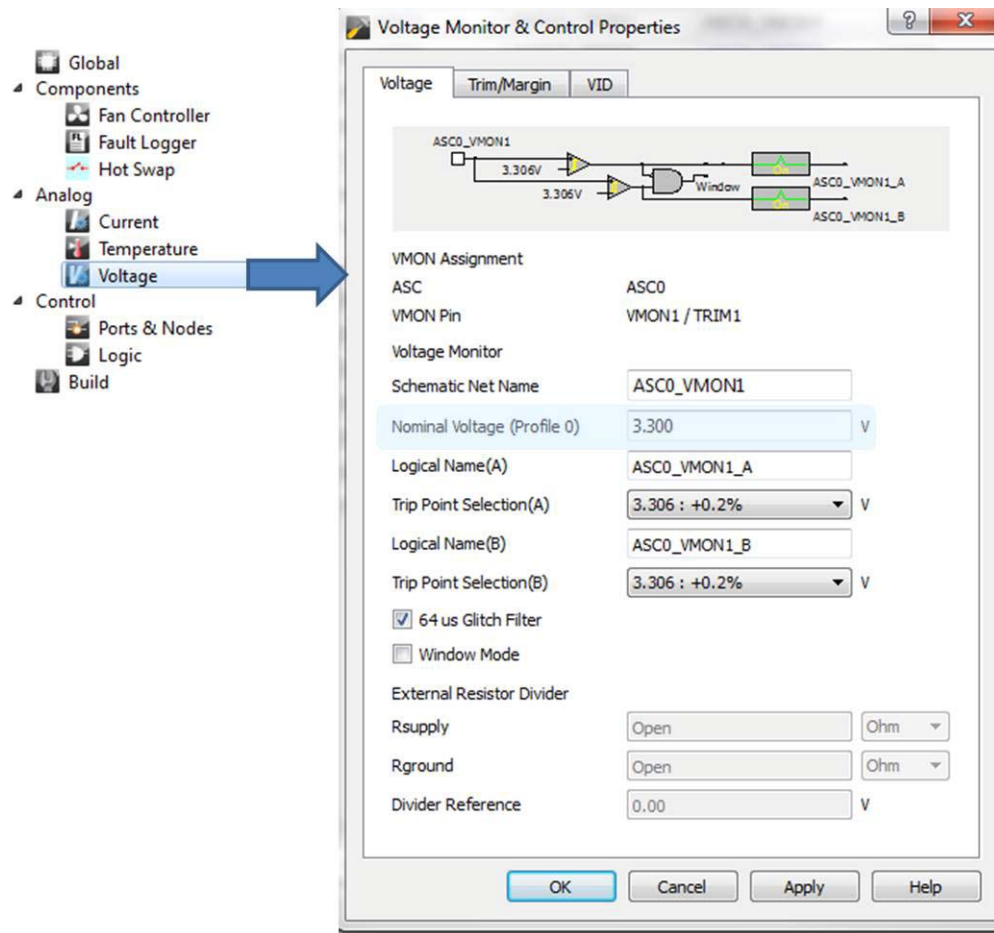
In the main window of the Platform Designer tool, select the  **Voltage** view to open a spreadsheet interface. On this interface, select the VMONy and TRIMy used for VID implementation. Double-click on the **VMONy/TRIMy** cell. This opens the Voltage Monitor & Control Properties dialog box. The selected VMONy/TRIMy are the interface pins for the VID channel in the implementation.

Defining VID Setpoint

In the Voltage tab of the Voltage Monitor & Control Properties dialog box, enter the VID Setpoint voltage in the *Nominal Voltage (Profile0)* field. This is highlighted in Figure 6.

The Profile0 is duplicated as VID Setpoint register inside the TrimCell. *Nominal Voltage (Profile0)* is the target voltage for the DC-DC converter output in close loop trim mode. The VID table should be constructed with the values close to this target voltage.

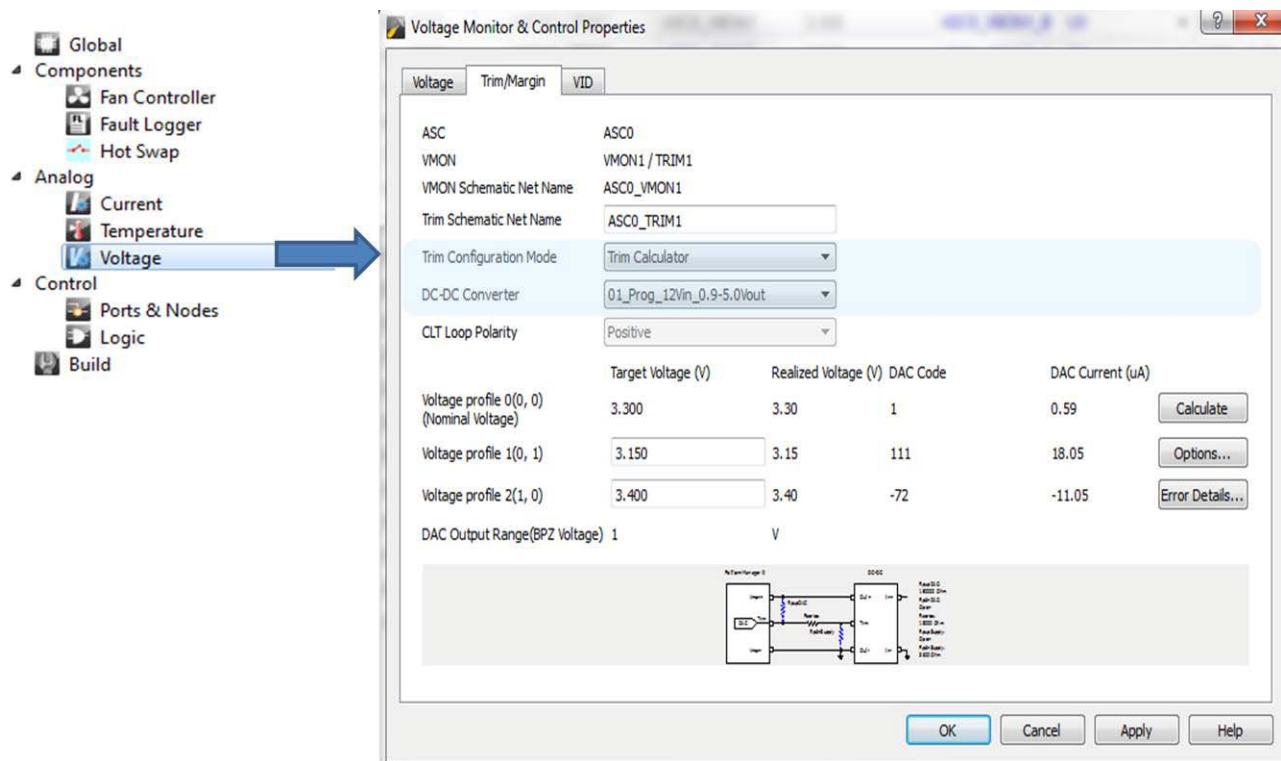
Figure 6. Define VID Setpoint (Profile0)



Step 2: Configure DC-DC Interface

The TrimCell inside ASC has a built-in DAC which provides the analog output at the TRIM pin of the DC-DC converter. Use the Trim/Margin tab in the Voltage Monitor & Control Properties dialog box to associate the DC-DC converter model, configure TrimCell and calculate trim resistors.

Figure 7. Settings for Configuring TrimCell



As highlighted in Figure 7 the Trim/Margin Tab provides the following features:

- **Trim Configuration Mode** – Provides the following two options for configuring the TrimCell operation:
 - **Manual** – Configures TrimCell for open loop operation. You are required to enter the DAC codes.
 - **Trim Calculator** – Configures TrimCell for closed loop trim. You are required to enter the Target Voltages. The DAC codes are calculated automatically by the software. For VID operation, this option should be selected.
- **DC-DC Converter** – This drop-down box provides a list of previously built DC-DC converter models. From the list, you can select the model used in VID implementation.
- **Voltage Profile0** – The Trim/Margin tab displays the VID Setpoint value (entered in Step 1) as the Target Voltage (V) for the Voltage Profile0 (Nominal Voltage). The corresponding DAC Code and DAC Current values are also shown.
- **Voltage Profile1, 2** – Enter the minimum and maximum values for Voltage Profile 1 and 2 to cover the expected range of VID operation. The software tool issues a warning message if the Voltage Profile 1 or 2 values exceed the DAC range. For the purposes of calculating the resistor interface, it does not matter which Voltage Profile contains the minimum or maximum value.
- **DAC Output Range (BPZ Voltage)** – This displays the Bi - Polar Zero (BPZ) Voltage which can be manually selected in the Options window or automatically from the **Calculate** button. Four values are supported, they are 0.6 V, 0.8 V, 1.0 V, and 1.25 V.
- **Calculate** – When you click the **Calculate** button, the Trim Resistor values are calculated and the interconnection of ASC with the DC-DC converter is displayed at the bottom of the Trim/Margin tab. Often the Trim Resistor Network can be simplified by specifying the BPZ Voltage that matches the DC-DC reference Voltage in the Options window.
- **Options** – Using the **Options** button, the Max Supply Adjustment Range can be expanded. The trim DAC has bounded range from -128 to +127 codes. By default, the Trim Calculator restricts the voltage setting ranges to +/-

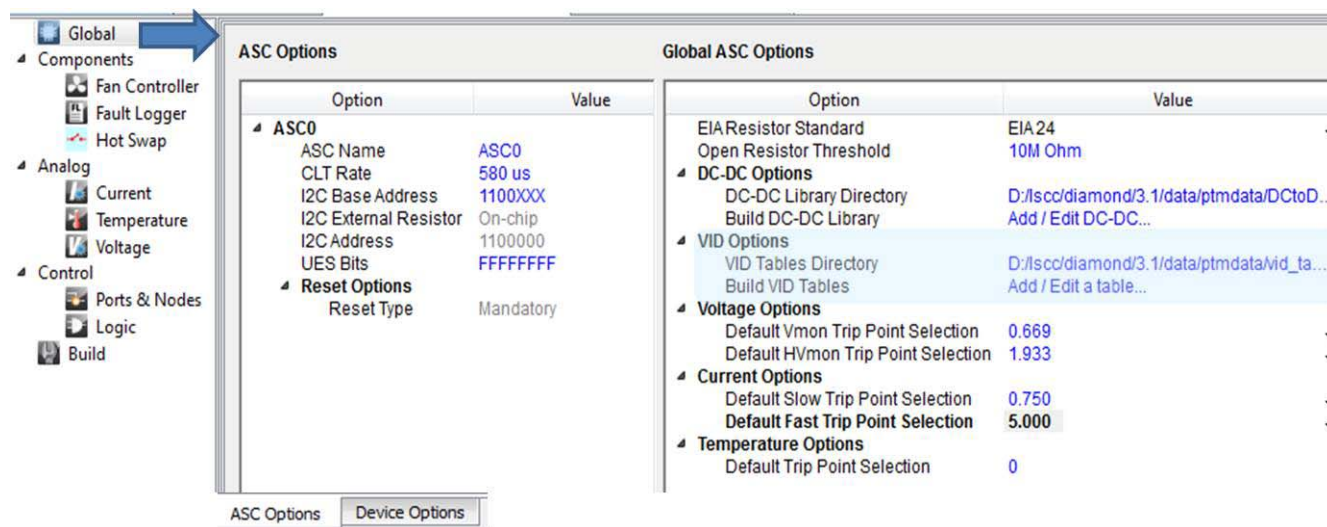
5% of the Nominal Voltage and +/- 110 DAC code.

Step 3: Create VID Tables and VID Codes

For VID operation, the target voltage output for the DC-DC converter must vary according to the VID code. A set of the desired target voltages is stored in the form of a lookup table (VID Lookup Table) in the Hardware Management Controller. The Platform Designer tool is used to create a VID table, build and maintain a library of VID tables, and select a VID table from an existing library.

To perform these tasks, select  **Global** view and select the ASC Options tab. Under Global ASC Options, set the VID Options values as highlighted in Figure 8.

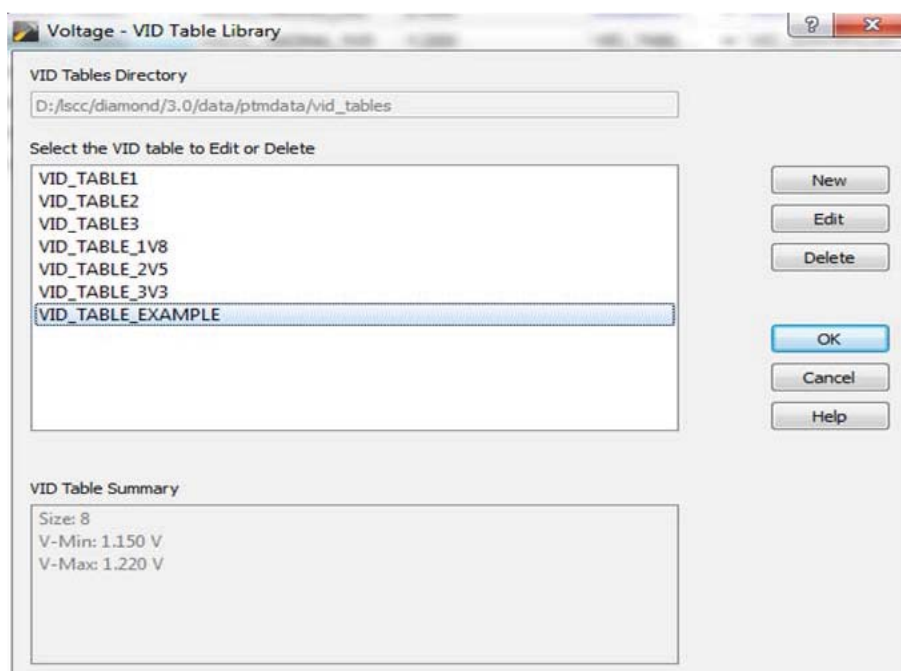
Figure 8. VID Tables and Directory



VID Options provides two features:

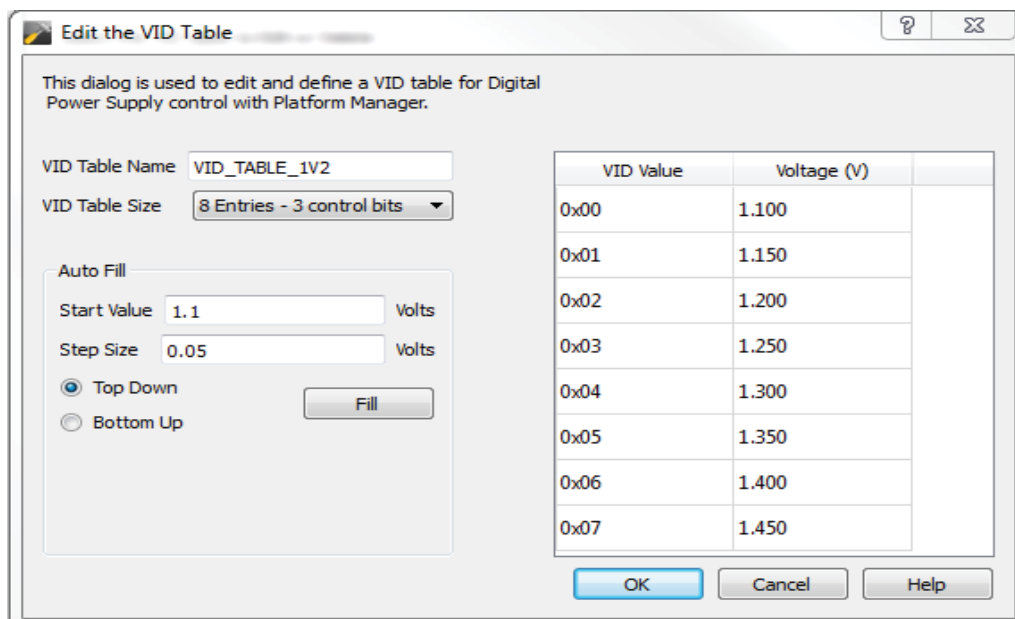
- **VID Tables Directory** – This feature is used to select a destination folder or directory to maintain repository of the created VID tables. Click the **Value** field for this feature to locate and select the folder for the VID Tables. The selected location is displayed along with this option as highlighted in Figure 8. A library of tables can be built and placed in the desired folder.
- **Build VID Tables** – Click the **Value** field for this feature to open the VID Table Library dialog box. A list of existing VID tables under VID Tables Directory is displayed. As shown in Figure 9, the dialog box provides the following options:
 - **New** – Click to create a new VID table.
 - **Edit** – Click to edit a VID table selected from the list of VID tables displayed.
 - **Delete** – Click to delete a VID table selected from the list of VID tables displayed.

Figure 9. VID Table Entry in a Library Dialog Box



When you click the **New** or **Edit** button, the VID Table dialog box opens and provides various fields for selecting and editing a VID table. A typical Edit the VID Table dialog box for editing a VID table is shown in Figure 10.

Figure 10. Edit the VID Table Dialog Box



The Edit the VID Table dialog box provides the following fields:

- **VID Table Name** – Enter a name for the created VID table. The VID table is stored under this name in the library. Each VID channel uses its own lookup table identified by the VID Table Name.
- **VID Table Size** – From the drop-down list, select the size of the VID table. The size determines the number of control bits for the VID code and the number of target voltage values.
The size of the table and corresponding control bits are selected from the drop-down list.
 - **8 Entries – 3 control bits**
 - **16 Entries – 4 control bits**
 - **32 Entries – 5 control bits**
 - **64 Entries – 6 control bits**

For example, a table with name 'VID_TABLE_1V2' having '8 Entries-3' control bits is shown in Figure 10. The table has eight rows with two columns. Each VID value and corresponding Voltage (V) is displayed on the table. For example consider sixth row of the table, if VOUT of the power supply is desired to be at 1.350 V then the 3-bit VID code should be 0x05(101).

The VID table can be edited manually or filled automatically using the Auto Fill settings.

- **Auto Fill-Start Value** – Starting value of target voltage that will be the top or bottom of the table. This value is typically the upper or lower limit of the trim range of the DC-DC used for VID application.
- **Auto Fill-Step Size** – Resolution of the voltage step. It is the difference between two consecutive target voltages.
- **Auto Fill-Top Down** – Select this option to auto-fill the table with the Start Value as the first target voltage (for lowest VID code 0x00) and add Step Size incrementally to each entry from top-down.
- **Auto Fill-Bottom Up** – Select this option to auto-fill the table with the Start Value as the last target voltage (for highest VID code) and add Step Size incrementally to each entry from bottom-up.
- **Fill** – Click the **Fill** button to fill all the table rows for Voltage (V) automatically. These values can be edited manually after the table is filled. The table in Figure 10 is filled using the settings shown.

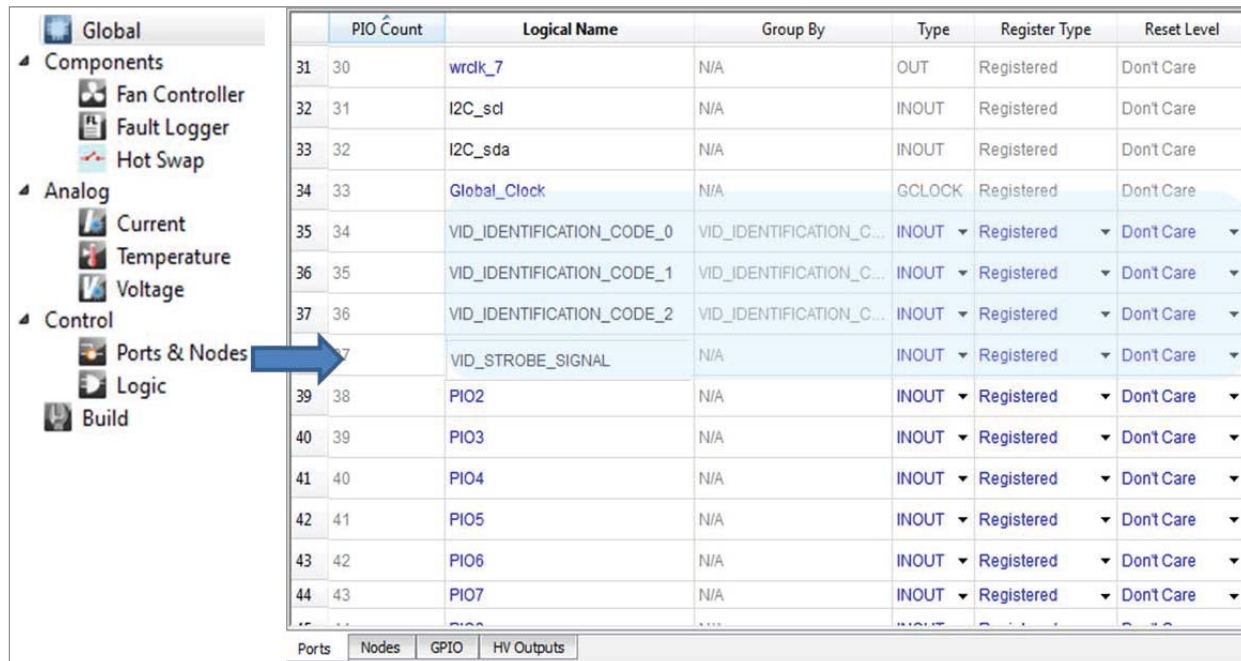
For VID operation, the VID table determines the range of the desired output voltage from the power supply module.

The target output voltage is adjusted by voltage from TrimCell DAC of the Platform Manager 2 device. The range of target values chosen in the table should not exceed the trim range of the DC-DC converter. This range is determined by the trim resistor network, the DC-DC trim behavior, and the DAC output voltage range. The Platform Designer tool issues a warning message if the VID table extends beyond the trim limits.

After constructing VID tables, the VID codes and control signals must be determined. The number of signals for the VID code depends upon the size of the table. The Platform Designer tool provides the interface to assign Ports (or internal Nodes) in Hardware Management Controller as VID codes and control signals. On the main window of the Platform Designer tool, select  **Ports & Nodes** view to open a spreadsheet interface showing the Ports tab. Right-click on this interface and select **Add Group** to assign selected ports as VID codes. The control signal assignment can be done in the cell by text entry. You can also perform a similar operation in the Nodes tab to assign internal nodes as VID code and control signals.

Figure 11 shows an example where ports of the Hardware Management Controller are assigned as a 3-bit group with the Logical Name of VID_IDENTIFICATION_CODE [2:0]. It also shows a strobe signal with the Logical Name of VID_STROBE_SIGNAL on the Ports tab.

Figure 11. VID Code and Control Signal



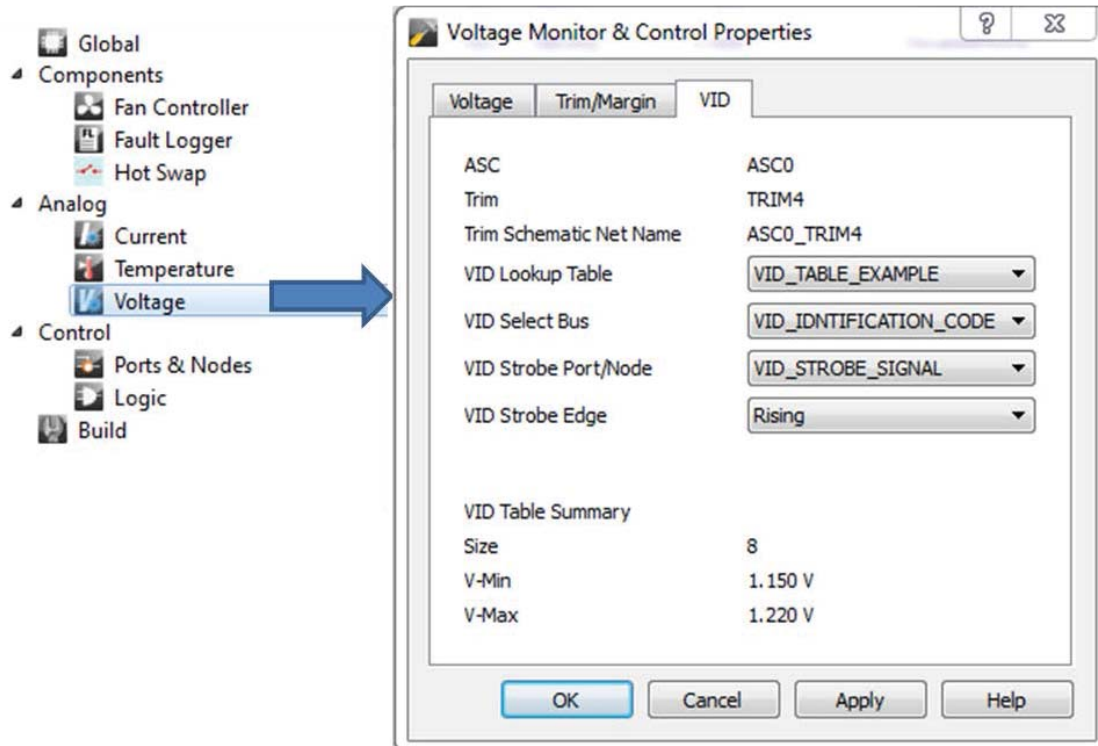
	PIO Count	Logical Name	Group By	Type	Register Type	Reset Level
31	30	wrclk_7	N/A	OUT	Registered	Don't Care
32	31	I2C_scl	N/A	INOUT	Registered	Don't Care
33	32	I2C_sda	N/A	INOUT	Registered	Don't Care
34	33	Global_Clock	N/A	GCLOCK	Registered	Don't Care
35	34	VID_IDENTIFICATION_CODE_0	VID_IDENTIFICATION_C...	INOUT	Registered	Don't Care
36	35	VID_IDENTIFICATION_CODE_1	VID_IDENTIFICATION_C...	INOUT	Registered	Don't Care
37	36	VID_IDENTIFICATION_CODE_2	VID_IDENTIFICATION_C...	INOUT	Registered	Don't Care
38	37	VID_STROBE_SIGNAL	N/A	INOUT	Registered	Don't Care
39	38	PIO2	N/A	INOUT	Registered	Don't Care
40	39	PIO3	N/A	INOUT	Registered	Don't Care
41	40	PIO4	N/A	INOUT	Registered	Don't Care
42	41	PIO5	N/A	INOUT	Registered	Don't Care
43	42	PIO6	N/A	INOUT	Registered	Don't Care
44	43	PIO7	N/A	INOUT	Registered	Don't Care

Ports Nodes GPIO HV Outputs

Step 4 - Associate VID tables, VID codes and control signal with VID channel

The Platform Designer tool provides interface to link all the VID settings completed in previous steps. In the main window, select the **Voltage** view, and open the Voltage Monitor & Control Properties by double-clicking on the ASC Device or Monitor / Trim Pin cell of associated with the VID. This dialog box has a VID tab which is used for selecting a VID Lookup Table from the library and other VID control signals, as shown in Figure 12.

Figure 12. VID Control Dialog Box



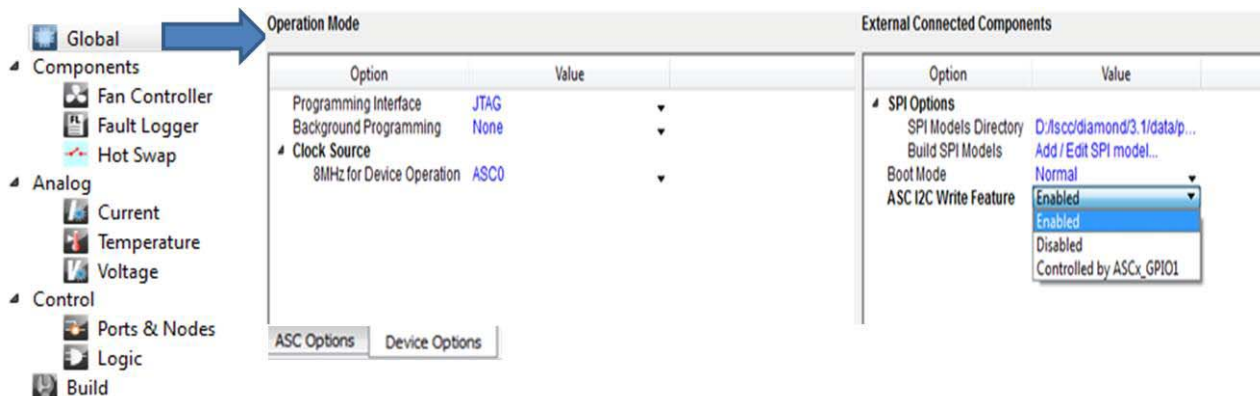
- **VID Lookup Table** – This drop-down list provides the names of existing VID tables under VID Tables Directory. By default, the VID channel is disabled. The VID channel is activated when a VID Lookup Table name is selected from the drop-down list.
- **VID Select Bus** – This drop-down list allows you to select a previously created Group. Only the groups that correspond to the correct number of control bits for the selected VID table are shown in the drop-down list. The width of the group or bus must correspond to the VID table size (3 bits for 8 values, 4 bits for 16 values, 5 bits for 32 values and 6 bits for 64 values). This bus provides the identification code to select an entry from the VID table.
- **VID Strobe Port/Node** – This drop-down list allows you to select the created strobe signal. The VID strobe signal triggers the VID module to sample the VID Select Bus and update the target voltage.
- **VID Strobe Edge** – This feature allows you to choose the edge of the VID Strobe Port/Node signal, either **Rising** or **Falling**, for triggering action.

Note: Nodes must be inserted in the Ports & Nodes view before they can be used for VID Select Bus or VID Strobe.

Step 5 - Enable ASC I2C Write Feature

The VID module uses I²C interface to update the Profile0 Setpoint and change the output at the ASCx_TRIMy pin. In the Platform Designer tool main window, select **Global** view. In the Device Options tab, set the ASC I2C Write Feature value by selecting options as highlighted in Figure 13.

Figure 13. Setting for ASC I2C Write Feature



- **ASC I2C Write Feature** – This is used to set the ASC I2C Write protection mode to one of the following:
 - **Enabled** – Select to permanently enable the I²C Write feature. Any I²C master can overwrite ASC device configuration and the VID Setpoint.
 - **Disabled** – Select to permanently disable the I²C Write feature. When this option is selected, VID does not function.
 - **Controlled by ASCx_GPIO1** – When this option is selected, the FPGA Port (External Connection) is displayed from the drop down list. Select the FPGA port which will be externally connected to the ASCx_GPIO1 port.

For VID operation, the registers inside ASC are required to be accessed by I²C. You are therefore required to select **Enabled** or **Controlled by ASCx_GPIO1**. If **Controlled by ASCx_GPIO1** is selected, the VID module automatically drives the associated FPGA port high during VID access.

Step 6 – Implement VID Control Logic

After all VID settings are completed, the VID algorithm can be implemented as required by the application. The  **Logic** view in Platform Designer tool provides an interface for implementing state machine sequences and logical equations, creating timers, and importing user HDL to a design.

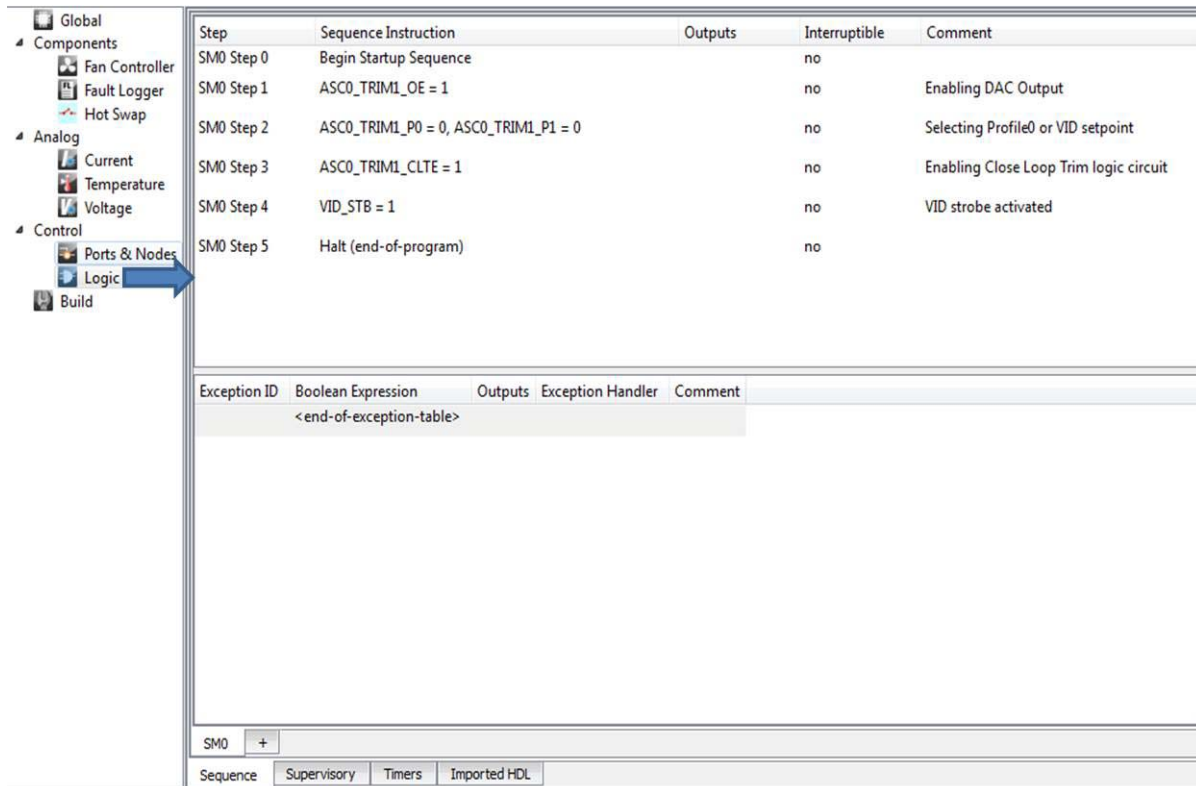
Enabling the VID

Several internal control nodes need to be driven properly to enable the closed-loop trimming of the DC-DC to the target VID setting. Those nodes are described here:

- **ASCx_Trimy_OE** – An internal node which controls the DAC of a TrimCell. When this node is driven high it the DAC output is enabled to provide voltage at TRIMx pin. The associated DAC needs to be enabled for each VID channel used.
- **ASCx_TRIMy_P0 / ASCx_TRIMy_P1** – Internal nodes which control the Profile select for the TrimCell. When both the nodes are driven low, Profile0 which has VID Setpoint is provided to the close loop trim logic.
- **ASCx_TRIMy_CLTE** – An internal node which enables the closed loop trim engine. Every TrimCell used for VID operation must have its closed trim enabled by driving this node high. When CLTE node is driven high it enables the closed loop trim engine which controls DAC output based on VID Setpoint register and VMONy feedback value.
- **VID strobe signal** – A user defined Port or Node which controls loading of VID table value in the VID Setpoint register. This signal can be configured to be active either on rising or falling edge as described in the VID settings. VID strobe signal can be activated externally (from another device on the board) or implemented using the  **Logic** view of Platform Designer tool.

The  **Logic** view with a typical sequencing instruction is shown in Figure 14.

Figure 14. Logic Editor with Sequence and Supervisory Instructions



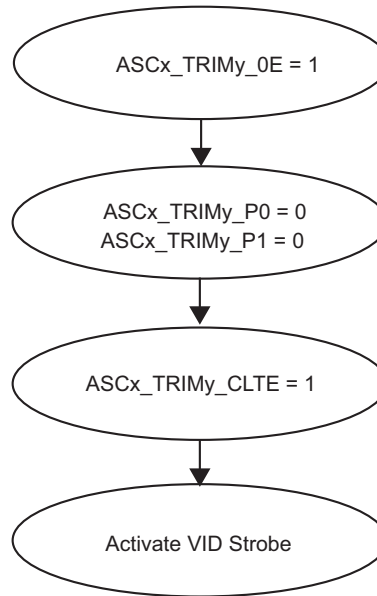
The screenshot shows the Logic Editor interface with a left-hand sidebar containing a tree view of components: Global, Components (Fan Controller, Fault Logger, Hot Swap), Analog (Current, Temperature, Voltage), and Control (Ports & Nodes, Logic, Build). The 'Logic' component is selected, indicated by a blue arrow. The main workspace displays a sequence of steps for a state machine (SM0).

Step	Sequence Instruction	Outputs	Interruptible	Comment
SM0 Step 0	Begin Startup Sequence		no	
SM0 Step 1	ASC0_TRIM1_OE = 1		no	Enabling DAC Output
SM0 Step 2	ASC0_TRIM1_P0 = 0, ASC0_TRIM1_P1 = 0		no	Selecting Profile0 or VID setpoint
SM0 Step 3	ASC0_TRIM1_CLTE = 1		no	Enabling Close Loop Trim logic circuit
SM0 Step 4	VID_STB = 1		no	VID strobe activated
SM0 Step 5	Halt (end-of-program)		no	

Below the sequence table, there is an 'Exception ID' table with columns: Exception ID, Boolean Expression, Outputs, Exception Handler, and Comment. The content is '<end-of-exception-table>'. At the bottom, there are tabs for 'Sequence', 'Supervisory', 'Timers', and 'Imported HDL', with 'Sequence' currently selected.

The user-defined Ports and built-in nodes for the TrimCell and VID controls need to be enabled for the VID operation. An example sequence in Figure 14 shows required user logic for successful VID operation. Exact implementation may have added steps or more control but the logic implementation should follow the sequence shown in the flowchart in Figure 15.

Figure 15. Basic Flowchart to Implement VID Algorithm Using Logic View



VID Channels Using Hardware Management Controller

The number of possible VID channels depends upon the specific application using Hardware Management Controller. The number of VID channels is limited by the logic resources available in a particular arrangement of the controller and possibly by other features in the design (such as fault logging, fan controllers, or hot swap components). The absolute maximum number of VID channels for any given configuration is 16. Table 1 provides the number of possible VID channels based on hardware configuration.

Table 1. Maximum Number of VID Channels Supported Based on Hardware

Hardware Configuration		Maximum Number of VID Channels
FPGA	External ASCs	
LPTM21	0	4
LPTM21	1, 2, 3	8
XO2-640 ¹	1,2	1
XO2-1200 ¹	1	4
XO2-1200 ¹	2, 3, 4	8
XO2-2000 ¹	1	4
XO2-2000 ¹	2	8
XO2-2000 ¹	3, 4, 5, 6	12
XO2-4000 ¹	1	4
XO2-4000 ¹	2	8
XO2-4000 ¹	3	12
XO2-4000 ¹	4, 5, 6, 7, 8	16
XO2-7000 ¹	1	4
XO2-7000 ¹	2	8
XO2-7000 ¹	3	12
XO2-7000 ¹	4, 5, 6, 7, 8	16
LCMXO3LF-640LF	1,2	1
LCMXO3LF-1300LF	1	4
LCMXO3LF-1300LF	2,3,4	8
LCMXO3LF-2100LF	1	4
LCMXO3LF-2100LF	2	8
LCMXO3LF-2100LF	3,4,5,6	12
LCMXO3LF-4300LF	1	4
LCMXO3LF-4300LF	2	8
LCMXO3LF-4300LF	3	12
LCMXO3LF-4300LF	4,5,6,7,8	16
LCMXO3LF-6900LF	1	4
LCMXO3LF-6900LF	2	8
LCMXO3LF-6900LF	3	12
LCMXO3LF-6900LF	4,5,6,7,8	16
LCMXO3LF-9400LF	1	4
LCMXO3LF-9400LF	2	8
LCMXO3LF-9400LF	3	12
LCMXO3LF-9400LF	4,5,6,7,8	16

Hardware Configuration		Maximum Number of VID Channels
FPGA	External ASCs	
ECP5 Family ^{2,3}	1	4
ECP5 Family ^{2,3}	2	8
ECP5 Family ^{2,3}	3	12
ECP5 Family ^{2,3}	4,5,6,7,8	16

1. Only MachXO2 types HC, HE, and UHC.

2. Only ECP5U types LFE5U-12F, LFE5U-25F, and LFE5U-45F.

3. Only ECP5UM types LFE5UM-25 and LFE5UM-45F.

Summary

The Hardware Management Controller based on Platform Manager 2 designs can provide a VID control function when the device is appropriately configured using Platform Designer software. The easy to use software tool provides options to create and maintain VID tables, VID codes and other control signals. The Platform Manager 2 design can be easily interfaced with a micro-controller or digital controller for VID operations. Platform Manager 2 designs can be built using the following Lattice devices; LPTM21 alone or with L-ASC10(s), MachXO2 with L-ASC10(s), MachXO3 with L-ASC10(s), or ECP5 with L-ASC10(s).

The VID function provided by Platform Manager 2 designs uses I²C read and write. Hence, it supports VID operations where a high rate-of-change is not required, as it can take tens of milliseconds for the VID module to slew between differing target voltages.

Related Literature

- DS1042, [L-ASC10 Data Sheet](#)
- DS1043, [Platform Manager 2 Data Sheet](#)
- [Platform Designer 3.4 User Guide](#)
- AN6074, [Interfacing the Trim Output of Power Manager II Devices to DC-DC Converters](#)

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Date	Version	Change Summary
September 2017	1.2	Added references to MachXO3 and ECP5 in the Introduction section.
		Updated the second paragraph of the Overview-VID Control Mechanism section.
		Changed “ASC” instances in various sections to “L-ASC10”.
		Added information to Calculate feature in the Step 2: Configure DC-DC Interface section.
		Added note to the Step 4 - Associate VID tables, VID codes and control signal with VID channel section.
		Updated Table 1 , Maximum Number of VID Channels Supported Based on Hardware. — Removed “HC” in MachXO2 devices and added footnote 1. — Added other devices.
		Updated Summary section.
		Updated Technical Support Assistance information.
April 2015	1.1	Removed LPTM20 reference.
August 2014	1.0	Initial release.