POWR607/6AT6 Evaluation Board

User's Guide

July 2014
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Introduction

Thank you for choosing the Lattice Semiconductor POWR607/6AT6 Evaluation Board!

This user's guide describes how to start using the POWR607/6AT6 Evaluation Board, an easy-to-use platform for evaluating and designing with the Lattice Power Manager II devices, POWR607 and POWR6AT6. The Evaluation Board has pre-loaded Processor Support demonstration design. You may also reprogram the POWR607/POWR6AT6 to review your own custom designs.

Note: Static electricity can severely shorten the lifespan of electronic components. See the POWR607/6AT6 Evaluation Board QuickSTART Guide for handling and storage tips.

Features

- POWR607/6AT6 Evaluation Board - A 3.75 by 2.00 inches form factor that features the following on-board components and circuits:
  - Power Manager II ispPAC® -POWR607
  - Power Manager II ispPAC® -POWR6AT6
  - LEDs for general purpose I/O, power indicators, and watchdog timer interrupt indication
  - Slide potentiometer
  - USB B-mini connector for power and programming
  - 2x14 expansion header for general I/O, voltage monitor inputs, and power supply trim outputs
  - Push buttons for reset and watchdog timer trigger
  - 4-bit DIP switch for watchdog timer period programming and reset pulse stretch enable
  - JTAG and I^2C header landings for JTAG cable programming and I^2C interface
- Pre-loaded Processor Support Demo - The board includes a pre-loaded demo design that demonstrates watchdog timer, voltage supervisor, and reset generation features of the POWR607.
- USB Connector Cable - The POWR607/6AT6 Evaluation Board is powered from the mini B USB socket when connected to a host PC with the included USB cable. The USB channel also provides a programming interface to the POWR607/6AT6 and POWR6AT6 JTAG ports.
- QuickSTART Guide - Provides information on connecting the POWR607/6AT6 Evaluation Board, running the pre-loaded processor support demo.
- POWR607/6AT6 Evaluation Board Web Page - Provides access to the latest documentation, demo designs, and drivers for the kit. See www.latticesemi.com/boards and look for the POWR607/6AT6 Evaluation Board.

The contents of this user's guide include demo operation, programming instructions, top-level functional descriptions of the evaluation board, descriptions of the on-board connectors, switches and a complete set of schematics of the board.

Software Requirements

You should install the following software before you begin developing designs for the board:

- PAC designer 6.25 or later
- Lattice Diamond Programmer

Figure 1. POWR607/6AT6 Evaluation Board, Top Side

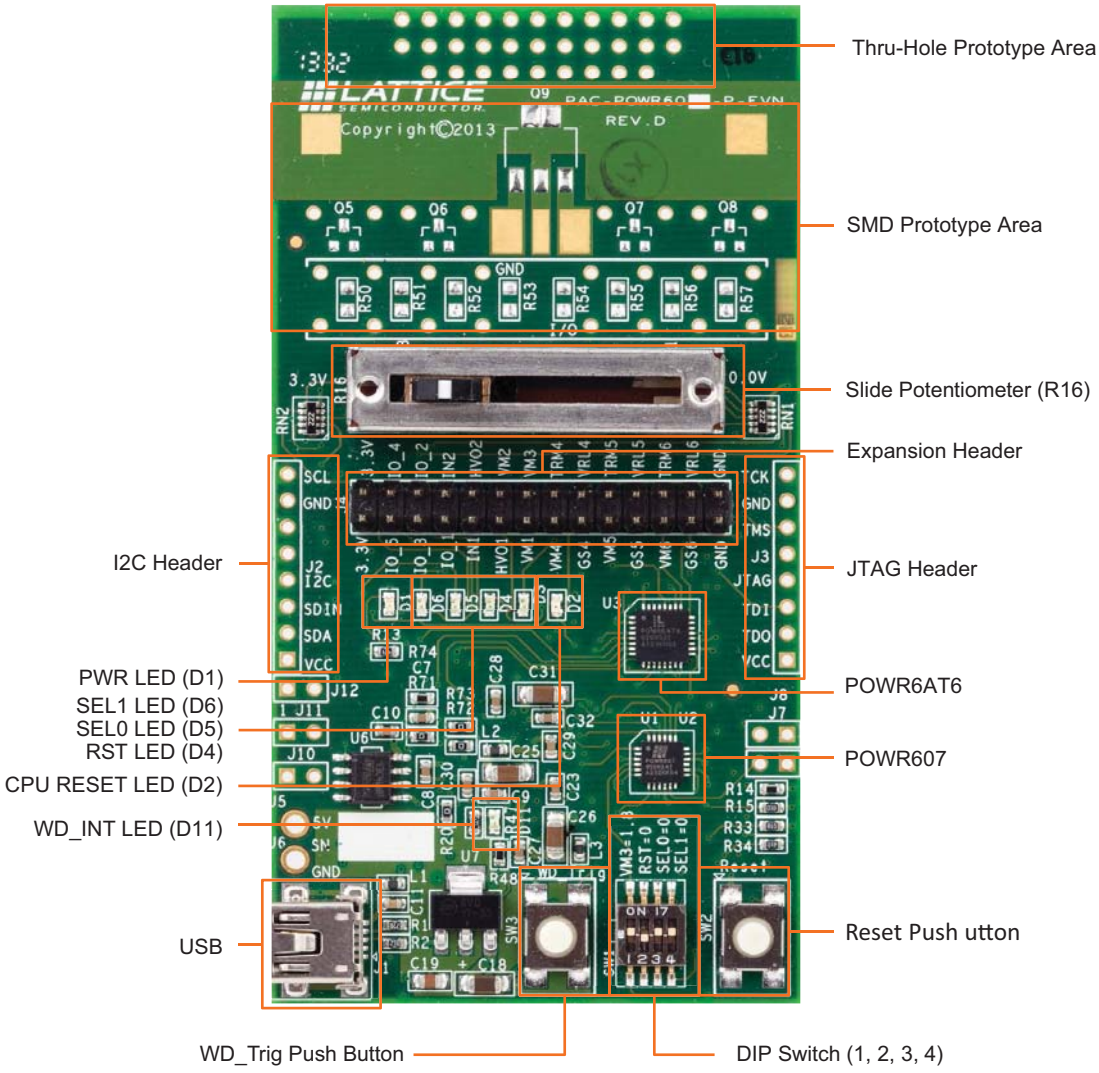
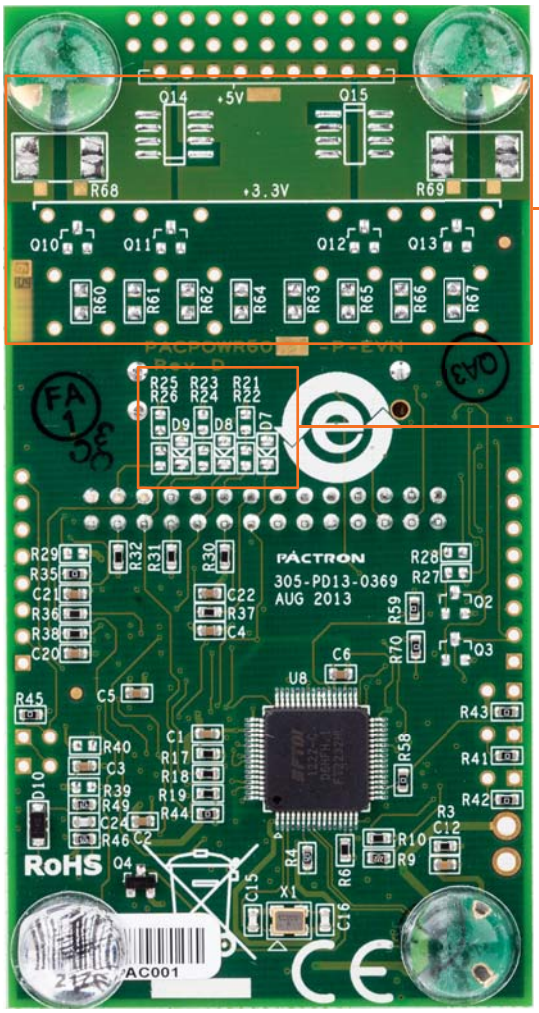


Figure 2. POWR607/6AT6 Evaluation Board, Bottom Side



POWR607 Device

This board features the POWR607, an in-system programmable, mixed-signal PLD that integrates high-performance analog voltage monitors, 4 timer counter blocks, and a 16-macrocell programmable logic device. A complete description of this device can be found in the DS1011, ispPAC-POWR607 Data Sheet.

Demonstration Designs

Lattice provides two demos that illustrate key applications of the Power Manager II devices POWR607 and POWR6AT6:

- **Processor Support** - Demonstrates the POWR607 as a power manager for a processor, DSP, ASSP, or ASIC. It integrates three functions traditionally covered by discrete ICs: voltage supervisor, reset generator, and watchdog timer. The programmable features of the POWR607 highlight its flexibility to be used in a variety of system support roles. The processor support demo design is pre-loaded into the POWR607 by Lattice.

  Note: The processor support demo program (JEDEC) differs slightly from the Initial Factory Configuration described in DS1011, ispPAC-POWR607 Data Sheet. WDT_Intr output is active-high in the demo program, and active-low in the factory configuration.

- **Voltage Monitoring** - Shows application of the ispPAC-POWR6AT6 to provide supply measurements via an I^2C interface. The voltage monitoring support demo design is pre-programmed into the POWR6AT6 by Lattice with the I^2C address of 0x6A.

  Note: It is possible that you may obtain your POWR607 board after it has been reprogrammed. To restore the factory default demo and program it with other Lattice-supplied examples see the Download Demo Designs and Download Windows Hardware Drivers sections of this document.

Processor Support Demo

The processor support demo is pre-programmed into the non-volatile elements of the POWR607 and POWR6AT6 devices and is operational upon power-up. The design provides the following features:

- Detect voltage supply violations and assert a CPU reset if a fault occurs.
- Provide a 500ms, 2 sec, 10 sec, or 1 min period watchdog timer and assert a watchdog timer interrupt if a timer expires before a watchdog trigger interrupt occurs.
- Assert CPU reset pulses if manual reset of the board occurs. Provide an optional 200ms pulse stretch of the reset.
- De-bounce manual reset input.

A PAC-Designer software project (.pac) defines the analog trip points for the POWR607 voltage monitors, timer-counter period, and supervisory equations that define logical functions.

Figure 3. Processor Support Demo Block Diagram

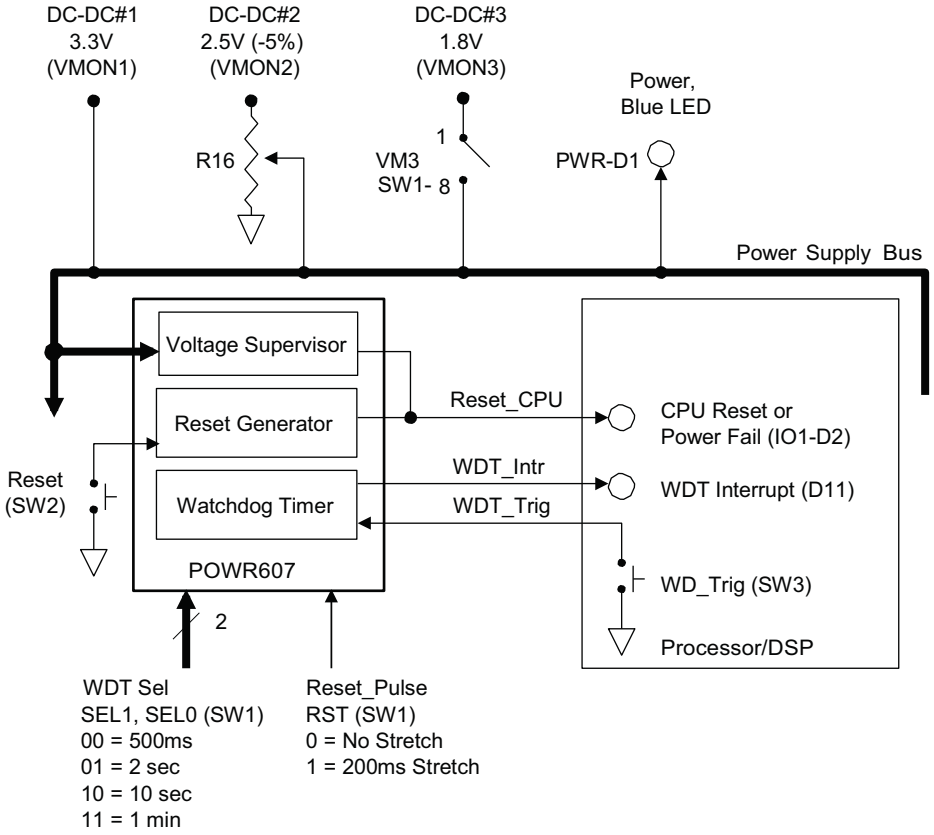


Table 1 describes the DIP switch, push-button inputs, and slide potentiometer settings that control the pre-configured POWR607 and emulate a variety of processor support scenarios. Use them as a reference as you follow the procedure. To indicate a '1' (logical True) on the DIP switch SW1, slide the switch towards the number indicated on the switch body. Note the circuit board silkscreen markings for: VM3=1.8, RST=0, SEL0=0, and SEL1=0.

Table 1. Processor Support Demo Switch and Button Settings

Setting	Function
DIP Switch (1, 2, 3, 4)	
XX00	**500ms WDT (SEL0=0, SEL1=0)** Enables a 500ms period watchdog timer (WDT). When active, the POWR607 will monitor the terminal count (TC) value a programmable timer. Once 500ms expires, the WDT_Intr output is asserted. An amber WDT_INT LED (D11) will light momentarily to indicate the WDT interrupt input to the processor/DSP is active. Once activated, you may reset the WDT by pressing the push-button switch (WD_Trig) to emulate a WDT trigger event asserted by the processor/DSP. A red LED D5 will light when SEL0=0 and LED D6 will light when SEL1=0. *Note: For the demonstration scenario, an additional transistor circuit of the evaluation board stretches WDT_Intr output period to make the interrupt event visible to the eye.*
XX10	**2 sec WDT (SEL0=1, SEL1=0)** Enables a 2-second period watchdog timer (WDT).
XX01	**10 sec WDT (SEL0=0, SEL1=1)** Enables a 10-second period watchdog timer (WDT).

Setting	Function
XX11	**1 min WDT (SEL0=1, SEL1=1)** Enables a 1-minute period watchdog timer (WDT).
X0XX	**Disable Reset Pulse Stretch (RST=0)** Disables the reset pulse stretch option of POWR607. A red LED D4 will light when RST=0.
X1XX	**Enable 200ms Reset Pulse Stretch (RST=1)** Appends an additional 200 ms period to any processor/DSP reset output asserted by the POWR607. Programmable clock and timer functions of the POWR607 allow for a variety of timeout intervals from 32 us to 1.96 sec in 128 steps. It may be necessary to connect a logic analyzer to detect the pulse stretch.
0XXX	**1.8 V Supply OK (VM3=1.8)** Connects the 1.8V supply rail to the voltage monitor input (VMON3) of the POWR607. This setting emulates a stable 1.8 V supply.
1XXX	**1.8 V Supply Failure (VM3=High-Z)** Disconnects the 1.8 V supply rail from the voltage monitor input (VMON3) of the POWR607. This setting emulates a DC-DC converter or other supply failure on the PCB. The POWR607 will assert the Reset_CPU output signal to initiate a reset of the processor/DSP target device. A red LED (D2) will light to indicate the power fail condition.
Push-button Switch	
WD_Trig	**WDT Trigger** Press the push-button switch (WD_Trig) to emulate the watchdog timer reset trigger issued periodically for normal operation by the processor/DSP.
Reset	**Manual Reset** Press the push-button switch (Reset) to assert a manual reset of the evaluation board. All timers of the POWR607 will be cleared and the Reset_CPU output signal will be asserted.
Slide Potentiometer	
R16	**Voltage Supervisor Input** A slide potentiometer emulates the variability of a 2.5 V voltage rail on the PCB. Slide the pot towards the 0.0 V position to lower the voltage level input to the POWR607 voltage monitor (VMON2).

Connect to the POWR607/6AT6 Evaluation Board

To power and program the evaluation board you may use a PC USB port or use a combination of an external 5 V power supply and a JTAG cable. If your PC does not provide a USB port, see Adding Support for a JTAG Cable and/or I^2C Communications in the Modifying the POWR607/6AT6 Evaluation Board section.

USB Cable Connection

Use the USB cable provided to connect the evaluation board to your PC:

1. Connect the USB cable from a USB port on your PC to the board's USB mini-B socket (J1) on the bottom left side of the board. After connection is made, a blue Power LED (PWR) will light up indicating the board is powered on.
2. If you are prompted, "Windows may connect to Windows Update" select **No, not this time** from available options and click **Next** to proceed with the installation. Choose the **Install from specific location (Advanced)** option and click **Next**.
3. Select **Search for the best driver in these locations** and click the **Browse** button to browse to the Windows driver folder created in the Download Windows Hardware Drivers section. Select the CDM 2.04.06 WHQL Certified folder and click **OK**.
4. Click **Next**. A screen will display as Windows copies the required driver files. Windows will display a message indicating that the installation was successful.
5. Click **Finish** to install the USB driver.

JTAG Cable Connection

Use a JTAG cable (sold separately) to connect the evaluation board to your PC:

1. Connect external +5 V and GND power to pad locations J5 and J6 (Schematic Sheet 5 of 6).
2. Connect a JTAG cable from a JTAG source to the board's JTAG header (J3) (Schematic Sheet 5 of 6) on the right side of the board.

See Adding Support for a JTAG Cable and/or I^2C Communications in the Modifying the POWR607/6AT6 Evaluation Board section for information on how to modify the evaluation board to add a JTAG header connection.

Run the Processor Support Demo

The POWR607 Processor Support Demo illustrates key functions of the POWR607: voltage supervisor, reset generator, and watchdog timer (WDT). The block diagram of the processor support demo, Figure 3, shows the POWR607 interface to a simulated processor/DSP. LEDs and switches are used to emulate the processor interface.

Many processor power management scenarios can be shown with the POWR607 evaluation board. Follow the procedure below to emulate one particular case.

1. Set the POWR607 configuration to indicate 1.8 V Supply OK, disable reset pulse stretch and enable a two- second watchdog timer period.

   Select DIP Switch (1, 2, 3, 4) = 0010

   Note: To indicate a logical 1, slide the switch towards the 1, 2, 3, or 4 numeral marks on the case. Select the R16 Slider = 3.3 V position.
2. Press and then release the Reset push button.

   The POWR607 Evaluation Board is reset. The CPU Reset LED (D2) lights to indicate the reset condition. The WDT timer is reset and the two-second WDT count begins.
3. Press and release the WD_Trig push button.

   The WDT_Trig signal is asserted by the processor/DSP. The POWR607 timer/counter is reset and the two- second watchdog timer restarts.

   Continue pressing the WD_Trig to "pet" the watchdog timer to prevent the two-second timeout.
4. Wait for two seconds and allow the WDT timer period to expire.

   The POWR607 asserts the WDT_Intr output signal and the WDT_Interrupt LED (D11) lights momentarily to indicate the interrupt condition.

   In the next step you will increase the watchdog timer period from 2 seconds to 10 seconds and enable Reset Pulse Stretch.
5. Select SW1 (1, 2, 3, 4) = 0101. Also select the R16 Slider = 3.3 V position. Press and release the Reset push button on the POWR607 board.

   The CPU Reset LED (D2) light indicates the reset condition. The WDT timer is reset and the 10-second WDT count begins.

   The following steps emulate a brown out condition of a 2.5 V supply rail output of a DC-to-DC converter (DC-DC#2) monitored by the POWR607.

6. Slowly slide R16 towards the 0.0 V position.

   Once the POWR607 voltage monitor detects the 2.5 V supply rail has dropped below a 2.5 V -5% threshold value a supply fault will be triggered and the Reset CPU output signal is asserted. The CPU Reset LED (D2) light indicates the reset condition. Note that the POWR607 watchdog timer is also disabled.
7. Slide R16 toward the 3.3 V position. Once the POWR607 voltage monitor detects that the 2.5 V rail is above a threshold value of 2.5 V -5%, the Reset CPU output signal is released. The CPU Reset LED (D2) light goes out.

Run the Voltage Monitoring Demo

The voltage monitor demo illustrates how to access the 2-wire I^2C slave interface of the ispPAC-POWR6AT6 device to perform voltage level measurements. This is a popular means for a microcontroller/microprocessor to monitor voltages and adjust the voltage profiles of the POWR6AT6 DC-DC converter margin output drivers. For more information on POWR6AT6 end applications see AN6077, Stable Operation of DC-DC Converters with Power Manager Closed Loop Trim. This demo uses the ispPAC-POWR6AT6 I^2C Utility software provided with PAC-Designer software running on a host PC to emulate a processor's interface to the POWR6AT6.

1. Modify the evaluation board to use the JTAG cable. See Adding Support for a JTAG Cable and/or I^2C Communications in the Modifying the POWR607/6AT6 Evaluation Board section for more information.
2. Install PAC-Designer software.
3. From the PAC-Designer<ver>\Macro directory, run PowerManager_6AT6_I2C_Utility.exe. For more information on the I^2C Hardware Verification Utility software and operation see AN6067, ispPAC-POWR1220AT8 I2C Hardware Verification Utility User's Guide.
4. Set I^2C Address = 6Ah

Download Demo Designs

The processor support demo is preprogrammed into the POWR607 Evaluation Board, however over time it is likely your board will be modified. Lattice distributes source and programming files for demonstration designs compatible with the POWR607 board.

To download demo designs:

1. Browse to the POWR607 Development Kit web page of the Lattice web site. Select the Demo Applications download and save the file.
2. Extract the contents of "POWR607_DK_DemoSource.zip" to an accessible location on your hard drive. Two demo design files are unpacked.

   Where:

Demo	Files
Processor Support Demo	Demo_POWR607_DK.pac
Voltage Monitoring with the POWR6AT6 Demo	Demo_POWR6AT6_DK.pac

Recompile a Demo Project with PAC-Designer

Use the procedure described below to recompile any of the demo projects for the POWR607 Evaluation Board.

1. Install PAC-Designer software
2. Download the demo source files from the POWR607 Development Kit web page.
3. Run PAC-Designer.
4. Open the **<demo>.pac** project file.
5. From the schematic block diagram, double-click the **Sequence Controller block**. The LogiBuilder interface appears.

6. Choose **Tools > Compile LogiBuilder Design**. After a few moments the JEDEC programming file is output.
7. See the Processor Support Demo section of this document for details on downloading a programming file to the board.

Download Windows Hardware Drivers

If you wish to reprogram the POWR607/6AT6 Evaluation Board, you will need to obtain the necessary hardware drivers for Windows. If your installation of Windows does not automatically install USB drivers when the evaluation board is connected to a USB port, then use the procedure below to download them from the Lattice web site.

To download Windows Hardware Drivers:

1. Browse to the POWR607/6AT6 Evaluation Board web page, locate the hardware device drivers for the USB/JTAG interface. See www.latticesemi.com/boards and look for the POWR607/6AT6 Evaluation Board.
2. Download the ZIP file to your system and unzip it to a location on your PC.

Programming with Lattice Diamond Programmer

The processor support and voltage monitoring demo designs are pre-programmed into the POWR607/6AT6 Evaluation Board by Lattice. To restore a POWR607/6AT6 Evaluation Board to factory settings or load an alternative demo design, use the procedures in this section.

To install Lattice Diamond Programmer:

1. Install Lattice Diamond or standalone Lattice Diamond Programmer.
2. Connect the board to a host PC using the USB port or JTAG header connection.
3. Follow the USB Cable Interface or JTAG Cable Interface procedure below to program the evaluation board.

USB Cable Interface

The POWR607/6AT6 Evaluation Board is equipped with a built-in USB-based programming circuit. This consists of a USB PHY and a USB connector. When the board is connected to a PC with a USB cable, it is recognized by the Diamond Programmer as a “USB Download Cable”. The POWR607 and POWR6AT6 can then be scanned and programmed using the Diamond Programmer.

To program a demo programming file:

1. From the Start menu, click **All Programs > Lattice Diamond > Accessories > Diamond Programmer** . Diamond Programmer starts.
2. The Diamond Programmer – Getting Started dialog box appears.
3. Select the following options:

   Create a New Project from a Scan.

   Cable: **USB2** Port: **FTUSB-0**

   Click **OK**.

4. The Diamond Programmer window appears.

   The New Scan Configuration Setup window appears. The ispPAC-POWR607 and ispPAC-POWR6AT6 device(s) appear in the device list. In case the devices fail to appear, try doing scanning again

   In Programmer, choose **Design > Scan** or click in the toolbar. Programmer opens a new chain configuration file, scans the printed circuit board connected to your computer, and lists the devices in the new chain file.
5. Make sure the **Operation** is **Erase**, **Program**, **Verify**.

6. Click on the **File Name** section and browse to the **<Demo Dir>\project** folder, select **<Demo>.jed**, and click **Open**.

   Select appropriate JEDEC files of POWR607 and POWR6AT6

7. In Programmer, choose **Design > Program**, or click  on the toolbar programming will start.

Programming requires about 20-40 seconds. During programming, a pop-up “Programming XCF” appears. At the end of programming, the Output console of Programmer should show “Operation: successful”.

JTAG Cable Interface

This section describes how to connect and reprogram the evaluation board using a JTAG cable.

1. Connect external +5 V and GND power to pad locations J5 and J6.
2. Connect the JTAG cable between J3 header and the JTAG source.
3. Run Lattice Diamond Programmer to program the POWR607 board.
4. Follow the procedure of “USB Cable Interface” using Diamond Programmer, select Cable “LATTICE” and download JEDEC files to selected devices.

POWR607/6AT6 Evaluation Board

This section describes the features of the POWR607/6AT6 evaluation board in detail.

Overview

The POWR607/6AT6 Evaluation Board is a complete development platform for the Lattice POWR607 mixed-signal device. The board includes circuitry to emulate a processor/DSP interface, a USB program/power port, SMD and thru-hole prototyping areas, and an expansion header to support test connections. A Power Manager II ispPAC-POWR6AT6 is included and can be programmed to demonstrate power supply margin and trim applications. The board is powered by a PC USB port and you may reprogram the board using Lattice Diamond Programmer. If no USB port is available for your PC, the board can be modified such that it can be powered with an external power supply and programmed with a JTAG cable (sold separately) from another JTAG source.

Figure 4. POWR607/6AT6 Evaluation Board Block Diagram

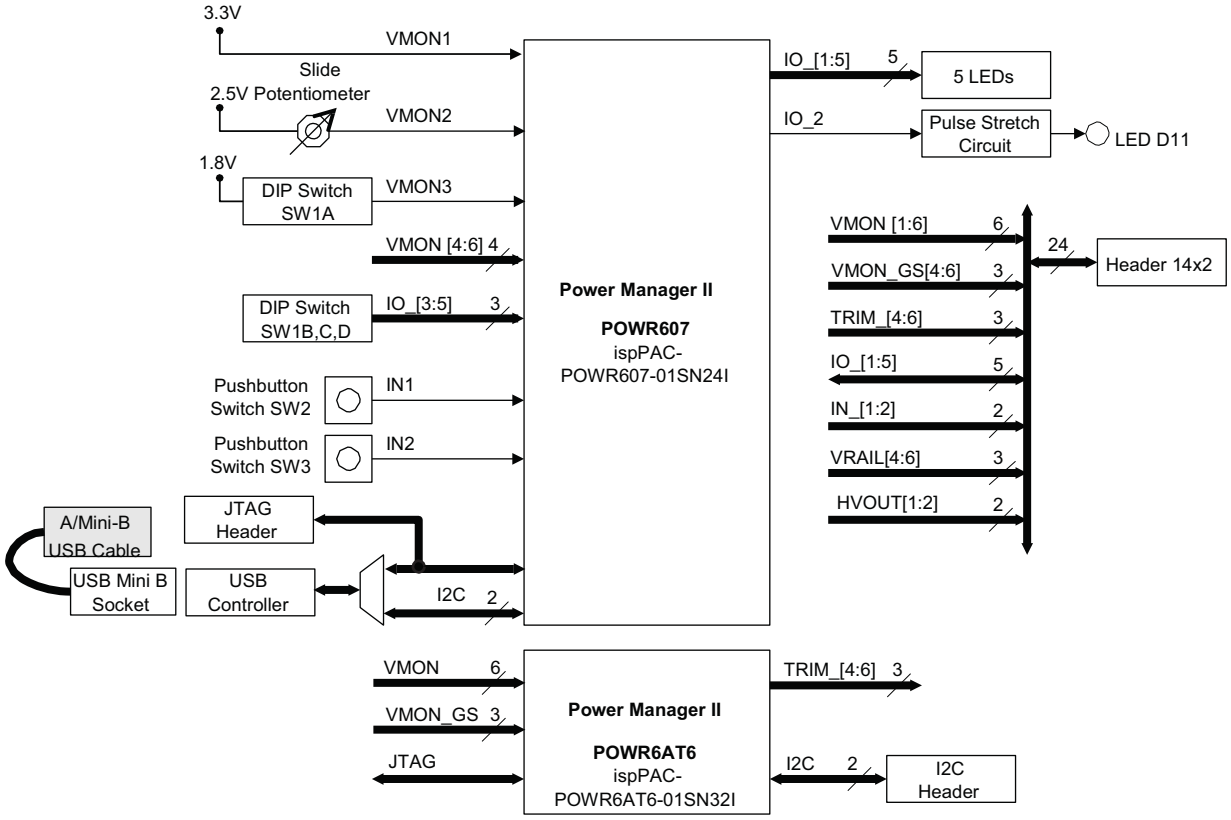


Table 2 describes the components on the board and the interfaces it supports.

Table 2. POWR607/6AT6 Evaluation Board Components and Interfaces

Component/Interface	Type	Schematic Reference	Description
Circuits			
Pulse Stretch Circuit	Circuit	Q4, D10, D11	Stretch watchdog interrupt pulse outputs to 40ms.
USB Controller	Circuit	U8:FT2232H	USB-to-JTAG interface.
USB Mini B Socket	I/O	J1:USB_MINI_B	Programming and debug interface.
Components			
Power Manager II	Mixed Signal IC	U3: ispPAC-POWR6AT6	Voltage monitor, margin, trim.
Power Manager II	Mixed Signal IC	U1:ispPAC-POWR607	Mixed Signal Device.
Interfaces			
8x1 Header Landing	I/O	J2:I2C	I^2C interface.
8x1 Header Landing	I/O	J3:JTAG Interface	JTAG interface.
14x2 Header	I/O	J4:HEADER 14X2	User-definable I/O.
5 LEDs	Output	D7-D0	User-definable LEDs, I/O1 to I/O5.
DIP Switch	I/O	SW1A, B, C, and D	4-bit DIP switch.
Push-button Switches	I/O	SW2:Reset, SW3:WD_Trigger	General-purpose push buttons.
Slide Potentiometer	I/O	R16	Potentiometer tied to 3.3 V rail. Emulates brown-out 2.5 V conditions at VMON2 inputs of POWR607 and POWR6AT6.

Subsystems

This section describes the principle sub-systems for the POWR607/6AT6 Evaluation Board in alphabetical order. When reviewing the board, orient it so the silkscreen markings are readable.

DIP Switch

The evaluation board includes a four-bit input toggle switch located in the lower-right corner of the board. Three are available as general purpose inputs. Slide the switch towards the numeral mark on the switch case to indicate a logical '1'.

Table 3. DIP Switch Reference

Item	Description
Reference Designators	SW1A, B, C and D
Part Number	219-4MST
Manufacturer	CTS
Web Site	www.ctscorp.com

Table 4. DIP Switch Pin Information

SW1	Description	POWR607 Pin
D/4	Watchdog Delay SEL1 or user-defined input	15
C/3	Watchdog Delay SEL0 user-defined input	17
B/2	Reset Pulse Stretch enable or user-defined input	18
A/1	3.3 V supply rails to VMON3 connection	4

Expansion Header

The expansion header provides 28user I/O's connected to the POWR607 and POWR6AT6. The remaining pins serve as power for expansion boards. The expansion connector is configured as one 16x2 100mil centered pin header.

Table 5. Expansion Connector Reference

Item	Description
Reference Designators	J4
Part Number	90131-0800
Manufacturer	Molex/Waldom Electronics
Web Site	www.molex.com

Table 6. Expansion Header Pin Information

J4 Pin	Function	POWR607 Pin	POWR6AT6 Pin	Other Connections
1	+3.3 V	—	—	
2	+3.3 V	—	—	
3	IO_5	IN_OUT5	—	
4	IO_4	IN_OUT4	—	
5	IO_3	IN_OUT3	—	
6	IO_2	IN_OUT2	—	
7	IO_1	IN_OUT1	—	
8	IN2	IN2	—	
9	IN1	IN1	—	

J4 Pin	Function	POWR607 Pin	POWR6AT6 Pin	Other Connections
10	HVOUT2	—	—	
11	HVOUT1	—	—	
12	VMON2	VMON2	VMON2	
13	VMON1	VMON1	VMON1	
14	VMON3	VMON3	VMON3	
15	VMON4	VMON4	VMON4	
16	TRM4	—	DAC4	
17	VMON4_GS	—	VMON4GS	
18	VRAIL4	—	—	Voltage supervisory circuit
19	VMON5	VMON5	VMON5	
20	TRM5	—	DAC5	
21	VMON5_GS	—	VMON5GS	
22	VRAIL5	—	—	Voltage supervisory circuit
23	VMON6	VMON6	VMON5	
24	TRM6	—	DAC6	
25	VMON6_GS	—	VMON6GS	
26	VRAIL6	—	—	Voltage supervisory circuit
27	GND	—	—	
28	GND	—	—	

JTAG Interface Circuits

For power and programming, an FTDI USB UART/FIFO IC converter provides a communication interface between a PC host and the JTAG programming chain of the POWR607 board. The USB 5 V supply is also used as a source for the 3.3 V and 1.8 V supply rails. A USB B-type mini socket is provided for the USB connector cable.

The evaluation board can be modified to use a JTAG cable for programming. See Adding Support for a JTAG Cable and/or I^2C Communications in the Modifying the POWR607/6AT6 Evaluation Board section for more information.

Table 7. JTAG Interface Reference

Item	Description
Reference Designators	U8
Part Number	FT2232H
Manufacturer	FTDI (Future)
Web Site	www.ftdichip.com

Table 8. JTAG Programming Pin Information

Signal Name	Description	POWR607 Pin	POWR6AT6
TDO	Test Data Output	11:TDO	4:TDI
PM_TDO	Test Data Output	—	1:TDO
PM_TDI	Test Data Input	13:TDI	—
TMS_605	Test Mode Select	14:TMS	—
TMS_6AT6	Test Mode Select	—	5:TMS
PM_TCK	Test Clock	12:TCK	3:TCK

LEDs

Five red LEDs (D2-D6) are used to reflect I/O's of the preprogrammed processor support demo. Three of the five LEDs are connected to DIP switch inputs. The LEDs are located in the center of the board, next to the expansion header. You may use D2-D6 for user-defined outputs for your own custom POWR607 designs.

A blue LED (POWR - D1) is used to indicate USB 5 V power. An amber LED (D11) is used to indicate interrupt events asserted by the POWR607.

Table 9. User LEDs Reference

Item	Description
Reference Designators	D2-D6
Part Number	LTST-C190CKT
Manufacturer	Lite-On
Web Site	www.liteonit.com

Table 10. LED Pin Information

Signal Name	Description (Processor Support Demo)	POWR607 Pin
D6	IO_5, Watchdog Delay SEL1 input	15
D5	IO_4, Watchdog Delay SEL0 input	17
D4	IO_3, Reset Pulse Stretch enable input	18
D3	IO_2, Watchdog timer interrupt (WDT_Intr) output	19
D2	IO_1, CPU Reset or Power Fail output	20
D1	USB 5 V Power	na
D11	Watchdog Timer Pulse	na

POWR607

The POWR607 device (ispPAC-POWR607) on the board integrates voltage supervisor, watchdog timer, and reset generator functions in a 4x4 mm chip scale package

Table 11. POWR607 PLD Reference

Item	Description
Reference Designators	U1
Part Number	ispPAC-POWR607-01-SN24I
Manufacturer	Lattice Semiconductor
Web Site	www.latticesemi.com

Table 12. POWR607 Pin Information

Pin #	Pin Function	Board Connection Processor Support Demo
1	VMON1	VMON1
2	VMON2	VMON2
3	VCCD	—
4	VMON3	VMON3
5	VMON4	VMON4
6	VMON5	VMON5
7	VMON6	VMON6
8	GNDA	—
9	GNDD	—
10	VCCJ	—
11	TDO	TDO
12	TCK	PM_TCK
13	TDI	PM_TDI
14	TMS	TMS_605
15	IN_OUT7	IO_5
16	VCCA	—
17	IN_OUT6	IO_4
18	IN_OUT5	IO_3
19	IN_OUT4	IO_2
20	IN_OUT3	IO_2
21	IN2	IN2
22	IN1_PWRDN\	IN1
23	HVOUT1	—
24	HVOUT2	—

Power Supply

A single 3.3 V supply voltage for the board components is provided from the USB connection.

POWR6AT6

The POWR6AT6 device (ispPAC-POWR6AT6) on the board provides power supply margin and trim functions, analog input monitoring with an embedded 10-bit ADC in a 5x5 mm quad flat-pack package.

Table 13. POWR6AT6 Reference

Item	Description
Reference Designators	U3
Part Number	ispPAC-POWR6AT6-01-SN32I
Manufacturer	Lattice Semiconductor
Web Site	www.latticesemi.com

Table 14. ispPAC-POWR6AT6 Pin Information

Pin #	Pin Function	Board Connection Processor Support Demo
1	TDO	PM_TDO
2	VCCJ	—
3	TCK	PM_TCK
4	TDI	TDO
5	TMS	TMS_6AT6
6	CLTENb	CLTENb
7	VPS0	VPS0
8	VPS1	VPS1
9	CLTLOCK/SMBA	—
10	SCL	PM_SCL
11	SDA	PM_SCA
12	VCCD	—
13	VCCA	—
14	VMON1GS	—
15	VMON1	VMON1
16	VMON2GS	—
17	VMON2	VMON2
18	VMON3GS	—
19	VMON3	VMON3
20	VMON4GS	VMON4_GS
21	VMON4	VMON4
22	VMON5GS	VMON5_GS
23	VMON5	VMON5
24	VMON6GS	VMON6_GS
25	VMON6	VMON6
26	TRIM6	TRIM6
27	TRIM5	TRIM5
28	TRIM4	TRIM4
29	TRIM3	—
30	TRIM2	—
31	TRIM1	—
32	GND	—

Pulse Stretch Circuit

The pulse stretch circuit (Schematic Sheet 4 of 5) produces a ~40ms period pulse so watchdog timer interrupt outputs are visible to the eye. When active, amber LED (D11) blinks. The actual output pulse generated by the POWR607 is about 6 µs.

Push-button Switches

The board has two momentary push-button switches (SW2 and SW3) to support the pre-loaded processor support demo. SW2 is tied to a POWR607 input pin (IN1) which asserts the Reset input. SW3 is tied to a POWR607 input pin (IN2) which asserts the watchdog trigger (WD_Trig) input. You may use SW2/SW3 for user-defined inputs for your own custom POWR607 designs.

Modifying the POWR607/6AT6 Evaluation Board

The POWR607/6AT6 Evaluation Board provides landing areas for additional circuits to support the following functions:

- Additional voltage supervisor input circuits
- SMD and thru-hole prototyping areas on top and bottom
- Measure power-down current draw of the POWR607 device
- Bypass devices in the JTAG programming chain
- Powering the board with an external 5 V supply
- Programming the board with a JTAG cable
- Interfacing to the PAC-Designer I²C Utility software for the POWR6AT6 Power Manager II

*Note: Modifying your board requires good e*lectronics handling and PCB fabrication techniques to avoid damage.

Adding Support for a JTAG Cable and/or I²C Communications

This section describes how to modify the POWR607/6AT6 evaluation board to use a JTAG cable for JTAG programming and/or I²C communications. The JTAG header interface is required if your PC does not provide a USB port interface and you wish to reprogram the board. The I²C header interface is required to communicate with the PAC-Designer POWR6AT6 I²C Utility program.

To modify the evaluation board to support a JTAG cable:

1. Remove R20, R35, R45 and R58 (Schematic Sheet 2 of 6).
2. Install R28, R29, R27, Q3 and Q2 (Schematic Sheet 5 of 6).
3. Install an 8-pin header at location J3 - JTAG Interface (Schematic Sheet 5 of 6).

To modify the evaluation board to support I²C communications:

1. Remove R59 and R70 (Schematic Sheet 2 of 6).
2. Install an 8-pin header at location J2 - I²C Interface (Schematic Sheet 5 of 6).

Add Voltage Supervisor Circuits

This section describes how to modify the POWR607/6AT6 Evaluation Board for additional voltage supervisor demonstrations. Add a pair of resistors for each additional voltage monitor input channel that you require to the onboard voltage supervisor circuits (Schematic Sheet 3 of 6) at positions R21/R22, R23/R24, and R25/R26. Each supervisor circuit is a voltage divider with the following characteristics:

- 1% accurate resistors
- yk <= 3k ohms
- Select x and y resistor values so VMON = 0.669V
- Install Zener diodes if VRAIL > 5.5 V
- Remove 100k ohm for higher accuracy

You may attach prototype circuits or test equipment to the VMON inputs using J4 - HEADER 14X2 (Schematic Sheet 5 of 6).

For more information on sensor circuit interfaces to Power Manager II and POWR607 devices, see AN6041, Extending the VMON Input Range of Power/Platform Management Devices.

Measure Power-Down Current of the POWR607

This section describes how to modify the POWR607 power supply connections to support current measurements.

1. Remove R43 and R44 (Schematic Sheet 1 of 6).
2. Install jumper at location J12 (PM_VCC) (Schematic Sheet 1 of 6).
3. Attach ammeter to pins 1 and 2 of J12.

JTAG Chain Bypass

This section describes how to selectively bypass the POWR607 or POWR6AT6 devices in the JTAG programming chain.

1. JTAG TMS bypass: Remove R42 (POWR607 TMS) or R41 (POWR6AT6 TMS) to bypass either device. To reverse the bypass you may install jumpers at locations J10 or J11 to reconnect the TMS circuit (Schematic Sheet 1 of 6).
2. Install 10k ohm resistors at locations R39 and R40 (Schematic Sheet 1 of 6).
3. JTAG TDI/TDO bypass: Install jumpers at locations J7 (Bypass 607/5) or J8 (Bypass 6AT6) to break the TDI / TDO circuit.

Mechanical Specifications

Dimensions: 3.75 in. [L] x 2.0 in. [W] x 1.00 in [H]

Environmental Requirements

The evaluation board must be stored between -40° C and 100° C. The recommended operating temperature is between 0° C and 55° C.

The evaluation board can be damaged without proper anti-static handling.

Glossary

CPLD: Complex Programmable Logic Device

DIP: Dual in-line package.

I^2C: Inter-Integrated Circuit.

LED: Light Emitting Diode.

Mixed-Signal PLD: A PLD integrated with analog and mixed signal support circuitry.

PCB: Printed Circuit Board.

RoHS: Restriction of Hazardous Substances Directive.

PLL: Phase Locked Loop.

SPI: Serial Peripheral Interface.

SRAM: Static Random Access Memory.

TransFR™: Transparent Field Reconfiguration.

UART: Universal Asynchronous Receiver/Transmitter.

USB: Universal Serial Bus.

WDT: Watchdog timer

Ordering Information

Description	Ordering Part Number	China RoHS Environment-Friendly Use Period (EFUP)
POWR607/6AT6 Evaluation Board	PACPOWR607-P-EVN	

Technical Support Assistance

e-mail: techsupport@latticesemi.com

Internet: www.latticesemi.com

Revision History

Date	Version	Change Summary
July 2014	01.0	Initial release.

Appendix A. Schematics

Figure 5. Power Manager 605, 607 and 6AT6

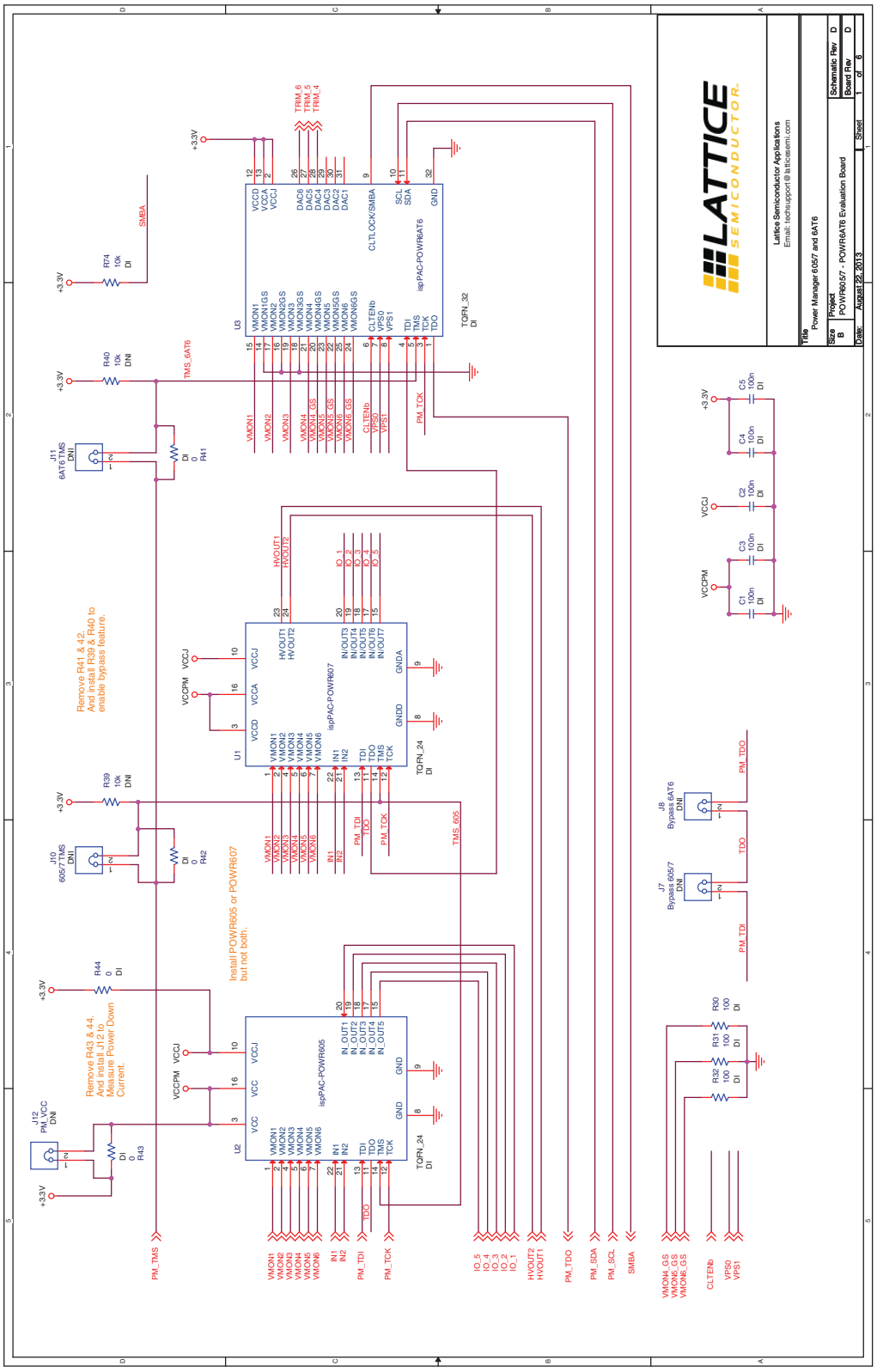


Figure 6. USB to JTAG and I²C Interface

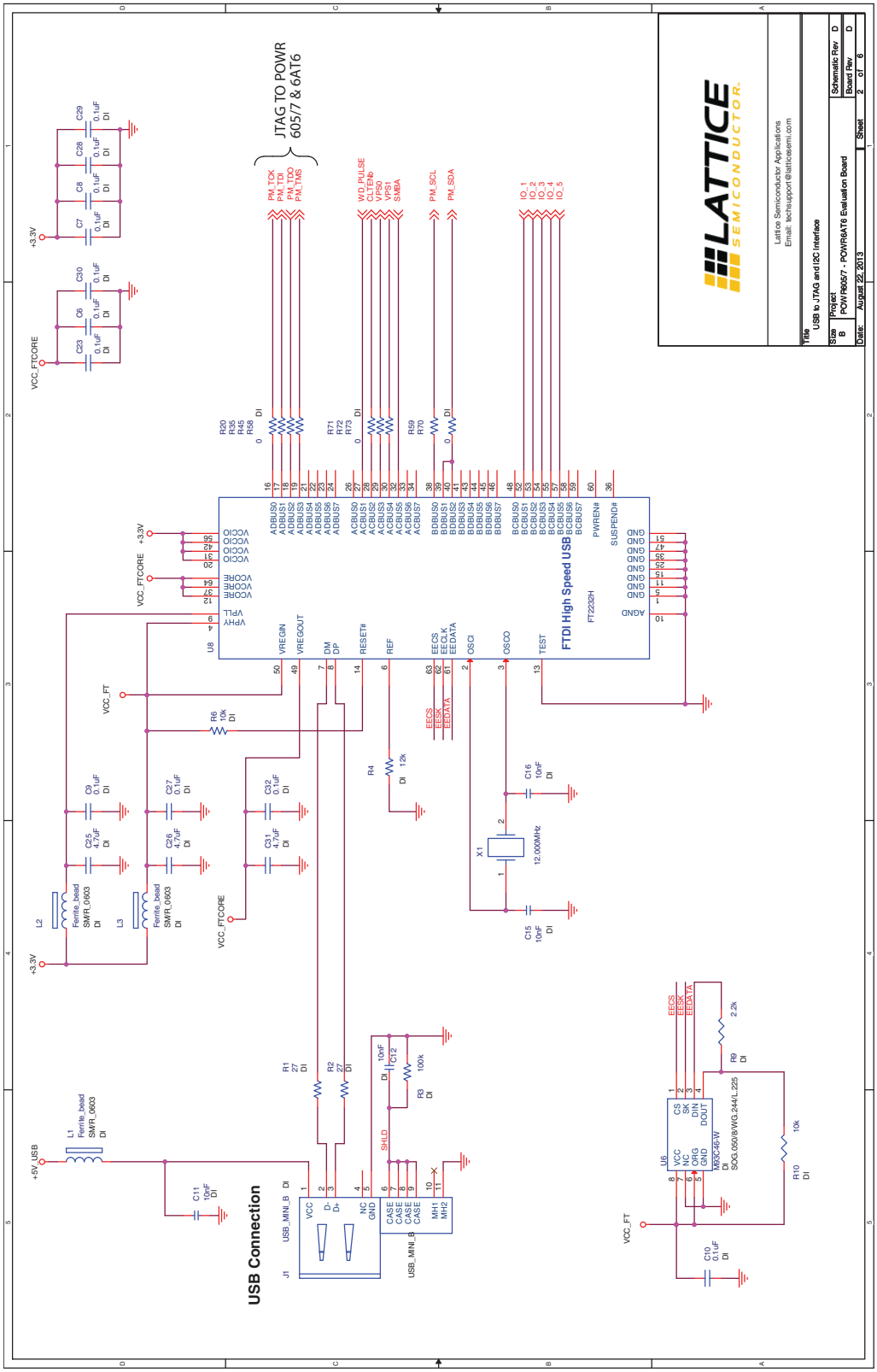


Figure 7. Power Supply

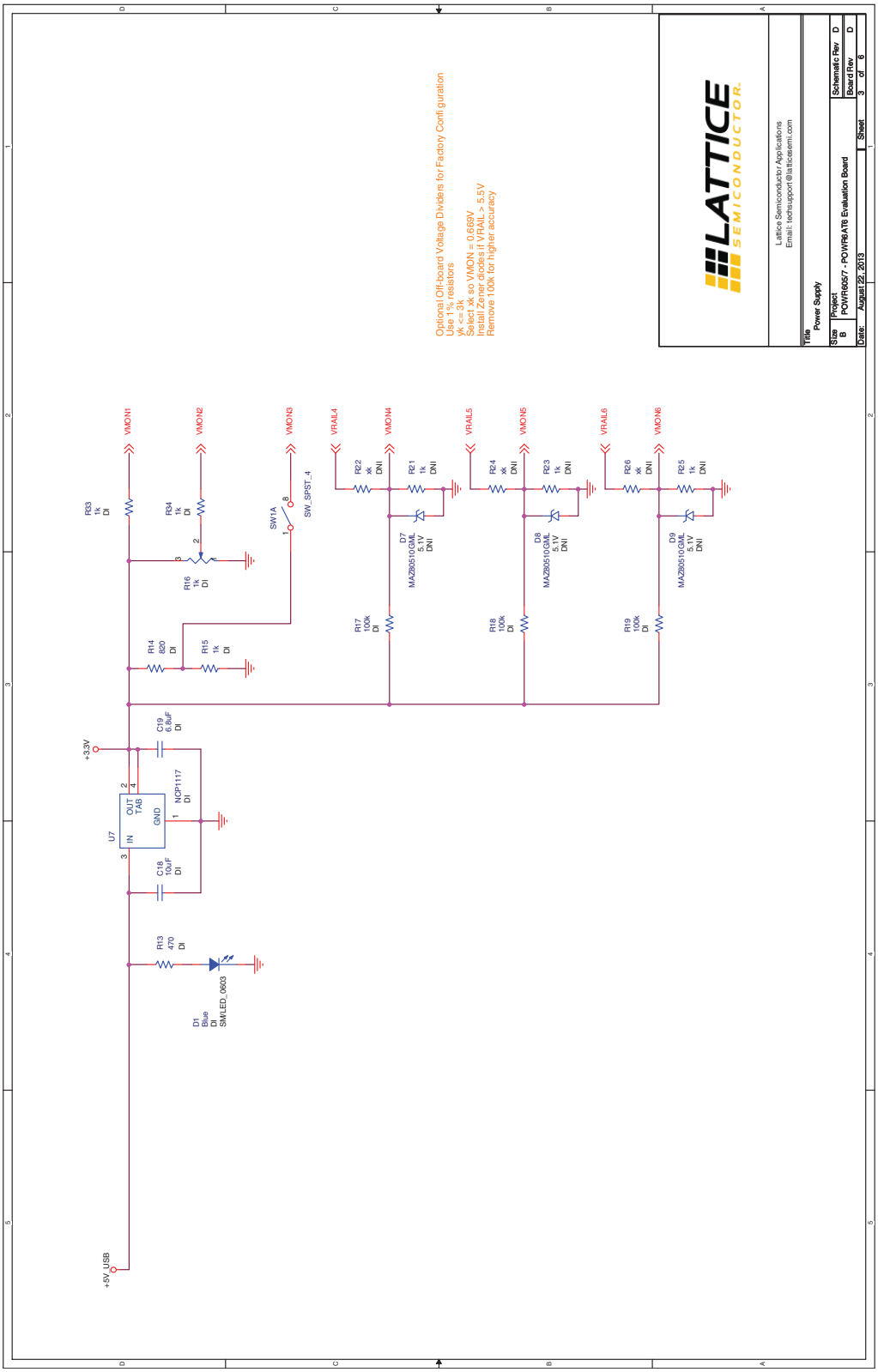


Figure 8. LEDs and Switches

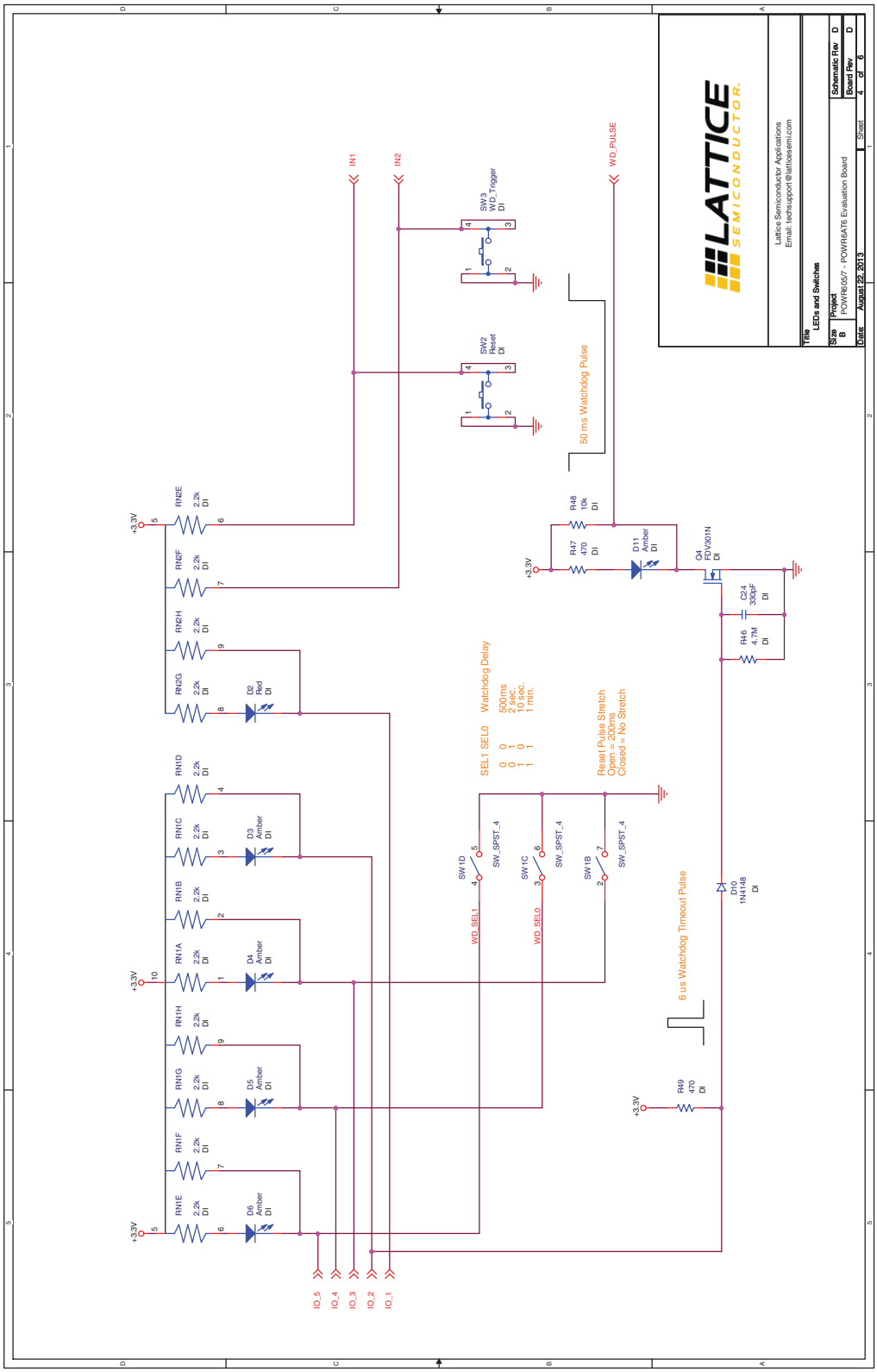


Figure 9. (Optional) JTAG, I²C and Test Headers

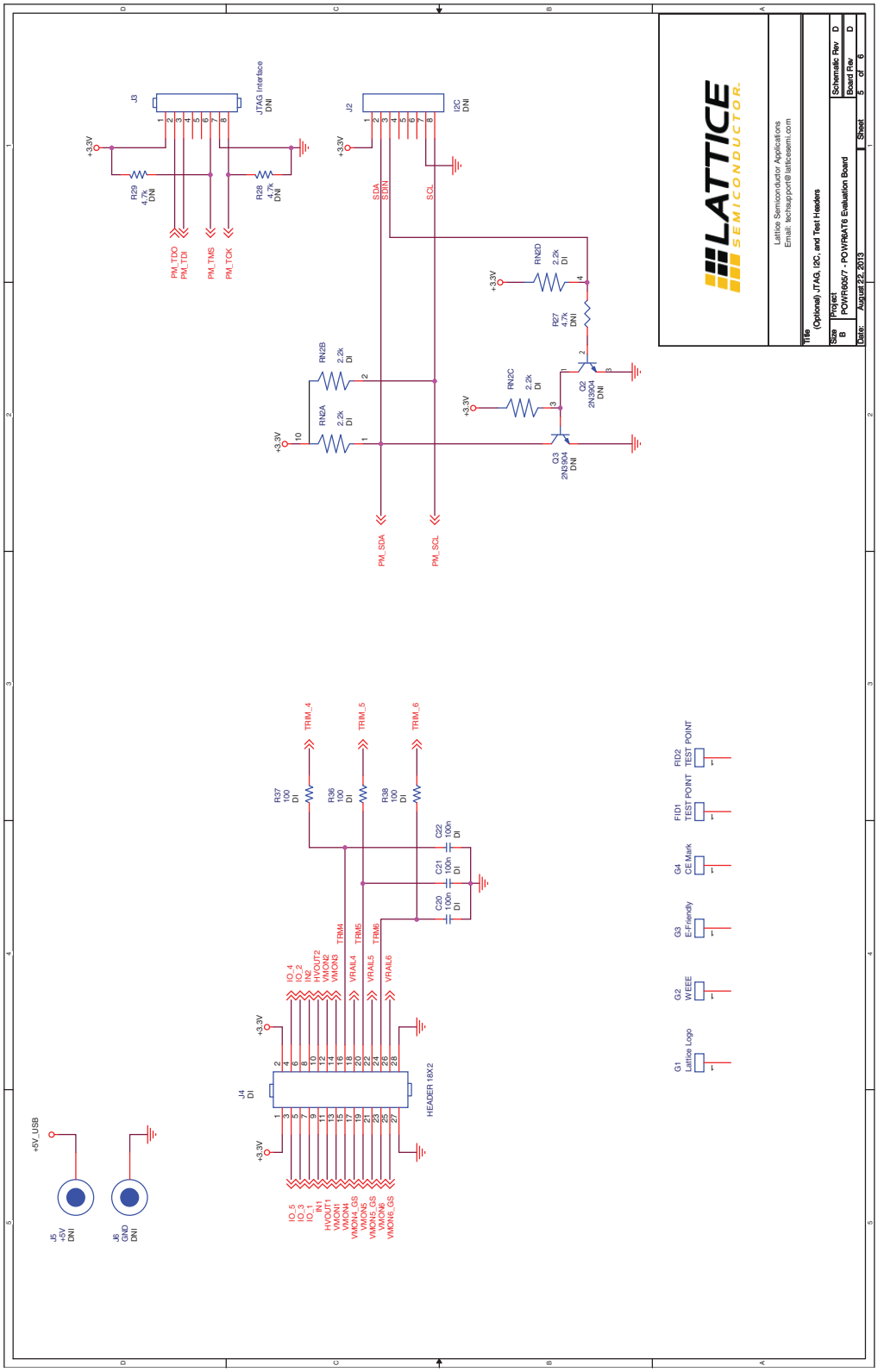
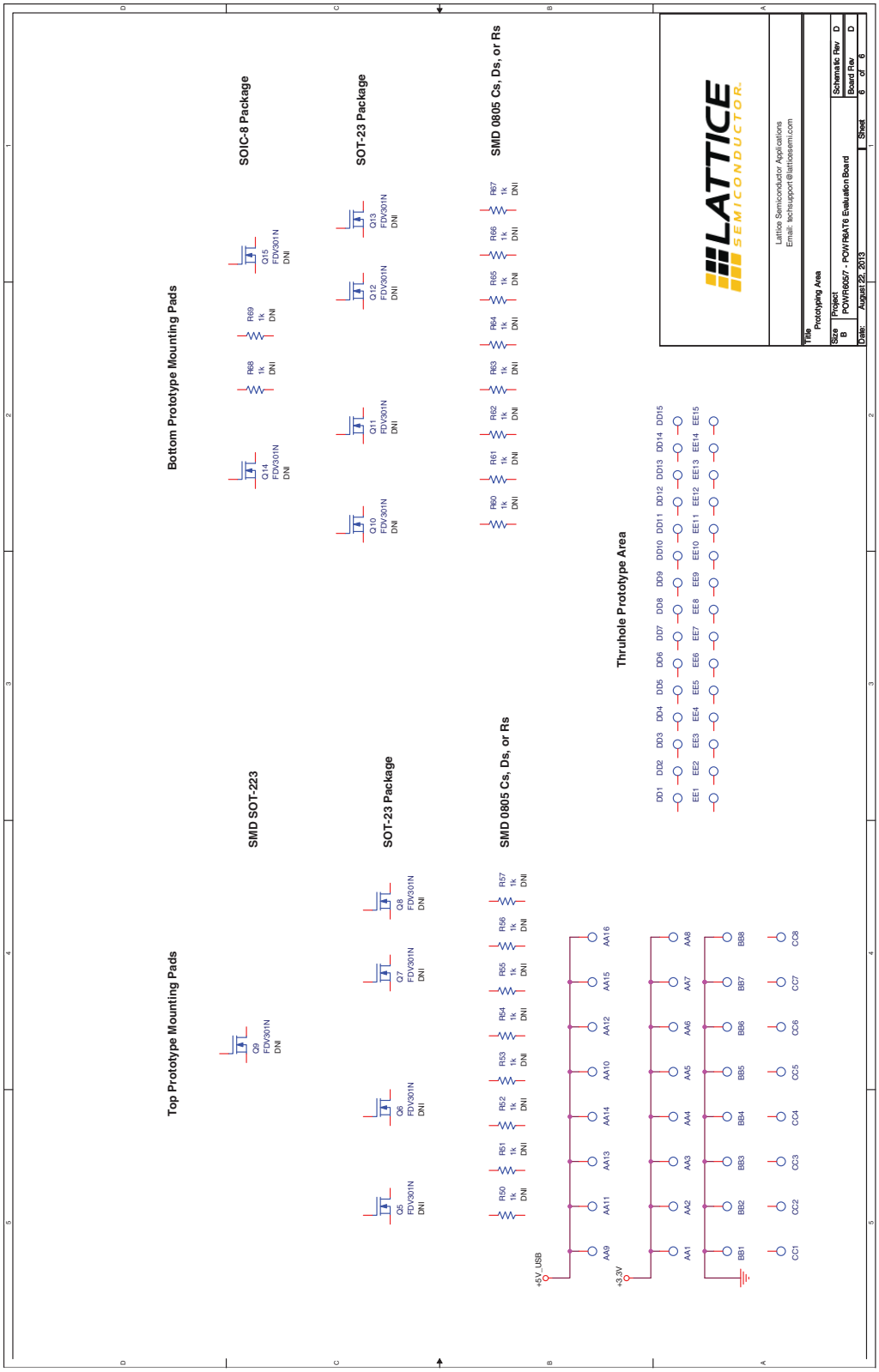


Figure 10. Prototype Area



Appendix B. Bill of Materials

Table 15. Bill of Materials

Item	Quantity	Reference	Part Number
1	1	U1	ispPAC-POWR607
2	0	U2	ispPAC-POWR605
3	1	U3	ispPAC-POWR6AT6
4	1	U6	M93C46-WMN6TP
5	1	U7	NCP1117ST33T3G
6	1	U8	FT2232H
7	1	D1	LTST-C190TBKT
8	1	D2	LTST-C190CKT
9	5	D3-D6,D11	LTST-C190AKT
10	1	D10	1N4148
11	16	C1-10, 20-22,23,27-30,32	ECJ-1VB1C104K
12	2	C11,12	ECJ-1VB1C103K
13	2	C15,16	ECJ-1VB1C103K
14	3	C25,26,31	ECJ-1VB1C475K
15	3	C30-32	ECJ-1VB1C104K
16	1	C18	ECJ-2YB1A105K
17	1	C19	F920J106MPA
18	1	Q4	FDV301N
19	1	J1	UX60-MB-5ST
20	1	J4	90131-0800
21	1	R16	RA2043F-20-10EB1-B1K
22	1	R46	ERJ-3GEYJ475V
23	4	R3,R17-19	ERJ-3GEYJ104V
24	4	R6,R10,R48,R74	ERJ-3GEYJ103V
25	1	R9	ERJ-3GEYJ222V
26	1	R4	ERJ-3GEYJ123V
27	3	R15,R33,R34	ERJ-3GEYJ102V
28	1	R14	ERJ-3GEYJ821V
29	3	R13,R47,R49	ERJ-3GEYJ471V
30	6	R30-32, R36-38	ERJ-3GEYJ101V
31	2	R1,2	ERJ-3GEYJ270V
32	13	R20,R35,R41-45,R58,59,R70-73	ERJ-3GEY0R00V
33	1	SW1	219-4MST
34	2	SW2, SW3	EVQ-Q2K03W
35	3	L1-L3	HI0603P600R-10
36	1	X1	7M-12.000MAAJ-T
37	2	RN1, RN2	746X101222JP
38	3	n/a	382811-9
39	4	n/a	SJ-5003
40	1	n/a	n/a
41	1	n/a	n/a

Table 16. Optional Parts

Item	Quantity	Reference	Part Number
1	6	J7-J12	
2	2	J2, J3	
3	2	J5, J6	
4	3	R27-R29	ERJ-3GEYJ472V
5	3	R39,R40	ERJ-3GEYJ103V
6	18	R50-57,R60-69	ERJ-3GEYJ102V
7	2	Q2,Q3	MMBT2369A
8	11	Q5-Q15	FDV301N
9	3	D7-D9	MAZ80510GML
10	6	R21-R26	