May 30, 2014

Subject: 300mm CS90F Process Transfer - Characterization Summary

SYNOPSIS

Lattice has completed the transfer of the 130nm CS90F process from Fujitsu's 200mm fab to the 300mm fab, located at the same site. This transfer effects only the Lattice Mach XO product family. Electrical characterization of the XO Product from the 300mm CS90F process was performed with very good match to product produced in the 200mm line. Lattice recommends release of the Mach XO family at the Fujitsu 300mm production line.

This document summarizes the supporting electrical characterization.

OVERALL TRANSFER PLAN

The transfer process was a cross-functional event with many moving parts. Here is a graphical overview of the process steps and sequence.

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<tr><td>Pre-Tapeout Activities</td><td>Tapeout and Fabrication</td><td>Production Wafer Sort</td><td>Package Assembly</td><td>Production Package Test</td><td>Reliability Qual</td></tr>
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Note that the characterization was performed in two steps. Wafer level characterization was performed for increased sample size. Unit-level characterization was also performed on packaged devices (256ftBGA) for those tests that were not conducive to the wafer probe environment or that required specialized bench equipment. Process-skewed wafers were generated at both the 300mm and 200mm fabs to measure operation across the full process range.

Wafer and unit characterizations were also performed by two separate engineering groups, that while coordinated in the planning process, allowed for independent auditing and reporting of the results.

Both characterization steps were focused on the largest device in the family – the XO2280E/C. Other devices in the family are characterized by extension and are validated by production yields.

Note that in this report, "200mm" will refer to the older production-released mask set, the XO2280-01 and "300mm" will refer to the new XO2280-02 mask set and process.

PRE-TAPEOUT ACTIVITIES

There is no schematic change of the MachXO2280 associated with this conversion to the 300mm wafer fab. Some changes to mask dimensions were required to keep the same dimensions on the final 300mm wafers the same as for 200mm wafers.

The intention was that the first silicon lot would be used to tune the process so that subsequent qual/characterization lots would use the final process. That is indeed what occurred but the performance of the first lot was so close to target that it was also used for yield analysis.

PROCESS SPLITS

Nominal and process skew wafers were generated for both the 200mm and 300mm process for both MXO2280C (3.3V, Upper Voltage) and MXO2280E (1.2V, Lower Voltage) product options. Note that the code for the various splits is N-channel speed/P-channel speed. For example: FF is a fast (low Vt) N-channel and fast P-channel split. Nom = nominal and LCD is long poly CD.

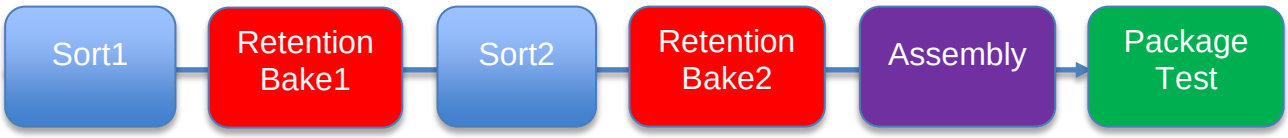
Lot	Fab	Wafer	Voltage	Split
Lot 1	300	1	LV	NOM
	300	5	LV	FF
	300	6	LV	SS
Lot 2	300	9	UV	NOM
Lot 3	300	11	UV	FF
	300	12	UV	SS
Lot 4	300	5	LV	FF
Lot 5	200	1	LV	NOM
	200	8	LV	LCD
	200	10	LV	FF
	200	21	UV	NOM
	200	17	UV	NOM
	200	19	UV	NOM

Wafers Used in Characterization

The goal was to make the 300mm process match the existing 200mm device parametric specifications (also known as E-Test or WAT data). Then, the process splits listed above were generated to allow characterization across the process spectrum. The 300mm split wafers generated a very good spectrum of devices across the entire E-test spec range.

WAFER SORT AND PACKAGE TEST YIELD SUMMARY

All wafers and packaged units for characterization first went through the standard production test flow which is shown graphically below.



Mach XO Production Test Flow

Sort 1 and sort 2 yields are equivalent for both the 200mm and 300mm processes.

Nominal and process split wafers from both 200mm and 300mm process were then assembled into packages and class tested. Package test yields (class yield) and binsplit for both processes are nearly identical. Binsplit is defined as the percentage of good units that meets the highest speed grade in the datasheet (-5, in this case).

The excellent correlation between production yields and binsplit were early indicators that product performance was the same between the production-released 200mm process and the new 300mm process.

WAFER CHAR DATA

Speed

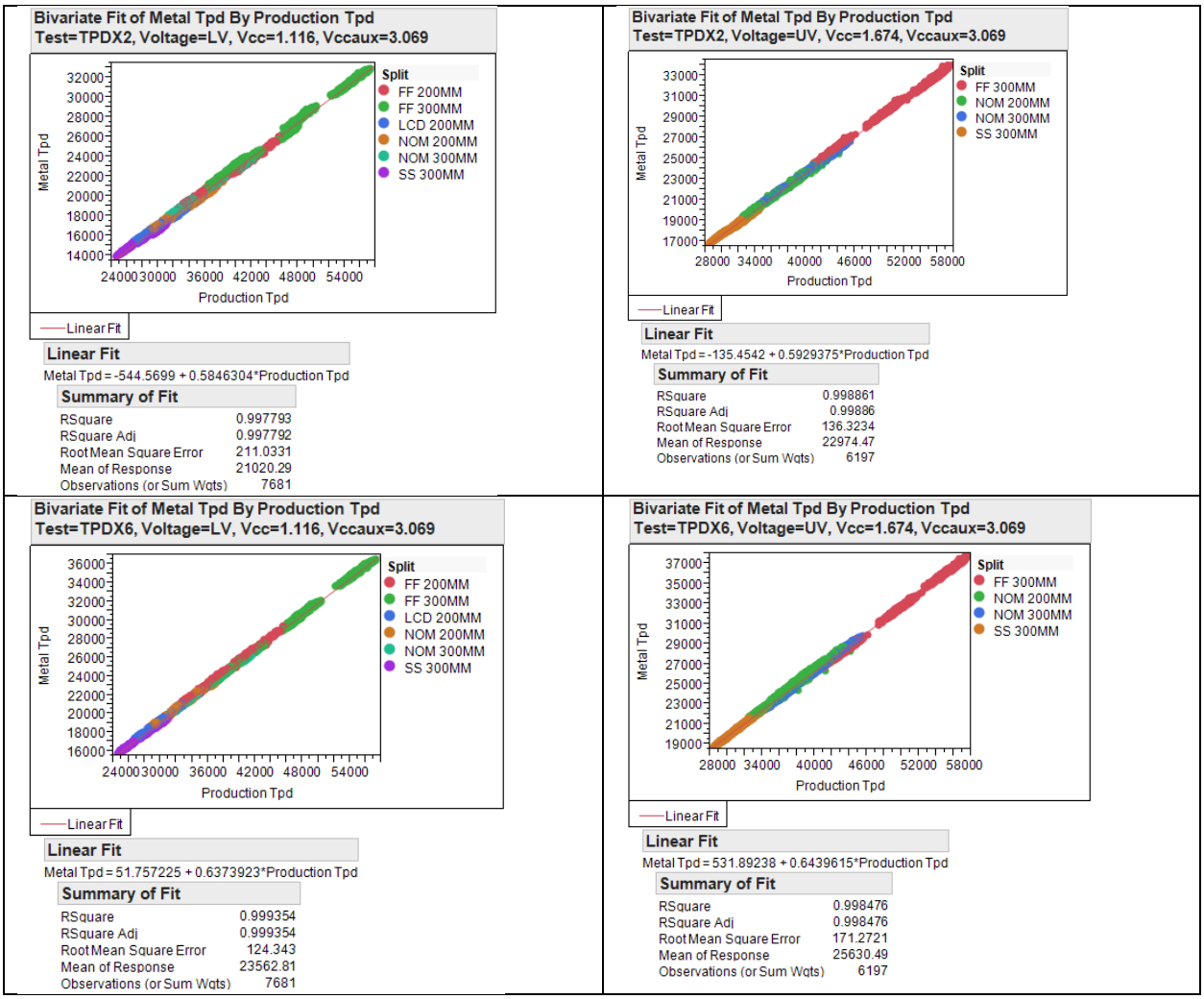
Manufacturing speed testing is done using BIST approach called a Tpdcounter. The idea is to create a ring oscillator that goes through as much of the FPGA fabric as possible and feed the result of that oscillator into a counter. The count after a specified period of time is known as the Tpdcount, which is highly correlated to other internal timings.

In addition to the production Tpdcounter, special characterization Tpdcounter patterns were created that focused specifically on certain routing paths. The X6 and X2 routing paths which are on specific metal layers in the layout were used to

1) Compare layer-layer capacitance
2) Compare 200mm vs 300mm speed performance

X2 and X6 Tpdcount values were plotted vs the more generic production Tpdcount for both UV and LV devices on both 200mm and 300mm processed wafers.

The extremely high Rsquared values show that there isn't a difference between the two routing paths between the 300mm and 200mm process.

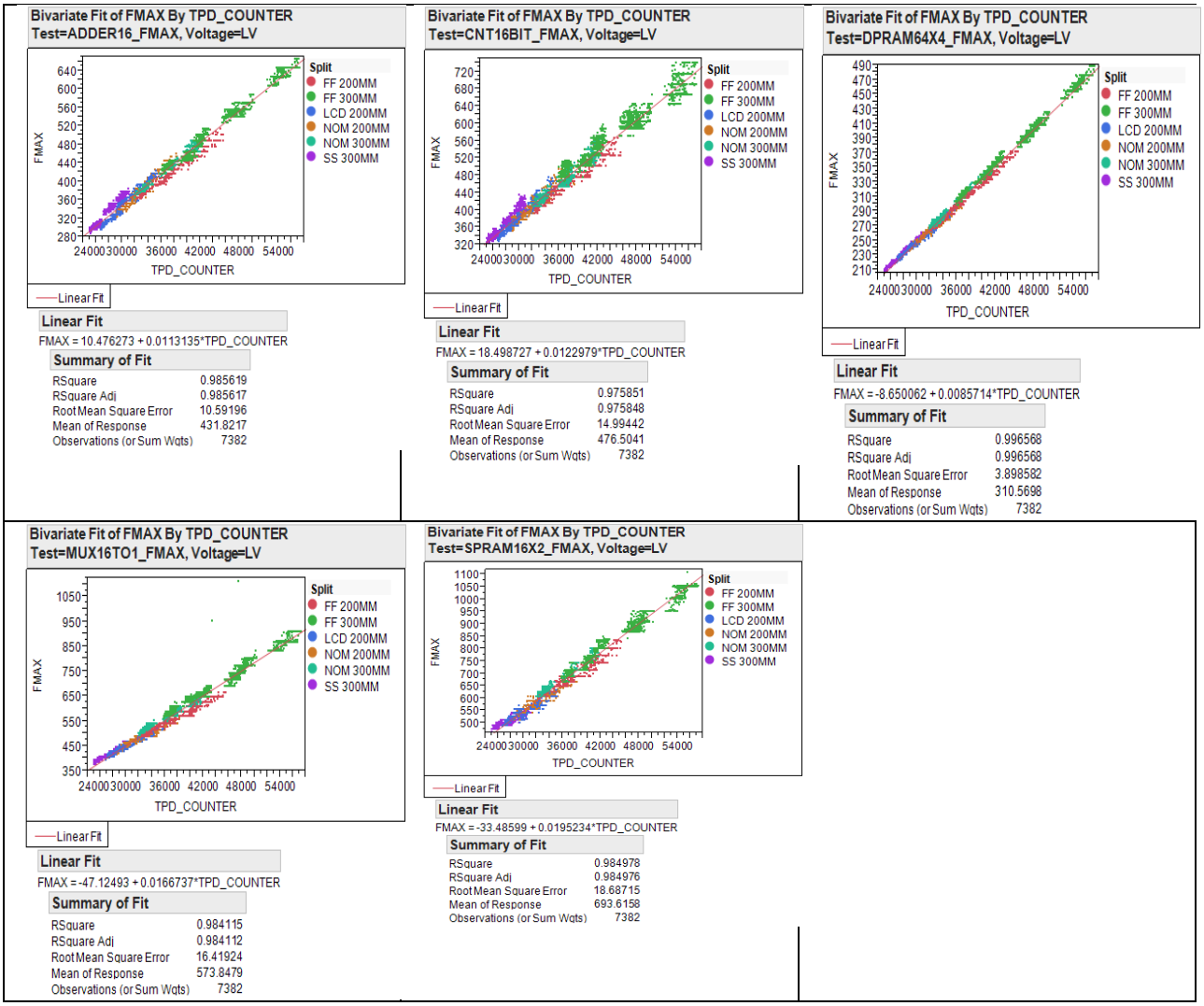


X2 and X6 Tpdcount vs Production Tpdcount Values

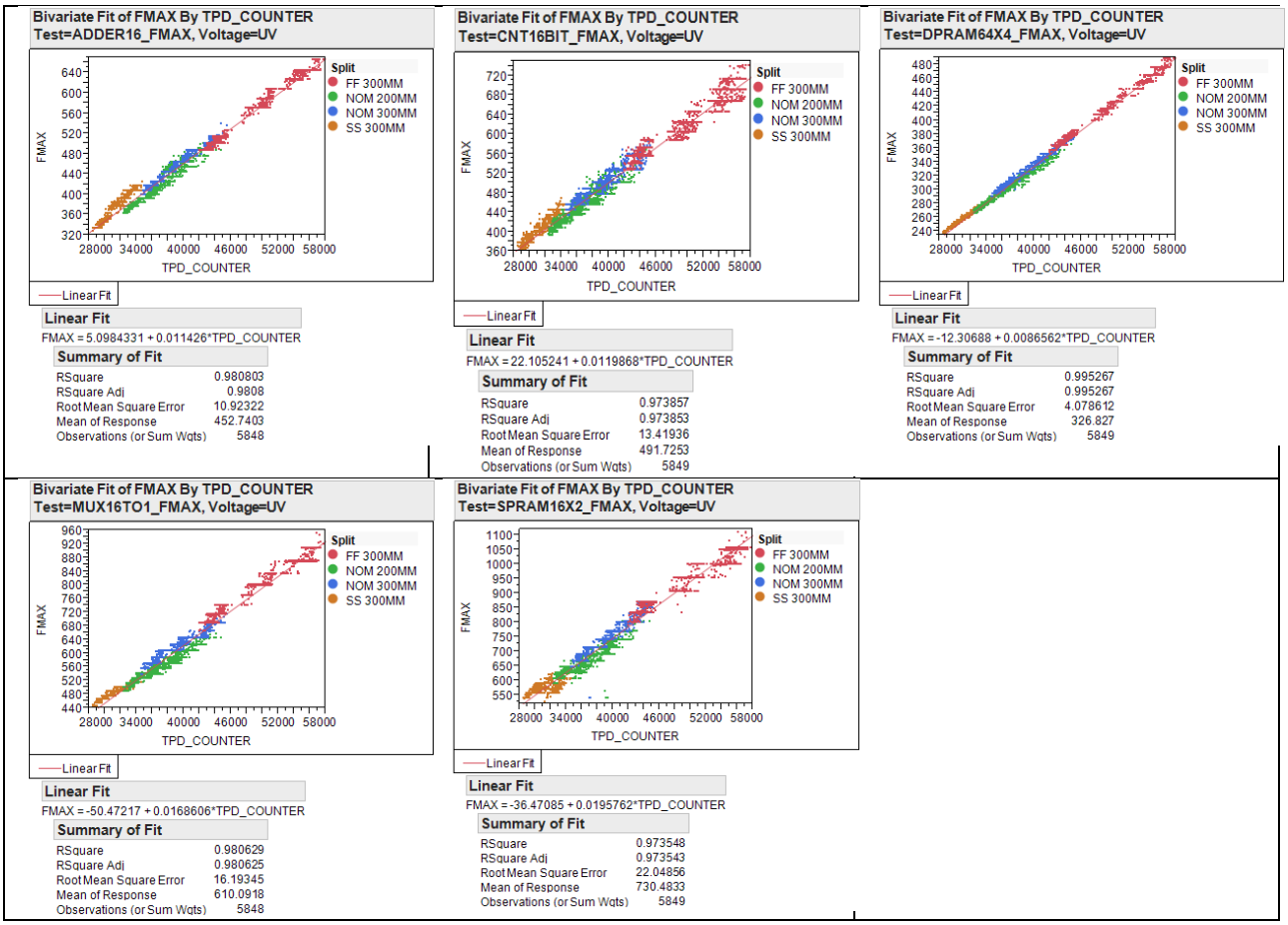
Building Block Performance

The Mach XO datasheet has a section called Typical Building Block Performance that lists the performance of various real-world applications. Those applications use a variety of chip resources including Embedded Block Ram in various configurations. Building block performance was plotted on a unit-by-unit basis for the production Tpdcount value for all process splits.

The correlation is excellent which is another indication that the performance of various routing paths, metal layer capacitance and EBR functions are all equivalent. This insures that the various components of system performance are identical and a part from the new 300mm process will respond the same as the older 200mm process.



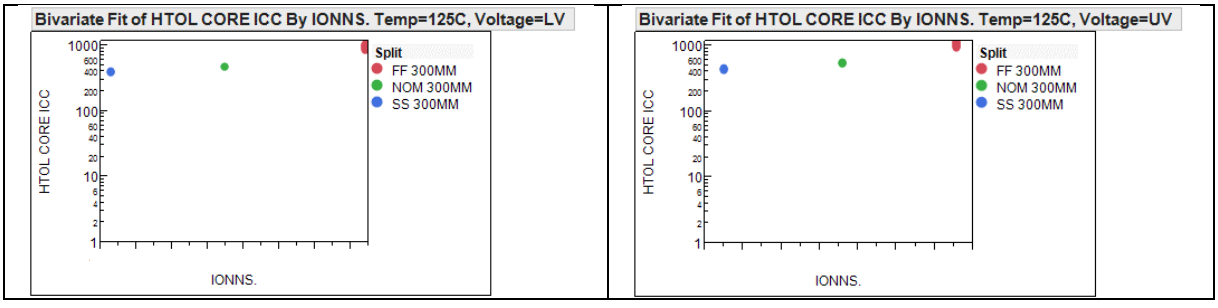
Building Block Performance (LV)

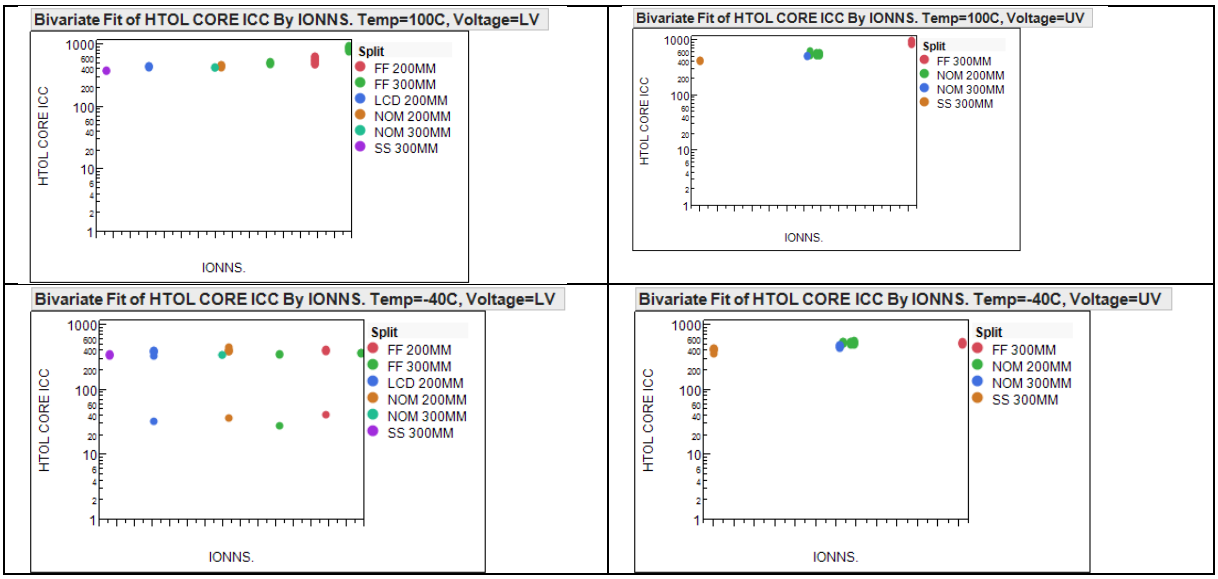


Building Block Performance (UV)

Power

Dynamic Icc at 100MHz was measured as a function of the E-Test parameter Ion. There is practically no difference between 200mm and 300mm process performance.





Dynamic Icc (100MHz) vs IonNS

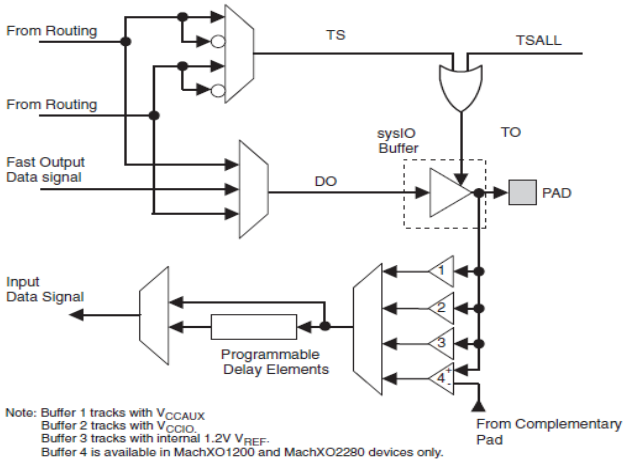
Flash Memory Characteristics

Flash memory data retention is tested in the production flow through two high temperature bake steps. The worst case cell threshold for all cells is measured pre- and post-bake in both erased and programmed state. The shift through the bake step is intended to weed out any leaky cells that might fail in the field. There was no issue with Vt shift measured in the programmed state for either 200mm or 300mm process. The maximum Vt shift for in the programmed state was measured at 0.02V.

Flash erase times were measured for all splits and no differences were seen. The flash performance of the 300mm process is equivalent to the production-released 200mm process.

External Timings

A key portion the unit-level characterization was the bench measurement of Tco/Tpd/Tsu/Thd parameters in the Programmable IO (PIO) using the primary clock tree. These measurements are the final word on comparing the timing performance of the 200mm process to that of the new 300mm process.



XO Programmable IO (PIO) Path

These parameters were tested over process, voltage and temperature (PVT) for both the 200mm and 300mm process splits. The two processes are identical for these external timing parameters.

PLL Performance

The PLL performance of the MachXO2280 was extensively tested during unit-level characterization. All PLL datasheet parameters were measured and checked across process, voltage and temperature (PVT). There is no difference between the 200mm and 300mm process performance.

PLL output jitter was also measured across PVT. All measurements less than datasheet specifications with no measureable difference between the two processes. Similarly, input clock jitter was well within specifications across PVT for both processes with no measureable differences. Overall, PLL performance between the two processes is identical.

IO Performance

Design Indices (DI, a measure similar to Cpk but calculated across multiple process splits) were calculated for 200mm and 300mm processes for DC Vol and Voh. The target DI is > 1 and the lowest DI calculated was 2.64, indicating plenty of margin to datasheet performance.

IO Fmax was also measured on the bench during unit characterization at 125C temperature across all process splits. DI was calculated at 2.58 for commercial temperatures and 1.46 at 125C, which also indicated plenty of margin to datasheet spec. 200mm and 300mm performance was identical.

IO Hotsocketing performance as measured by the Idk specification was characterized during unit characterization at maximum supply voltage conditions at both -55C and 125C. Idk was measured dynamically as function of time and statically as a function of Vin. There were no differences between the 200mm and 300mm process and both showed excellent margin to the datasheet specification.

The 300mm process performance was compared to the Diamond SW-supplied IBIS model. There are no differences and the existing IBIS model can be used safely with the new 300mm process.

Timing Adders

The unit-level characterization measured values for all the parameters in the Timing Adder section of the MachXO datasheet. The value of these adders shows how pin-to-pin timings change as a function of the programmed IO type. These adders are automatically compensated for in the Diamond timing SW. The timing adders indicate no difference between the 200mm and 300mm processes and no changes to Diamond SW is required.

Other Parameters

Design Indices (DI, a measure similar to Cpk but calculated across multiple process splits) were calculated for 200mm and 300mm processes for various datasheet parameters (Icc, Leakage, Vil, Vih, Vol, Voh) for comparison. No differences were found.

CONCLUSION

Electrical characterization of the new 300mm CS90F process was performed and no issues were discovered. Lattice recommends release of the Mach XO family at the Fujitsu 300mm production line.