H264-ENC1

H264-HD ENCODER IP

A high performance HD compression core IP that implements the H.264 (MPEG-4/AVC) video coding standard using the baseline/main/high profile up to level 4.1

Our core is designed to provide high compression levels while preserving image quality; this encoder can compress HD and SD video with high fidelity to minimal bitrate streams.

Superior quality video at low bit rates is achieved by using such features as our high performance motion estimation engine and intelligent macroblock skip.

Supported resolutions range from 64x64 pixels through 2048x2084, including standard resolutions such as QCIF, CIF, D1, 720p, etc...

An advanced frequency domain noise filtering algorithm uses statistics from motion estimation.

Very large search area (1024x512 pixel) can be covered through intelligent recursive motion estimation algorithm

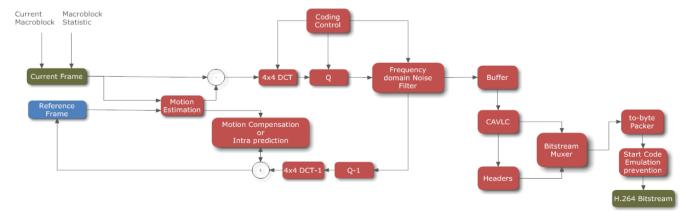
- Only 133MHz required for 1080p at 30fps compression
- > ~56K LUTs on Lattice ECP2-70/ ECP3-70 FPGA
- Very low latency
- All resolutions and frame rates supported
- ➤ Large 1024x512 motion estimation search range
- Bitrates from 64Kbit/s to 150Mbit/s
- ➤ H.264 baseline/main/high profile up to level 4.1
- > Lossless compression mode

Frame rates are only limited by clock frequency. At 133MHz 1920x1088 pictures can be processed at 30 frames per second.

Our core does not require an external CPU for operation. Optionally, a CPU can be used for encoder configuration or bitstream data transfer.

As the core operates at 133MHz for all HDTV resolutions, it can be easily implemented in a low cost FPGA.

Enciris encoder IP





Key Features

- Compliant with International Standard
 ISO/CEI MPEG-4 Part 10 (ISO/CEI 14496-10)
- h.264 baseline/main/high profile up to level 4.1
- Very low latency
 - Less than 3ms at 30fps
- Very efficient processing
 - Only 133MHz for 1920x1088@30fps
- Motion estimation
 - o 1024x512 full pel search range
 - o 1/4-pixel search (available soon)
 - Optional output of all Motion Vectors
- Bitrate control
 - Rate distortion optimization algorithm
 - VBR(variable bitrate) and CBR (constant bitrate) control
 - o From 64Kbit/s up to 150Mbit/s
- Entropy coding
 - o CAVLC
 - High throughput (400Mbits/sec on peak)
- Texture coding
 - 4x4 Precision forward DCT and inverse DCT and quantization
- Arbitrary resolutions supported
 - All standard resolutions such as QCIF, CIF, D1, 720P, 1080P
 - Any multiple of 16 resolution
- Lossless compression mode using quantization parameter 0
- In-loop frequency noise filter
- Fully synchronous design
- No CPU required for encoding
- Few internal memory resources
- 133MHz operation in low cost Lattice ECP2/M FPGA
- Available for ASIC

Applications

- Multimedia systems
- HDTV
- Digital video recorders
- Video Medical systems
- Video surveillance systems
- HDTV video cameras

Deliverables

- ❖ EDIF netlist
- RTL source code
- Complete test-bench
- Bit accurate C model
- Complete data sheet

Other IP's

- Motion estimation Core
- ❖ H.264 CODEC
- Video preprocessing
- Multiport DDR memory controller

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