Lattice MachXO Product Family Qualification Summary

Lattice Document # 25 - 106236 January 2015

Dear Customer,

Enclosed is Lattice Semiconductor's MachXO Product Family Qualification Report.

This report was created to assist you in the decision making process of selecting and using our products. The information contained in this report represents the entire qualification effort for this device family.

The information is drawn from an extensive qualification program of the wafer technology and packaging assembly processes used to manufacture our products. The program adheres to JEDEC and Automotive Industry standards for qualification of the technology and device packaging. This program ensures you only receive product that meets the most demanding requirements for Quality and Reliability.

Your feedback is valuable to Lattice. If you have suggestions to improve this report, or the data included, we encourage you to contact your Lattice representative.

Sincerely,

James M. Orr
Vice President,
Corporate Quality & Product Development
Lattice Semiconductor Corporation

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1.0 INTRODUCTION

The MachXO product family combines Flash and SRAM technology to provide "instant-on" capabilities in a single low-cost device. This combination of SRAM and Flash enables easy field updates via Lattice's unique TransFR technology.

The MachXO product family offers a flexible LUT (Look Up Table) architecture that provides 256 to 2280 LUTs and in multiple Thin Quad Flat Pack (TQFP), Fine-Pitch Thin BGA (ftBGA) and Chip Scale BGA (csBGA) packages with user I/O counts ranging from 78 to 271 I/Os. Table 1.1 shows the LUTs, package and I/O options, along with other key parameters.

Table 1.1 MachXO Product Family Attributes

	LCMXO256	LCMXO640	LCMXO1200	LCMXO2280
Vcc Voltage	1.2/1.8/2.5/3.3V	1.2/1.8/2.5/3.3V	1.2/1.8/2.5/3.3V	1.2/1.8/2.5/3.3V
LUTs	256	640	1200	2280
Density Macrocells*	128	320	600	1140
tPD (ns)	3.5	3.5	3.6	3.6
Fmax (MHz)	388	388	388	388
Dist RAM (Kbits)	2.0	6.0	6.25	7.5
EBR SRAM (Kbits)	0	0	9.2	27.6
Number of PLLs	0	0	1	2
Max. I/O	78	159	211	271
Die Fabrication Site	Fujitsu - Mie	Fujitsu - Mie	Fujitsu - Mie	Fujitsu - Mie
Fabrication Process Technology	0.13um CMOS	0.13um CMOS	0.13um CMOS	0.13um CMOS
Packages – I/O				
100-pin Lead-Free TQFP (14x14 mm)	78	74	73	73
144-pin Lead-Free TQFP (20x20 mm)		113	113	113
100-ball Lead-Free csBGA (8x8 mm)	78	74		
132-ball Lead-Free csBGA (8x8 mm)		101		
256-ball Lead-Free ftBGA (17x17 mm)		159	211	211
324-ball Lead-Free ftBGA (19x19 mm)				271

*Assumes 1 macrocell = 2 LUTs

The MachXO product family features Lattice's exclusive sysCLOCK PLLs, sysMEM embedded memory blocks (EBRs) and high-performance I/Os. The MachXO product family also offers flexible I/O buffers which supports with a wide range of interfaces including LVCMOS 3.3/2.5/1.8/1.5/1.2 LVTTL, PCI, LVDS, Bus-LVDS, LVPECL and RSDS. The MachXO product family is in-system programmable through the IEEE Standard 1532 interface. IEEE Standard 1149.1 boundary scan testing capability also allows product testing on automated test equipment.

The MachXO product family is built on CS90F (also known as EE12) process technology. The CS90F Process Technology is a 130 nm Flash CMOS process with low-k dielectric and copper metallization, fabricated by Fujitsu Limited. This process uses 8 planarized Cu metal interconnect layers, an Al top layer metal layer and a double layer poly-silicon flash cell. The CS90F process technology was originally qualified using qualification vehicles from the Lattice XP Product Family. Therefore, data from those devices are included in this report.

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2.0 LATTICE PRODUCT QUALIFICATION PROGRAM

Lattice Semiconductor Corp. maintains a comprehensive reliability qualification program to assure that each product achieves its reliability goals. After initial qualification, the continued high reliability of Lattice products is assured through ongoing monitor programs as described in Reliability Monitor Program Procedure (Doc. #70-101667). All product qualification plans are generated in conformance with Lattice Semiconductor's Qualification Procedure (Doc. #70-100164) with failure analysis performed in conformance with Lattice Semiconductor's Failure Analysis Procedure (Doc. #70-100166). Both documents are referenced in Lattice Semiconductor's Quality Assurance Manual, which can be obtained upon request from a Lattice Semiconductor sales office. Figure 2.1 shows the Product Qualification Process Flow.

If failures occur during qualification, an 8D process is used to find root cause and eliminate the failure mode from the design, materials, or process. The effectiveness of any fix or change is validated through additional testing as required. Final testing results are reported in the qualification reports.

Failure rates in this reliability report are expressed in FITs. Due to the very low failure rate of integrated circuits, it is convenient to refer to failures in a population during a period of 10^9 device hours; one failure in 10^9 device hours is defined as one FIT.

Product families are qualified based upon the requirements outlined in Tables 2.2. In general, Lattice Semiconductor follows the current Joint Electron Device Engineering Council (JEDEC) and Military Standard testing methods. Lattice automotive products are qualified and characterized to the Automotive Electronics Council (AEC) testing requirements and methods. Product family qualification will include products with a wide range of circuit densities, package types, and package lead counts. Major changes to products, processes, or vendors require additional qualification before implementation.

The Lattice MachXO product family is Lattice's second 130 nm Flash Technology based product offering. The LatticeXP product family was the initial 130 nm Flash Technology product line and as such was used as the primary technology qualification vehicle. The LatticeXP and MachXO product families are built on the same foundry line (Fujitsu Mie-323 200mm), using the same technology design rules, design methodology and share the same standard design library. In 2014 the very popular MachXO product family is transferring to an alternate foundry line (Fujitsu Mie-101 300mm) to assure a long term supply. This foundry line currently manufactures the LatticeXP2 product family.

Lattice Semiconductor maintains a regular reliability monitor program. The current Lattice Reliability Monitor Report can be found at Product Reliability Monitor Report.

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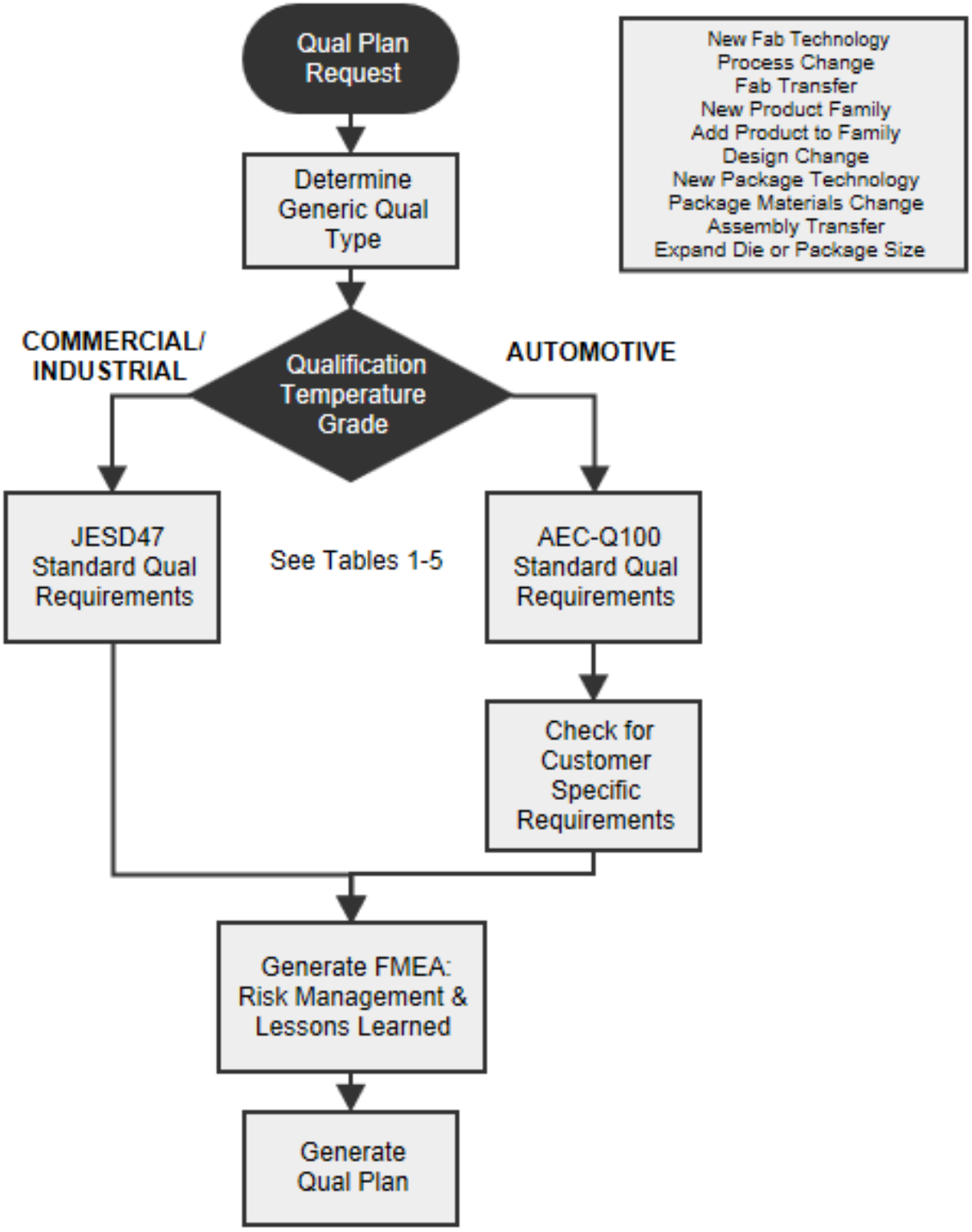
Figure 2.1 Lattice Standard Product Qualification Process Flow



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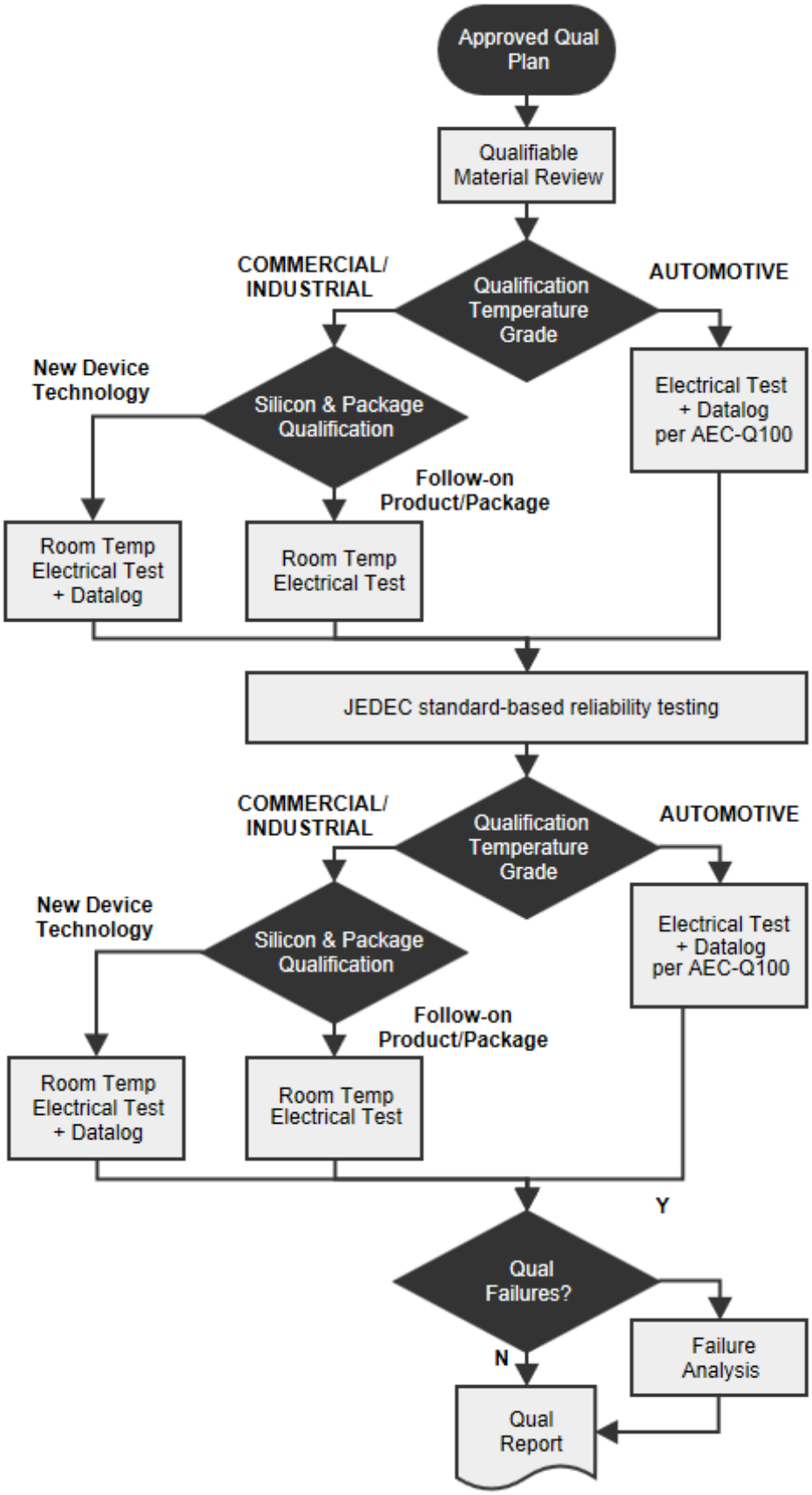

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Table 2.2 Standard Qualification Testing

TEST	STANDARD	TEST CONDITIONS	SAMPLE SIZE (Typ)	PERFORMED ON
High Temperature Operating Life HTOL	Lattice Procedure # 87-101943, JESD22-A108 Mach XO Mach XO2 LatticeXP	125° C, Maximum operating Vcc, 168, 500, 1000 hours Preconditioned with 1000 read/write cycles	77/lot 2 lots	Design, Foundry Process, Package Qualification
High Temp Data Retention HTRX	Lattice Procedure # 87-101925, JESD22-A103 JESD22-A117 Mach XO Mach XO2 LatticeXP	150° C, Maximum operating Vcc, 168, 500, 700 hrs. Preconditioned with 1000 read/write cycles	100/lot 2 lots	Design, Foundry Process, Package Qualification E^2 Cell Products Flash based Products
High Temp Storage Life HTSL	Lattice Procedure # 87-101925, JESD22-A103	150° C, at 168, 500, 1000 hours.	77/lot 2 lots	Design, Foundry Process, Package Qualification
Endurance - Program/Erase Cycling Flash based Products	Lattice Procedure, # 70-104633 JESD22-A117 MachXO LatticeXP	Program/Erase devices to 10,000 cycles	10/lot 2 lots typical	Design, Foundry Process, Package Qualification
ESD HBM	Lattice Procedure # 70-100844, JS-001-2012	Human Body Model (HBM) sweep to 2000V (130nm and older)	3 parts/lot 1-3 lots typical	Design, Foundry Process
ESD CDM	Lattice Procedure # 70-100844, JESD22-C101	Charged Device model (CDM) sweep to 1000V (130nm and older)	3 parts/lot 1-2 lots typical	Design, Foundry Process
Latch Up Resistance LU	Lattice Procedure # 70-101570, JESD78	±100 ma on I/O's, Vcc +50% on Power Supplies. (Max operating temperature)	6 parts/lot 1-2 lots typical	Design, Foundry Process
Surface Mount Pre-conditioning SMPC	Lattice Procedure # 70-103467, IPC/JEDEC J-STD-020D.1 JESD-A113 CPLD/FPGA - MSL 3	10 Temp cycles, 24 hr 125° C Bake 192hr. 30/60 Soak 3 SMT simulation cycles	All units going into Temp Cycling, UHAST, BHAST, 85/85	Plastic Packages only
Temperature Cycling TC	Lattice Procedure #70-101568, JESD22-A104	(700 or 1000 cycles) Repeatedly cycled between -55° C and +125° C in an air environment	45 parts/lot 2 lots	Design, Foundry Process, Package Qualification

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Unbiased HAST UHAST	Lattice Procedure # 70-104285 JESD22-A118	2 atm. Pressure, 96 hrs, 130 C, 85% Relative Humidity	45 parts/lot 2 lots	Foundry Process, Package Qualification Plastic Packages only
Moisture Resistance Temperature Humidity Bias 85/85 THB or Biased HAST (BHAST)	Lattice Procedure # 70-101571, JESD22-A101 JESD22-A110	Biased to maximum operating Vcc, 85° C, 85% Relative Humidity, 1000 hours or Biased to maximum operating Vcc, 2atm. Pressure, 96 hrs, 130 C, 85% Relative Humidity	45 devices/lot 2 lots	Design, Foundry Process, Package Qualification Plastic Packages only
Physical Dimensions	Lattice Procedure # 70-100211, MIL-STD- 883 Method 2016 or applicable LSC case outline drawings	Measure all dimensions listed on the case outline.	5 devices	Package Qualification
Wire Bond Strength	Lattice Procedure # 70-100220	6 gr. min. for 1.25 mil gold wire	15 devices per pkg. per year	Design, Foundry Process, Package Qualification
Solderability	Lattice Procedure # 70-100212, MIL-STD-883, Method 2003	Steam Pre-conditioning 4-8 hours. Solder dip at 245°C+5°C	22 leads/ 3 devices/ Package family/	All packages except BGAs

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3.0 QUALIFICATION DATA FOR CS90F PROCESS TECHNOLOGY

The Lattice MachXO product family is the Lattice's second 130 nm Flash Technology based product offering. The LatticeXP product family was the initial 130 nm Flash Technology product line and as such was used as the primary technology qualification vehicle in the Fujitsu Mie-323 200mm foundry, using the same technology design rules, design methodology and share the same standard design library. In 2014 the very popular MachXO product family is transferring to an alternate foundry line (Fujitsu Mie-101 300mm) to assure a long term supply. This foundry line currently manufactures the Flash Technology based LatticeXP2 product family.

Product Family: MachXO, LFXP
Packages offered: ftBGA, csBGA, fpBGA, PQFP and TQFP
Process Technology Node: 130nm

3.1 MachXO Product Family Life Data

High Temperature Operating Life (HTOL) Test

The High Temperature Operating Life test is used to thermally accelerate those wear out and failure mechanisms that would occur as a result of operating the device continuously in a system application. Consistent with JEDEC JESD22-A108 "Temperature, Bias, and Operating Life", a pattern specifically designed to exercise the maximum amount of circuitry is programmed into the device and this pattern is continuously exercised at specified voltages as described in test conditions for each device type.

CS90F Life Test (HTOL) Conditions:
Stress Duration: 168, 500, 1000 (qual complete) hours; 1500 & 2000 (extended stress) hours
Temperature: 125°C
Stress Voltage MachXO (LCMXO): V_{CC}=1.26V (E) or 3.47V (C) / V_{CCIO}=3.47V
Stress Voltage LAMachXO (LA-MXO): V_{CC}=1.26V (E) or 3.47V (C) / V_{CCIO}=3.47V
Stress Voltage LatticeXP (LFXP): V_{CC}=1.26V/ V_{CCIO}=3.47V, V_{CC}=2.5V/ V_{CCIO}=3.47V
Preconditioned with 1000 read/write cycles
Method: Lattice Document # 87-101943 and JESD22-A108D

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Table 3.1.1 MachXO Product Family (CS90F) Life Results

Product Name	Wafer Fab	Lot #	Qty	168 Hrs Result	500 Hrs Result	1000 Hrs Result	1500 Hrs Result	2000 Hrs Result	Cumulative Hours
LCMXO2280C	Mie-101	Lot #1	78	0	NA	NA	NA	NA	13,104
LCMXO2280E	Mie-101	Lot #1	84	0	0	0	NA	NA	84,000
LCMXO2280E	Mie-101	Lot #2	85	0	0	0	NA	NA	85,000
LCMXO2280E	Mie-101	Lot #3	85	0	0	0	NA	NA	85,000
LCMXO640E	Mie-323	Lot #1	44	0	0	0	NA	0	88,000
LCMXO640C	Mie-323	Lot #1	44	0	0	0	NA	0	88,000
LCMXO640E	Mie-323	Lot #2	44	0	0	0	NA	0	88,000
LCMXO640C	Mie-323	Lot #2	44	0	0	0	NA	0	88,000
LCMXO640E	Mie-323	Lot #3	40	0	0	0	NA	0	80,000
LCMXO640C	Mie-323	Lot #3	40	0	0	0	NA	0	80,000
LCMXO256E	Mie-323	Lot #1	38	0	0	0	NA	0	76,000
LCMXO256C	Mie-323	Lot #1	38	0	0	0	NA	0	76,000
LCMXO256E	Mie-323	Lot #2	38	0	0	0	NA	0	76,000
LCMXO256C	Mie-323	Lot #2	38	0	0	0	NA	0	76,000
LFXP10C	Mie-323	Lot #A	70	0	0	0	NA	NA	70,000
LFXP10C	Mie-323	Lot #B	50	0	0	0	0	0	100,000
LFXP10C	Mie-323	Lot #C	75	0	0	0	0	0	150,000
LFXP10E	Mie-323	Lot #D	59	0	0	0	0	N/A	88,500
LFXP10E	Mie-323	Lot #E	35	0	0	0	0	0	70,000
LFXP3E	Mie-323	Lot #1	76	0	0	0	0	0	152,000
LFXP3E	Mie-323	Lot #2	75	0	0	0	0	0	150,000
LAMXO256C	Mie-323	Lot #9	79	0	0	0	NA	NA	79,000
LAMXO256E	Mie-323	Lot# 10	78	0	0	0	NA	NA	78,000
LAMXO640E	Mie-323	Lot #12	80	0	0	0	NA	NA	80,000

CS90F Cumulative Device Hours = 2,100,604
CS90F Cumulative Sample Size = 0 / 1,417
CS90F FIT Rate = 6 FIT

MachXO Cumulative Result = 0 / 740
LatticeXP Cumulative Result = 0 / 440
LAMachXO Cumulative Result = 0 / 237

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3.2 MachXO Product Family High Temperature Retention (HTRX) Data

High Temperature Data Retention (HTRX)

The High Temperature Data Retention test measures the Flash cell reliability while the High Temperature Operating Life test is structured to measure functional operating circuitry failure mechanisms. The High Temperature Data Retention test is specifically designed to accelerate charge gain on to or charge loss off of the floating gates in the device's array. Since the charge on these gates determines the actual pattern and function of the device, this test is a measure of the reliability of the device in retaining programmed information. In High Temperature Data Retention, the Flash cell reliability is determined by monitoring the cell margin after biased static operation at 150°C. All cells in all arrays are life tested in both programmed and erased states. Prior to data retention testing all products are pre-conditioned to the maximum data sheet conditions program/erase cycles.

The High Temperature Storage Life (HTSL) test is used to determine the effect of time and temperature, under storage conditions, for thermally activated failure mechanisms. For the non-volatile based products, the HTRX and HTSL stress and test conditions condition are the same. The HTSL test is covered by HTRX.

CS90F Data Retention (HTRX) Conditions:

Stress Duration: 168, 500, 1000 hours.

Temperature: 150°C

Stress Voltage MachXO (LCMXO): V_{CC}=1.3V (E) or 3.6V (C) / V_{CCIO}=3.6V

Stress Voltage LAMachXO (LA-MXO): V_{CC}=1.3V (E) or 3.6V (C) / V_{CCIO}=3.6V

Stress Voltage LatticeXP (LFXP): V_{CC}=1.26V/ V_{CCIO}=3.6V, V_{CC}=2.5V/ V_{CCIO}=3.6V

Stress Voltage LatticeXP2 (LFXP2): V_{CC}=1.26V/ V_{CCIO}=3.6V, V_{CC}=2.5V/ V_{CCIO}=3.6V

Method: Lattice Document # 87-101925 and JESD22-A103D / JESD22-A117C

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Table 3.2.1 CS90F High Temperature Retention Results

Product Name	Wafer Fab	Package Type	Assembly Site	Lot #	Qty	168 Hrs Result	500 Hrs Result	1000 Hrs Result	1500 Hrs Result	2000 Hrs Result	Cumulative Hours
LCMXO2280C	Mie-101	324 ftBGA	ASEM	Lot #1*	28	0	0	0	NA	NA	28,000
LCMXO2280C	Mie-101	324 ftBGA	ASEM	Lot #2*	28	0	0	0	NA	NA	28,000
LCMXO2280C	Mie-101	324 ftBGA	ASEM	Lot #3*	28	0	0	0	NA	NA	28,000
LCMXO2280E	Mie-101	100 TQFP	ASEM	Lot #1*	27	0	0	0	NA	NA	27,000
LCMXO2280E	Mie-101	100 TQFP	ASEM	Lot #2*	27	0	0	0	NA	NA	27,000
LCMXO2280E	Mie-101	100 TQFP	ASEM	Lot #3*	27	0	0	0	NA	NA	27,000
LAXP2-17E	Mie-323	256 ftBGA	ASEM	Lot #1**	69	0	0	0	NA	NA	69,000
LAXP2-17E	Mie-323	256 ftBGA	ASEM	Lot #8**	100	0	0	0	NA	NA	100,000
LAXP2-17E	Mie-323	256 ftBGA	ASEM	Lot #9**	80	0	0	0	NA	NA	80,000
LAXP2-17E	Mie-323	256 ftBGA	ASEM	Lot #10**	80	0	0	0	NA	NA	80,000
LFXP2-40E	Mie-323	672 fpBGA	ASEM	Lot #1**	80	0	0	0	NA	NA	80,000
LFXP2-8E	Mie-323	144 TQFP	ASEM	Lot #1***	46	0	0	0	NA	NA	46,000
LFXP2-5E	Mie-323	144 TQFP	ASEM	Lot #1***	80	0	0	0	NA	NA	80,000
LFXP2-5E	Mie-323	144 TQFP	ASEM	Lot #2***	80	0	0	0	NA	NA	80,000
LAXP2-5E	Mie-323	208 PQFP	ASEM	Lot #1***	80	0	0	0	NA	NA	80,000
LAXP2-5E	Mie-323	208 PQFP	ASEM	Lot #2***	80	0	0	0	NA	NA	80,000
LAXP2-5E	Mie-323	208 PQFP	ASEM	Lot #3***	77	0	0	0	NA	NA	77,000
LCMXO640C	Mie-323	256 fpBGA	ASEM	Lot #1***	88	0	0	0	NA	NA	88,000
LCMXO640C	Mie-323	256 fpBGA	ASEM	Lot #2***	88	0	0	0	NA	NA	88,000
LFXP10C	Mie-323	388 fpBGA	ASEM	Lot #3***	148	0	0	0	0	0	296,000
LFXP10C	Mie-323	388 fpBGA	ASEM	Lot #6***	150	0	0	0	0	0	300,000
LFXP10C	Mie-323	388 fpBGA	ASEM	Lot #7***	55	0	0	0	0	0	110,000
LAMXO256C	Mie-323	100 TQFP	ASEM	Lot #9***	80	0	0	0	NA	NA	80,000
LAMXO256E	Mie-323	100 TQFP	ASEM	Lot# 10***	80	0	0	0	NA	NA	80,000
LAMXO640E	Mie-323	256 fpBGA	ASEM	Lot #12***	78	0	0	0	NA	NA	78,000

* These lots have copper (Cu) wire bonds & stressed as High Temperature Storage Life (150°C bake – NVM cells erased).
** These lots have gold (Au) wire bonds & stressed as High Temperature Data Retention (150°C bake– NVM cells 50/50 programmed & erased).
*** These lots have gold (Au) wire bonds & stressed as High Temperature Storage Life (150°C bake – NVM cells erased).

CS90F Cumulative HTRX Failure Rate = 0 / 1,784

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3.3 MachXO Product Family Endurance Cycling Data

Endurance testing measures the durability of the device through programming and erase cycles. Endurance testing consists of repeatedly programming and erasing all cells in the array at 25°C to simulate programming cycles the user would perform. This test evaluates the integrity of the thin tunnel oxide through which current passes to program the floating gate in each cell of the array.

CS90F Endurance Test Conditions:

Stress Duration: 1K, 2K, 3K, 5K, 10K Cycles

Stress Voltage MachXO (LCMXO): V_{CC}=3.6V/ V_{CCIO}=3.6V

Stress Voltage LatticeXP (LFXP): V_{CC}=2.5V/ V_{CCIO}=3.6V

Method: Lattice Document # 70-104633 and JESD22-A117A

Table 3.3.1 CS90F Flash Endurance Cycling Results

Product Name	Wafer Fab	Lot #	Qty	1K CYC Result	2K CYC Result	3K CYC Result	5K CYC Result	10K CYC Result	Cumulative Cycles
LCMXO2280E	Mie-101	Lot #1	79	0	0	0	0	0	790,000
LCMXO640C	Mie-323	Lot #3	24	0	0	0	0	0	240,000
LFXP10C	Mie-323	Lot #6	10	0	0	0	0	0	100,000
LFXP10C	Mie-323	Lot #7	10	0	0	0	0	0	100,000

CS90F Cumulative Endurance Failure Rate = 0 / 123
CS90F Cumulative Endurance Cycles = 1,230,000

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3.4 MachXO Product Family – ESD and Latch UP Data

Electrostatic Discharge-Human Body Model:

MachXO (LCMXO) product family was tested per the JS-001-2012 Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM) procedure and Lattice Procedure # 70-100844.

All units were tested at 25°C and +105°C prior to reliability stress and after reliability stress. No failures were observed within the passing classification.

Table 3.4.1 MachXO (LCMXO) ESD-HBM Data

Product/Package	100 TQFP	144 TQFP	100 csBGA	132 csBGA	256 ftBGA	324 ftBGA
LCMXO2280C	> 2KV Class 2*			>1.8KV Class 1C*	> 2KV Class 2*	> 2KV Class 2*
LCMXO2280E	QBS > 2KV Class 2			QBS > 2KV Class 2	QBS > 2KV Class 2	> 2KV Class 2
LCMXO1200C	> 2KV Class 2*	> 2KV Class 2*		>1.9KV Class 1C*	> 2KV Class 2*	
LCMXO1200E	> 2KV Class 2*	> 2KV Class 2*		> 2KV Class 2*	> 2KV Class 2*	
LCMXO640C	QBS > 2KV Class 2		QBS > 2KV Class 2		> 2KV Class 2	
LCMXO640E	QBS > 2KV Class 2		QBS > 2KV Class 2		> 2KV Class 2	
LCMXO256C	> 2KV Class 2					
LCMXO256E	> 2KV Class 2		QBS > 2KV Class 2			

*Current HBM results based on the Mie-323 wafer fab. The Mie-101 wafer fab results Q1'15.
HBM classification for Commercial/Industrial products, per JS-001-2012
All HBM levels indicated are dual-polarity (±)
Each device (unique silicon mask set) is Qualified-by-similarity (QBS) from one of the device/package combinations

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Electrostatic Discharge-Charged Device Model:

MachXO (LCMXO) product family was tested per the JESD22-C101F, Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components procedure and Lattice Procedure # 70-100844.

All units were tested at 25°C and +105°C prior to reliability stress and after reliability stress. No failures were observed within the passing classification.

Table 3.4.2 MachXO (LCMXO) ESD-CDM Data

Product/Package	100 TQFP	144 TQFP	100 csBGA	132 csBGA	256 ftBGA	324 ftBGA
LCMXO2280C	QBS Class 3			QBS Class 3	QBS Class 3	> 1KV Class 3
LCMXO2280E	QBS Class 3			QBS Class 3	QBS Class 3	> 1KV Class 3
LCMXO1200C	QBS Class 3	QBS Class 3		QBS Class 3	> 1KV Class 3	
LCMXO1200E	QBS Class 3	QBS Class 3		QBS Class 3	> 1KV Class 3	
LCMXO640C	QBS Class 3		QBS Class 3		> 1KV Class 3	
LCMXO640E	QBS Class 3		QBS Class 3		> 1KV Class 3	
LCMXO256C	> 1KV Class 3					
LCMXO256E	>1KV Class 3		QBS Class 3			

CDM classification for Commercial/Industrial products, per JESD22-C101F
All CDM levels indicated are dual-polarity (±)
Each device (unique silicon mask set) is Qualified-by-similarity (QBS) from one of the device/package combinations

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Latch-Up:

MachXO (LCMXO) product family was tested per the JEDEC EIA/JESD78 IC Latch-up Test procedure and Lattice Procedure # 70-101570.

All units were tested at 25°C and +105°C prior to reliability stress and after reliability stress. No failures were observed within the passing classification.

Table 3.4.3 MachXO (LCMXO) I/O Latch Up Data

Product/Package	100 TQFP	144 TQFP	100 csBGA	132 csBGA	256 ftBGA	324 ftBGA
LCMXO2280C	QBS Class II			QBS Class II	QBS Class II	>+/-100mA Class II
LCMXO2280E	QBS Class II			QBS Class II	QBS Class II	>+/-100mA Class II
LCMXO1200C	QBS Class II	QBS Class II		QBS Class II	>+/-100mA Class II	
LCMXO1200E	QBS Class II	QBS Class II		QBS Class II	>+/-100mA Class II	
LCMXO640C	QBS Class II		QBS Class II		>+/-100mA Class II	
LCMXO640E	QBS Class II		QBS Class II		>+/-100mA Class II	
LCMXO256C	>+/-100mA Class II					
LCMXO256E	>+/-100mA Class II		QBS Class II			

I-Test LU classification for Commercial/Industrial products, per JESD78
All IO-LU levels indicated are dual-polarity (±)
Latch Up Classification: The two main classes are Class I for latch-up at room-temperature and Class II for Latch-Up at the maximum-rated ambient temperature
Each device (unique silicon mask set) is Qualified-by-similarity (QBS) from one of the device/package combinations

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Table 3.4.4 MachXO (LCMXO) Power Supply Over-Voltage Latch-Up Data

Product/Package	100 TQFP	144 TQFP	100 csBGA	132 csBGA	256 ftBGA	324 ftBGA
LCMXO2280C	QBS Class II			QBS Class II	QBS Class II	>1.5xVcc Class II
LCMXO2280E	QBS Class II			QBS Class II	QBS Class II	>1.5xVcc Class II
LCMXO1200C	QBS Class II	QBS Class II		QBS Class II	>1.5xVcc Class II	
LCMXO1200E	QBS Class II	QBS Class II		QBS Class II	>1.5xVcc Class II	
LCMXO640C	QBS Class II		QBS Class II		>1.5xVcc Class II	
LCMXO640E	QBS Class II		QBS Class II		>1.5xVcc Class II	
LCMXO256C	>1.5xVcc Class II					
LCMXO256E	>1.5xVcc Class II		QBS Class II			

Power Supply Over-Voltage Latch-Up LU classification for Commercial/Industrial products, per JESD78D
Latch-Up Classification: The two main classes are Class I for latch-up at room-temperature and Class II for Latch-Up at the maximum-rated ambient temperature.
Each device (unique silicon mask set) is Qualified-by-similarity (QBS) from one of the device/package combinations

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4.0 PACKAGE QUALIFICATION DATA FOR MACHXO PRODUCT FAMILY

The MachXO and LFXP product family is offered in ftBGA, csBGA, fpBGA PQFP and TQFP packages. To cover the range of die in the largest package types for this product family, different package and die combinations were chosen as the generic qualification vehicles for all the package qualification tests including, Temperature Cycling (T/C), Un-biased HAST (UHAST)and Biased HAST (BHAST). Mechanical evaluation tests include Scanning Acoustic Tomography (SAT) and visual package inspection.

The generation and use of generic data is applied across a family of products or packages emanating from one base wafer foundry or assembly process is a Family Qualification, or Qualification-By-Similarity. For the package stresses BHAST and UHAST, these are considered generic for a given Package Technology. T/C is considered generic up to an evaluated die size + package size + 10%, for a given Package Technology. Surface Mount Pre-Conditioning (SMPC) is considered generic up to an evaluated Peak Reflow temperature, for a given Package Technology. The following table demonstrates the package qualification matrix.

Table 4.0 Product-Package Qualification-By-Extension Matrix

<table>
<tr><th rowspan="2">Products</th><th rowspan="2">Stress Test</th><th colspan="2">ASEM / ATK / UTAC
Leaded Packages</th><th colspan="4">ASEM / ATP / UTAC
Saw-singulated BGA Packages</th></tr>
<tr><th>100-TQFP</th><th>144-TQFP</th><th>100-csBGA</th><th>132-csBGA</th><th>256-ftBGA</th><th>324-ftBGA</th></tr>
<tr><td rowspan="4">LCMXO-2280C/E</td><td>SMPC</td><td>260°C</td><td>260°C</td><td rowspan="8"></td><td>260°C</td><td rowspan="8">(3)</td><td>260°C</td></tr>
<tr><td>T/C</td><td>700/1K cyc</td><td>700/1K cyc</td><td>700/1K cyc</td><td>700/1K cyc</td></tr>
<tr><td>BHAST</td><td>96 hours</td><td>96 hours</td><td rowspan="2">130°C/96hr, 110°C/264hr</td><td rowspan="2">130°C/96hr, 110°C/264hr</td></tr>
<tr><td>UHAST</td><td>96 hours</td><td>96 hours</td></tr>
<tr><td rowspan="4">LCMXO-1200C/E</td><td>SMPC</td><td rowspan="8">(1)</td><td rowspan="4">(2)</td><td rowspan="4">(3)</td><td rowspan="8"></td></tr>
<tr><td>T/C</td></tr>
<tr><td>BHAST</td></tr>
<tr><td>UHAST</td></tr>
<tr><td rowspan="4">LCMXO-640C/E</td><td>SMPC</td><td>260°C</td><td rowspan="4">(3)</td><td>260°C</td><td rowspan="4">(3)</td></tr>
<tr><td>T/C</td><td>700/1K cyc</td><td>700/1K cyc</td></tr>
<tr><td>BHAST</td><td>96 hours</td><td rowspan="2">130°C/96hr, 110°C/264hr</td></tr>
<tr><td>UHAST</td><td>96 hours</td></tr>
<tr><td rowspan="4">LCMXO-256C/E</td><td>SMPC</td><td>260°C</td><td rowspan="4"></td><td>260°C</td><td rowspan="4"></td><td rowspan="4"></td></tr>
<tr><td>T/C</td><td>1000 cycles</td><td>1000 cycles</td></tr>
<tr><td>BHAST</td><td rowspan="2">(1)</td><td rowspan="2">(3)</td></tr>
<tr><td>UHAST</td></tr>
</table>

1 – Qualified-by-similarity (QBS) from the 100TQFP Package and the 144TQFP Package
2 – Qualified-by-similarity (QBS) from the LCMXO-1200 144TQFP and the LCMXO-2280 144TQFP (largest die/package combination)
3 – Qualified-by-similarity (QBS) from the LCMXO-2280 324-ftBGA (largest die/package combination)

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4.1 MachXO Product Family Surface Mount Preconditioning Testing

The Surface Mount Preconditioning (SMPC) Test is used to model the surface mount assembly conditions during component solder processing. All devices stressed through Temperature Cycling, Un-biased HAST and Biased HAST were preconditioned. This preconditioning is consistent with JEDEC JESD22-A113F "Preconditioning Procedures of Plastic Surface Mount Devices Prior to Reliability Testing", Moisture Sensitivity Level 3(MSL3) package moisture sensitivity and dry-pack storage requirements.

Surface Mount Preconditioning (MSL3)

(10 Temperature Cycles, 24 hours bake @ 125°C, 30°C/60% RH, soak 192 hours, 225/245/250/260°C Reflow Simulation, 3 passes) performed before all CS90F package tests.

MSL3 Packages: TQFP, PQFP, fpBGA, ftBGA, csBGA

Method: Lattice Procedure # 70-103467, J-STD-020D.1, JESD22-B101B; JESD22-A113F, and JESD22-A104D

Table 4.1.1 Surface Mount Precondition Data

Product Name	Package	Assembly Site	Lot Number	Quantity	# of Fails	Reflow Temperature
LCMXO2280C	132 csBGA	ASEM	Lot #1*	30	0	260°C
LCMXO2280C	132 csBGA	ASEM	Lot #2*	30	0	260°C
LCMXO2280C	132 csBGA	ASEM	Lot #3*	30	1[A]	260°C
LCMXO2280C	324 ftBGA	ASEM	Lot #1*	104	0	260°C
LCMXO2280C	324 ftBGA	ASEM	Lot #2*	84	0	260°C
LCMXO2280C	324 ftBGA	ASEM	Lot #3*	84	0	260°C
LCMXO2280E	100 TQFP	ASEM	Lot #1*	84	0	260°C
LCMXO2280E	100 TQFP	ASEM	Lot #2*	84	0	260°C
LCMXO2280E	100 TQFP	ASEM	Lot #3*	84	0	260°C
LCMXO2280E	144 TQFP	ASEM	Lot #1*	30	0	260°C
LCMXO2280E	144 TQFP	ASEM	Lot #2*	30	0	260°C
LCMXO2280E	144 TQFP	ASEM	Lot #3*	30	0	260°C
LFXP3E	100 TQFP	ASEM	Lot #1**	45	0	260°C
LFXP3E	208 PQFP	ASEM	Lot #3**	45	0	245°C
LFXP10C	256 fpBGA	ASEM	Lot #13**	32	0	250°C
LFXP10C	256 fpBGA	ASEM	Lot #14**	17	0	250°C
LFXP10C	256 fpBGA	ASEM	Lot #15**	3	0	250°C
LFXP10E	256 fpBGA	ASEM	Lot #16**	40	0	250°C
LCMXO2280	256 ftBGA	ASEM	Lot #1**	45	0	260°C
LCMXO2280	256 ftBGA	ASEM	Lot #2**	45	0	260°C
LFXP10E	388 fpBGA	ASEM	Lot #2**	135	0	250°C
LFXP10E	388 fpBGA	ASEM	Lot #5**	135	0	250°C
LFXP10E	388 fpBGA	ASEM	Lot #8**	45	0	250°C
LFXP10C	388 fpBGA	ASEM	Lot #9**	25	0	250°C
LFXP10C	388 fpBGA	ASEM	Lot #10**	14	0	250°C
LFXP10C	388 fpBGA	ASEM	Lot #11**	26	0	250°C
LFXP10C	388 fpBGA	ASEM	Lot #12**	28	0	250°C

Product Name	Package	Assembly Site	Lot Number	Quantity	# of Fails	Reflow Temperature
LCMXO256C	100 TQFP	ATK	Lot #1**	45	0	260°C
LCMXO256C	100 TQFP	ATK	Lot #2**	45	0	260°C
LAMXO640C	144 TQFP	ATK	Lot #1**	241	0	260°C
LAMXO640C	144 TQFP	ATK	Lot #2**	240	0	260°C
LAMXO2280E	144 TQFP	ATK	Lot #3**	233	0	260°C
LAMXO2280E	144 TQFP	ATK	Lot #4**	217	0	260°C
LCMXO256C	100 csBGA	ATP	Lot #3**	45	0	260°C
LCMXO256C	100 csBGA	ATP	Lot #4**	45	0	260°C
LCMXO640E	132 csBGA	ATP	Lot #1**	90	0	260°C
LCMXO640C	256 fpBGA	ATP	Lot #1**	46	0	250°C
LCMXO640C	256 fpBGA	ATP	Lot #2**	48	0	250°C
LCMXO2280C	324 ftBGA	ATP	Lot #1**	45	0	260°C
LCMXO2280C	324 ftBGA	ATP	Lot #2**	45	0	260°C
LAMXO2280E	324 ftBGA	ATP	Lot #5**	166	0	260°C
LAMXO2280E	324 ftBGA	ATP	Lot #6**	232	0	260°C
LAMXO2280E	324 ftBGA	ATP	Lot #7**	217	0	260°C
LAMXO2280E	324 ftBGA	ATP	Lot #8**	79	0	260°C
LFXP10E	388 fpBGA	ATP	Lot #1**	90	0	225°C
LFXP6C	144 TQFP	UTAC	Lot #7**	77	0	260°C
LFXP6C	144 TQFP	UTAC	Lot #8**	77	0	260°C
LFXP6C	144 TQFP	UTAC	Lot #9**	77	0	260°C
LFXP20E	256 ftBGA	UTAC	Lot # 1**	77	0	260°C
LFXP20E	256 ftBGA	UTAC	Lot # 2**	77	0	260°C

* These qual lots have copper (Cu) wire bonds.
** These qual lots have gold (Au) wire bonds.
A = FAR#1444: One unit functional failure (root cause analysis in-process)

Cumulative SMPC Failure Rate CS90F = 1 / 3,938

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4.2 MachXO Product Family Temperature Cycling Data

The Temperature Cycling test is used to accelerate those failures resulting from mechanical stresses induced by differential thermal expansion of adjacent films, layers and metallurgical interfaces in the die and package. Devices are tested at 25°C after exposure to repeated cycling between -55°C and +125°C in an air environment consistent with JEDEC JESD22-A104 "Temperature Cycling", Condition B temperature cycling requirements. Prior to Temperature Cycling testing, all devices are subjected to Surface Mount Preconditioning. Temperature cycling Qual-Complete is 700 cycles and is a relatively new requirement consistent with JESD47I.

MSL3 Packages: TQFP, PQFP, fpBGA, ftBGA, csBGA
Stress Duration: 700 and 1000 cycles
Stress Conditions: Temperature cycling between -55°C to 125°C
Method: Lattice Procedure # 70-101568, JESD47I, and JESD22-A104D

Table 4.2.1 Temperature Cycling Data

Product Name	Package	Assembly Site	Lot Number	Quantity	250 Cycles	500 Cycles	700 Cycles	1000 Cycles
LCMXO2280C	324 ftBGA	ASEM	Lot #1*	28	0	0	0	N/A
LCMXO2280C	324 ftBGA	ASEM	Lot #2*	28	0	0	0	N/A
LCMXO2280C	324 ftBGA	ASEM	Lot #3*	28	0	0	0	N/A
LCMXO2280C	132 csBGA	ASEM	Lot #1*	30	0	0	0	N/A
LCMXO2280C	132 csBGA	ASEM	Lot #2*	30	0	0	0	N/A
LCMXO2280C	132 csBGA	ASEM	Lot #3*	29	0	0	0	N/A
LCMXO2280E	100 TQFP	ASEM	Lot #1*	27	0	0	0	N/A
LCMXO2280E	100 TQFP	ASEM	Lot #2*	27	0	0	0	N/A
LCMXO2280E	100 TQFP	ASEM	Lot #3*	27	0	0	0	N/A
LCMXO2280E	144 TQFP	ASEM	Lot #1*	30	0	0	0	N/A
LCMXO2280E	144 TQFP	ASEM	Lot #2*	30	0	0	0	N/A
LCMXO2280E	144 TQFP	ASEM	Lot #3*	29	0	0	0	N/A
LFXP3E	100 TQFP	ASEM	Lot #4**	57	0	0	N/A	0
LFXP3E	208 PQFP	ASEM	Lot #3**	49	0	0	N/A	0
LFXP10C	256 fpBGA	ASEM	Lot #13**	32	0	0	N/A	0
LFXP10C	256 fpBGA	ASEM	Lot #14**	17	0	0	N/A	0
LFXP10C	256 fpBGA	ASEM	Lot #15**	3	0	0	N/A	0
LFXP10C	256 fpBGA	ASEM	Lot #16**	40	0	0	N/A	0
LCMXO2280	256 ftBGA	ASEM	Lot #1**	45	0	0	N/A	0
LCMXO2280	256 ftBGA	ASEM	Lot #2**	45	0	0	N/A	0
LFXP10E	388 fpBGA	ASEM	Lot #1**	45	0	0	N/A	0
LFXP10C	388 fpBGA	ASEM	Lot #9**	25	0	0	N/A	0
LFXP10C	388 fpBGA	ASEM	Lot #10**	14	0	0	N/A	0
LFXP10C	388 fpBGA	ASEM	Lot #11**	26	0	0	N/A	0
LFXP10C	388 fpBGA	ASEM	Lot #12**	28	0	0	N/A	0

Product Name	Package	Assembly Site	Lot Number	Quantity	250 Cycles	500 Cycles	700 Cycles	1000 Cycles
LCMXO256C	100 TQFP	ATK	Lot #1**	45	0	0	N/A	0
LCMXO256C	100 TQFP	ATK	Lot #2**	45	0	0	N/A	0
LAMXO640C	144 TQFP	ATK	Lot #1**	241	0	0	N/A	0
LAMXO640C	144 TQFP	ATK	Lot #2**	240	0	0	N/A	0
LAMXO640C	144 TQFP	ATK	Lot #1**	80	0	0	N/A	0
LAMXO640C	144 TQFP	ATK	Lot #2**	80	0	0	N/A	0
LAMXO2280E	144 TQFP	ATK	Lot #3**	76	0	0	N/A	0
LAMXO2280E	144 TQFP	ATK	Lot #4**	79	0	0	N/A	0
LCMXO256C	100 csBGA	ATP	Lot #3**	45	0	0	N/A	0
LCMXO256C	100 csBGA	ATP	Lot #4**	45	0	0	N/A	0
LCMXO640E	132 csBGA	ATP	Lot #3**	45	0	0	N/A	0
LCMXO640C	256 fpBGA	ATP	Lot #1**	46	0	0	N/A	0
LCMXO640C	256 fpBGA	ATP	Lot #2**	48	0	0	N/A	0
LCMXO2280C	324 ftBGA	ATP	Lot #1**	45	0	0	N/A	0
LCMXO2280C	324 ftBGA	ATP	Lot #2**	45	0	0	N/A	0
LAMXO2280E	324 ftBGA	ATP	Lot #5**	62	0	0	N/A	0
LAMXO2280E	324 ftBGA	ATP	Lot #6**	72	0	0	N/A	0
LAMXO2280E	324 ftBGA	ATP	Lot #7**	72	0	0	N/A	0
LAMXO2280E	324 ftBGA	ATP	Lot #8**	25	0	0	N/A	0
LFXP6C	144 TQFP	UTAC	Lot #7**	77	0	0	N/A	0
LFXP6C	144 TQFP	UTAC	Lot #8**	77	0	0	N/A	0
LFXP6C	144 TQFP	UTAC	Lot #9**	77	0	0	N/A	0
LFXP20E	256 ftBGA	UTAC	Lot # 1**	77	0	0	N/A	0
LFXP20E	256 ftBGA	UTAC	Lot # 2**	77	0	0	N/A	0

* These qual lots have copper (Cu) wire bonds.
** These qual lots have gold (Au) wire bonds.

Cumulative Temp Cycle Failure Rate CS90F = 0 / 2,590

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4.3 Unbiased HAST Data

Unbiased Highly Accelerated Stress Test (HAST) testing uses both pressure and temperature to accelerate penetration of moisture into the package and to the die surface. The Unbiased HAST test is designed to detect ionic contaminants present within the package or on the die surface, which can cause chemical corrosion. Consistent JEDEC JESD22-A118, "Accelerated Moisture Resistance - Unbiased HAST," the Unbiased HAST conditions are 96 hour exposure at 130°C, 85% relative humidity, and 2 atmospheres of pressure. Prior to Unbiased HAST testing, all devices are subjected to Surface Mount Preconditioning.

MSL3 Packages: TQFP, PQFP, fpBGA, ftBGA, csBGA
Stress Duration: 96 Hrs
Stress Conditions: 130°C, 15psig, 85% RH
Method: Lattice Procedure # 70-104285 and JESD22-A118A

Table 4.3.1 Unbiased HAST Data

Product Name	Package	Assembly Site	Lot Number	Quantity	# of Fails	Stress Duration
LCMXO640E	132 csBGA	ASEM	Lot #1	45	0	96 Hrs
LFXP10E	388 fpBGA	ASEM	Lot #1	45	0	96 Hrs
LFXP10E	388 fpBGA	ASEM	Lot #2	45	0	96 Hrs
LFXP10E	388 fpBGA	ASEM	Lot #5	45	0	96 Hrs
LAMXO640C	144 TQFP	ATK	Lot #1	81	0	96 Hrs
LAMXO640C	144 TQFP	ATK	Lot #2	79	0	96 Hrs
LAMXO2280E	144 TQFP	ATK	Lot #3	77	0	96 Hrs
LAMXO2280E	144 TQFP	ATK	Lot #4	58	0	96 Hrs
LAMXO2280E	324 ftBGA	ATP	Lot #5	46	0	96 Hrs
LAMXO2280E	324 ftBGA	ATP	Lot #6	72	0	96 Hrs
LAMXO2280E	324 ftBGA	ATP	Lot #7	73	0	96 Hrs
LAMXO2280E	324 ftBGA	ATP	Lot #8	40	0	96 Hrs

Cumulative Unbiased HAST failure Rate CS90F = 0 / 706

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4.4 THB: Biased HAST Data

Highly Accelerated Stress Test (HAST) testing uses both pressure and temperature to accelerate penetration of moisture into the package and to the die surface. The Biased HAST test is used to accelerate threshold shifts in the MOS device associated with moisture diffusion into the gate oxide region as well as electrochemical corrosion mechanisms within the device package. Consistent with JEDEC JESD A110-B "Highly-Accelerated Temperature and Humidity Stress Test (HAST)", the biased HAST conditions are with Vcc bias and alternate pin biasing in an ambient of 130°C, 85% relative humidity, for 96 hours; or 110°C, 85% relative humidity, for 264 hours. Prior to Biased HAST testing, all devices are subjected to Surface Mount Preconditioning.

MSL3 Packages: TQFP, PQFP, fpBGA, ftBGA, csBGA

Stress Conditions: Vcc= 1.2V/ V_{CCIO} = 3.3V, and either 130°C / 85% RH, 96 hrs; or 110°C / 85% RH, 264 hrs

Method: Lattice Procedure # 70-101571, JESD47I, and JESD22-A110D

Table 4.4.1 Biased HAST Data

Product Name	Package	Assembly Site	Lot Number	Quantity	# of Fails	Stress Temp	Stress Duration
LCMXO2280C	324 ftBGA	ASEM	Lot #1*	26	0	110°C	264 Hrs
LCMXO2280C	324 ftBGA	ASEM	Lot #2*	27	0	110°C	264 Hrs
LCMXO2280C	324 ftBGA	ASEM	Lot #3*	25	0	110°C	264 Hrs
LCMXO2280E	100 TQFP	ASEM	Lot #1*	26	0	130°C	96 Hrs
LCMXO2280E	100 TQFP	ASEM	Lot #2*	27	0	130°C	96 Hrs
LCMXO2280E	100 TQFP	ASEM	Lot #3*	27	0	130°C	96 Hrs
LFXP10E	388 fpBGA	ASEM	Lot #2**	45	0	130°C	96 Hrs
LFXP10E	388 fpBGA	ASEM	Lot #5**	45	0	130°C	96 Hrs
LFXP10E	388 fpBGA	ASEM	Lot #8**	45	0	130°C	96 Hrs
LAMXO640C	144 TQFP	ATK	Lot #2**	81	0	130°C	96 Hrs
LAMXO2280E	144 TQFP	ATK	Lot #3**	80	0	130°C	96 Hrs
LAMXO2280E	144 TQFP	ATK	Lot #4**	80	0	130°C	96 Hrs
LAMXO2280E	324 ftBGA	ATP	Lot #5**	58	0	130°C	96 Hrs
LAMXO2280E	324 ftBGA	ATP	Lot #6**	88	0	130°C	96 Hrs
LAMXO2280E	324 ftBGA	ATP	Lot #7**	72	0	130°C	96 Hrs
LAMXO2280E	324 ftBGA	ATP	Lot #8**	14	0	130°C	96 Hrs

* These qual lots have copper (Cu) wire bonds.
** These qual lots have gold (Au) wire bonds.

Cumulative BHAST failure Rate CS90F = 0 / 766

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4.5 MachXO Product Family High Temperature Storage Life (HTSL)

High Temperature Storage Life (HTSL)

The High Temperature Storage Life test is used to determine the effect of time and temperature, under storage conditions, for thermally activated failure mechanisms. Consistent with JEDEC JESD22-A103D, the devices are subjected to high temperature storage Condition B: +150 (-0/+10) °C for 1000 hours. Prior to High Temperature Storage, all MachXO2 devices are subjected to Surface Mount Preconditioning as mentioned in Table 4.1.1. This is a relatively new requirement consistent with JESD47F for Pb-free, wirebonded packages. For the non-volatile based products, the HTRX and HTSL stress and test conditions condition are the same. The HTSL test can be covered by HTRX.

MSL3 Packages: TQFP, csBGA, QFN

Stress Duration: 1000 hours

Temperature: 150°C (ambient)

Method: Lattice Document # 87-101925, JESD47I, JESD22-A103D, and JESD22-A113F

Table 4.5.1 MachXO High Temperature Storage Life Results

Product Name	Wafer Fab	Package Type	Assembly Site	Lot #	Qty	168 Hrs Result	500 Hrs Result	1000 Hrs Result	1500 Hrs Result	2000 Hrs Result	Cumulative Hours
LCMXO2280C	Mie-101	324 ftBGA	ASEM	Lot #1*	28	0	0	0	NA	NA	28,000
LCMXO2280C	Mie-101	324 ftBGA	ASEM	Lot #2*	28	0	0	0	NA	NA	28,000
LCMXO2280C	Mie-101	324 ftBGA	ASEM	Lot #3*	28	0	0	0	NA	NA	28,000
LCMXO2280E	Mie-101	100 TQFP	ASEM	Lot #1*	27	0	0	0	NA	NA	27,000
LCMXO2280E	Mie-101	100 TQFP	ASEM	Lot #2*	27	0	0	0	NA	NA	27,000
LCMXO2280E	Mie-101	100 TQFP	ASEM	Lot #3*	27	0	0	0	NA	NA	27,000
LAXP2-17E	Mie-323	256 ftBGA	ASEM	Lot #1**	69	0	0	0	NA	NA	69,000
LAXP2-17E	Mie-323	256 ftBGA	ASEM	Lot #8**	100	0	0	0	NA	NA	100,000
LAXP2-17E	Mie-323	256 ftBGA	ASEM	Lot #9**	80	0	0	0	NA	NA	80,000
LAXP2-17E	Mie-323	256 ftBGA	ASEM	Lot #10**	80	0	0	0	NA	NA	80,000
LFXP2-40E	Mie-323	672 fpBGA	ASEM	Lot #1**	80	0	0	0	NA	NA	80,000
LFXP2-8E	Mie-323	144 TQFP	ASEM	Lot #1***	46	0	0	0	NA	NA	46,000
LFXP2-5E	Mie-323	144 TQFP	ASEM	Lot #1***	80	0	0	0	NA	NA	80,000
LFXP2-5E	Mie-323	144 TQFP	ASEM	Lot #2***	80	0	0	0	NA	NA	80,000
LAXP2-5E	Mie-323	208 PQFP	ASEM	Lot #1***	80	0	0	0	NA	NA	80,000
LAXP2-5E	Mie-323	208 PQFP	ASEM	Lot #2***	80	0	0	0	NA	NA	80,000
LAXP2-5E	Mie-323	208 PQFP	ASEM	Lot #3***	77	0	0	0	NA	NA	77,000
LCMXO640C	Mie-323	256 fpBGA	ASEM	Lot #1***	88	0	0	0	NA	NA	88,000
LCMXO640C	Mie-323	256 fpBGA	ASEM	Lot #2***	88	0	0	0	NA	NA	88,000

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Product Name	Wafer Fab	Package Type	Assembly Site	Lot #	Qty	168 Hrs Result	500 Hrs Result	1000 Hrs Result	1500 Hrs Result	2000 Hrs Result	Cumulative Hours
LFXP10C	Mie-323	388 fpBGA	ASEM	Lot #3***	148	0	0	0	0	0	296,000
LFXP10C	Mie-323	388 fpBGA	ASEM	Lot #6***	150	0	0	0	0	0	300,000
LFXP10C	Mie-323	388 fpBGA	ASEM	Lot #7***	55	0	0	0	0	0	110,000
LAMXO256C	Mie-323	100 TQFP	ASEM	Lot #9***	80	0	0	0	NA	NA	80,000
LAMXO256E	Mie-323	100 TQFP	ASEM	Lot# 10***	80	0	0	0	NA	NA	80,000
LAMXO640E	Mie-323	256 fpBGA	ASEM	Lot #12***	78	0	0	0	NA	NA	78,000

* These qual lots have copper (Cu) wire bonds & stressed as High Temperature Storage Life (150°C bake) with SMPC.
** These qual lots have gold (Au) wire bonds & stressed as High Temperature Data Retention (150°C bake) without SMPC.
*** These lots have gold (Au) wire bonds & stressed as High Temperature Storage Life (150°C bake) without SMPC.

Cumulative HTSL failure Rate = 0 / 1,784
Cumulative HTSL device hours = 2,137,000

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5.0 CS90F PROCESS RELIABILITY WAFER LEVEL REVIEW

Several key fabrication process related parameters have been identified by the foundry that would affect the Reliability of the End-Product. These parameters are tested during the Development Phase of the Technology. Passing data (a 10yr lifetime at the reliability junction temperature) must be obtained for three lots minimum for each parameter before release to production. Normal operating conditions are defined in the Electrical Design Rules (EDR). These parameters are:

Hot Carrier Immunity (**HCI**): Effect is a reduction in transistor Idsat. Worst case is low temperature.

Time Dependent Dielectric Breakdown (**TDDB**): Transistor and capacitor oxide shorts or leakage.

Negative Bias Temperature Instability (**NBTI**): Symptom is a shift in Vth (also a reduction in Idsat).

Electromigration Lifetime (**EML**): Symptom is opens within, or shorts between, metal conductors.

Stress Migration (**SM**): Symptom is a void (open) in a metal Via due to microvoid coalescence.

Table 5.1 Wafer Level Reliability Results Fujitsu Mie Fabs

HCI	Device	LVN	MVN	HVN	LVP	MVP	HVP
	Celsius	25	25	25	25	25	25
	delta Ids	-10%	-10%	-10%	-10%	-10%	-10%
	Vds	1.32	3.6	5.5	-1.32	-3.6	-3.6
	TTF	3 lots > 180yr	5 lots > 18yr	4 lots > 30yr	3 lots > 120yr	3 lots > 64yr	3 lots > 36yr
TDDB	Device	LVN	MVN	HVN	LVP	MVP	HVP
	Celsius	125	125	125	125	125	125
	0.1% TTF	2 lots > 23yr	2 lots > 25yr	1 lot > 10yr	2 lots > 50yr	2 lots > 300yr	1 lot > 10yr
NBTI	Device	LVP	MVP	HVP			
	delta Ids	-10%	-10%	-10%			
	Celsius	125	125	125			
	TTF	3 lots > 60yr	5 lots > 47yr	3 lots > 200yr			
EML	Device	Intermediate	Semi-Global	Global (Top Al)			
	Celsius	125	125	125			
	0.1% TTF	3 lots > 45yr	1 lot > 72yr	1 lot > 89yr			
SM	Device	Intermediate*	Semi-Global				
	Celsius	125	125				
	TTF	3 lots > 11yr	3 lots > 11yr				

Note: Reliability life times are based on listed temperature and used conditions. Detailed WLR test conditions are available upon request.

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6.0 MACHXO PACKAGE ASSEMBLY INTEGRITY TESTS

6.1 Wire Bond Shear Test

This procedure is used to measure the wire bond strength at the ball joints. Thirty bonds from a minimum of five devices were used for Wire Bond Shear.

WIRE BOND SHEAR TEST RESULTS: All bond shear observations were > 15 grams for TQFP and ftBGA packages tested.

The average measured bond shear results for 100 and 144 pin TQFP were Cpk of > 3.7 and Ppk of > 3.7.
The average measured bond shear results for 256 and 324 ball ftBGA were Cpk of > 3.5 and Ppk of > 3.5

6.2 Wire Bond Pull

This procedure is used to measure the wire bond strength at the ball joints and stitch bonds. For products evaluation thirty bonds from a minimum of five devices were used for and Wire Bond Pull. Test conditions for these tests were 6 grams minimum for 1.0 mil gold wire

WIRE BOND PULL RESULTS: All bond pull observations were > 6 grams for TQFP and ftBGA packages tested.

The average measured wire bond pull results for 100 and 144 pin TQFP were Cpk of > 3.2 and Ppk of > 3.2.
The average measured wire bond pull results for 256 and 324 ball ftBGA were Cpk of > 2.4 and Ppk of > 2.4.

6.3 Solderability

This procedure is used to evaluate the solderability of device terminals normally joined by a soldering operation. An accelerated aging test is included in this test method, which simulates natural aging under a combination of various storage conditions that have deleterious effects. Units are exposed to a 8 hour steam preconditioning followed a flux exposure for 7 seconds and a dip in Pb-free solder alloy @ 245°C ± 5°C for 5 seconds. Minimum of 22 leads from 3 devices per lot were tested with zero failure acceptance.

No failures were observed for MachXO devices in TQFP packages. All the tested units passed. There was less than 5% pitting and dewetting on the solder covered area.

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6.4 Physical Dimensions

Devices were measured using the appropriate Lattice Semiconductor case outline drawings.

The 10 devices each of 100 and 144 pin TQFP from 3 different lots were measured with no failures found. The calculated Cpk on this small sample is Cpk > 5.2.

The 10 devices each of 256 and 324 pin ftBGA from 3 different lots were measured with no failures found. The calculated Cpk on this small sample is Cpk > 2.0.

6.5 Solder Ball Shear

For the 256 ball and 324 ball ftBGA packages, ten devices from three lots were tested. All units were exposed to two surface mount reflow simulations.

The 256 ball ftBGA packages use a 0.40 mm barrier metal diameter. All ball shear observations were > 800 grams.

The 324 ball ftBGA packages use a 0.45 mm barrier metal diameter. All ball shear observations were > 1200 grams.

The average measured ball shear results for 256 and 324 ball ftBGA packages post reflow stress were Cpk of > 2.0.

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7.0 MACHXO ADDITIONAL FAMILY DATA

Table 7.1 MachXO Package Assembly Data – csBGA/ ftBGA

Package Attributes / Assembly Sites	ASEM	Amkor	UTAC
Die Family (Product Line)	MachXO	MachXO	MachXO
Fabrication Process Technology	CS90F (130nm CMOS)	CS90F (130nm CMOS)	CS90F (130nm CMOS)
Package Assemble Site	Malaysia	Philippines	Singapore
Package Type	csBGA/ftBGA	csBGA/caBGA/ ftBGA	csBGA/ftBGA
Ball Counts	100/132/256	100/132/256/324	100/132/256
Die Preparation/Singulation	wafer saw, full cut	wafer saw, full cut	wafer saw, full cut
Die Attach Material	Ablebond 2100A	Ablebond 2300	Ablebond 2100A
Mold Compound Supplier/ID	Sumitomo / G770 Series	Sumitomo / G770 Series	Hitachi 9750HF Series
Wire Bond Material	Gold (Au)	Gold (Au)	Gold (Au)
Wire Bond Methods	Thermosonic Ball	Thermosonic Ball	Thermosonic Ball
Substrate Material	Bismaleimide Triazine HL83X Series	Bismaleimide Triazine HL83X Series	Bismaleimide Triazine HL83X Series
L/F Plating or BGA Ball	Sn96.5/Ag3.0/Cu0.5	Sn95.5/Ag4.0/Cu0.5	Sn96.5/Ag3.0/Cu0.5
Lead Finish	SnAgCu solder ball	SnAgCu solder ball	SnAgCu solder ball
Marking	Laser	Laser	Laser

Table 7.2 MachXO Package Assembly Data- TQFP

Package Attributes / Assembly Sites	ASEM	Amkor	UTAC
Die Family (Product Line)	MachXO	MachXO	MachXO
Fabrication Process Technology	CS90F (130nm CMOS)	CS90F (130nm CMOS)	CS90F (130nm CMOS)
Package Assembly Site	Malaysia	Korea	Singapore
Package Type / Pin Count	TQFP 100/144	TQFP 100/144	TQFP 100/144
Die Preparation/Singulation	wafer saw, full cut	wafer saw, full cut	wafer saw, full cut
Die Attach Material	Ablebond 3230	Ablebond 3230	Ablebond 3230
Mold Compound Supplier/ID	Hitachi 9220HFA Series	KTMC5700TQ Series	Hitachi 9510HF Series
Wire Bond Material	Gold (Au)	Gold (Au)	Gold (Au)
Wire Bond Methods	Thermosonic Ball	Thermosonic Ball	Thermosonic Ball
Lead frame Material	Cu Alloy	Cu Alloy	Cu Alloy
Lead Finish	Matte Sn (annealed)	Matte Sn (annealed)	Matte Sn (annealed)
Marking	Laser	Laser	Laser

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Table 7.3 Copper (Cu) Bond Wire Bills of Material by Package Type and Assembly Site

Attributes	Saw-Singulated BGA	TQFP	Overmolded BGA
Assembly Site	ASEM / ASET / ATP	ASEM / ASET / ATP	ASEM / ASET / ATP
Die Family (Product Line)	ispMACH 4000ZE, LatticeECP3, LatticeXP2, MachXO and MachXO2	ispMACH 4000ZE, LatticeEC, LatticeECP, LatticeECP2, LatticeECP3, LatticeXP, LatticeXP2, MachXO and MachXO2	LatticeEC, LatticeECP, LatticeECP2M, LatticeECP3, LatticeXP, LatticeXP2, and MachXO2
Fabrication Process Technology	65nm, 90nm, 130nm & 180nm	65nm, 90nm, 130nm & 180nm	65nm, 90nm, & 130nm
Package Type	ucBGA, csBGA, caBGA & ftBGA	TQFP	fpBGA
Ball/Lead Counts	64/132, 56/64/100/132/144/328, 256/332 & 256/324	44, 48, 64, 100, 128 & 144	256, 388, 484, 672, 900, 1152 & 1156
Die Attach Material	Ablebond 2100A / Ablebond 2100A / Ablebond 2300	Yizbond 8143 / CRM-1076WA / Ablebond 3230	Ablebond 2100A / Ablebond 2100A / Ablebond 2300
Mold Compound Supplier/ID	Sumitomo EME G750E / KEG-1250LKDS / GE-110	Sumitomo EME G700Y / EME-G631H / G700SY	Sumitomo EME G750SE / CEL-9750ZHF10AKL-U / GE-110
Mold Compound Chlorine (Cl^-) content	≤ 10 ppm	≤ 20 ppm	≤ 10 ppm
Mold Compound pH level	5 to 7	5 to 7	5 to 7
Wire Bond Material	Palladium-coated Copper (PdCu)	Copper (Cu) / Palladium-coated Copper (PdCu) / Palladium-coated Copper (PdCu)	Palladium-coated Copper (PdCu)
Wire Bond Methods	Thermosonic Ball	Thermosonic Ball	Thermosonic Ball

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8.0 REVISION HISTORY

Table 8.0 Lattice MachXO Product Family Qualification Summary Revisions

Date	Revision	Section	Change Summary
October 2005	A		New Release
May 2006	B		Updated Data in report
April 2009	C		Updated report
October 2012	D	2.2, 3.4.2	ESD-MM data added, administrative change to add document wrapper.
November 2012	E	3.4.2	Update ESD-MM terminology
June 2014	F	All	CS90F Fab transfer to Fujitsu Mie-101; deleted ESD MM data
September 2014	G	All	1000 hour HTOL update; update ESD follow on products; remove revision levels from Jedec tables; update Product Qualification Process Flowchart
January 2015	H		Provide schedule for update of correct ESD-HBM data; correct wrapper title page

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