L-ASC10 and Platform Manager 2 Hardware Checklist

Technical Note

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
ASC	Analog Sense and Control
FPGA	Field Programmable Gate Array
HDL	Hardware Description Language
I^2C	Inter-Integrated Circuit
JTAG	Joint Test Action Group
PCB	Printed circuit board
QFN	Quad Flat No-leads
SPI	Serial Peripheral Interface

1. Introduction

When designing complex hardware using L-ASC10 and Platform Manager 2, designers must pay special attention to critical hardware configuration requirements. This technical note guides the designer through these critical hardware requirements related to the L-ASC10 and Platform Manager 2 devices. This document does not provide detailed step-by-step instructions but gives a high-level summary and checklist to assist in the design process.

This technical note assumes that the reader is familiar with the L-ASC10 and Platform Manager 2 device features as described in L-ASC10 Data Sheet (FPGA-DS-02038) and Platform Manager 2 Data Sheet (FPGA-DS-02036).

The critical hardware areas covered in this technical note include:

- Power supplies as they relate to the Platform Manager 2 supply rails and how to connect them to the PCB and the associated system
- Configuration and how to connect the configuration mode selection for proper power up configuration
- System connections required for proper operation of the Platform Manager 2 system
- Device I/O interface and critical signals.

Important: Users should refer to the following documents for detailed recommendations.

- Power Decoupling and Bypass Filtering for Programmable Devices (TN1068)
- Power Estimation and Management for MachXO2 Devices (TN1198)
- MachXO2 sysI/O Usage Guide (TN1202)
- Using User Flash Memory and Hardened Control Functions in MachXO2 Devices (TN1205)
- Power and Thermal Estimation and Management for MachXO3 Devices (TN1289)
- MachXO3 sysI/O Usage Guide (TN1280)
- Using Hardened Control Functions in MachXO3 Devices (TN1293)

2. Power Supplies

There are several different types of power rails required to operate the Platform Manager 2 devices. Each type is discussed to assist the user in setting up the board correctly.

2.1. VCC

The core power for the FPGA section of the Platform Manager 2 is the VCC rail. VCC is nominally 3.3 V, with a minimum of 2.8 V and a maximum of 3.465 V. VCC must have 0.1 uF decoupling capacitors located as close to the VCC pins as possible. In addition to the 0.1 uF capacitors, a 1-10 uF tantalum capacitor should be added to the rail on the board.

2.2. VCCA

The VCCA is an analog supply for the ASC section of Platform Manager 2. This supply should have a 0.1 uF capacitor close to the VCCA pin and a ferrite bead to isolate the supply from the VCC rail. The nominal value is 3.3 V, with a minimum of 2.8 V and a maximum of 3.465 V. The values listed here are practical limits taking into account the interface to any of the following: FPGA section of Platform Manager 2, MachXO2, or MachXO3.

2.3. VCCIO0, VCCIO1, VCCIO2, and VCCIO3

These are the FPGA PIO bank supplies. In general, the VCCIO supply must be in the range from 1.14 V minimum to 3.465 V maximum except where noted below. It is recommended to include a 0.1 uF decoupling capacitor located close to the VCCIO pins. When a PIO bank is hooked up as 3.3 V, for example, all of the PIOs in that bank share a common 3.3 V I/O voltage. If a PIO bank is not used, the VCCIO pins for that bank should be connected to the VCC rail on the board.

2.4. VCCIO0

This is the supply for FPGA Bank 0 as well as the supply for the JTAG and I^2C ports. This rail is required for programming and has a minimum of 2.8 V and a maximum of 3.465 V. It is recommended to include a 0.1 uF capacitor located close to the VCCIO0 pin.

2.5. VCCIO1

This is the supply for FPGA Bank 1. For LPTM21L (100-Ball caBGA) devices, Bank 1 is not used to interface to the internal ASC, see VCCIO3. For LPTM21 (237 Ball ftBGA) devices, Bank 1 is used to interface to the internal ASC section. Therefore, the VCCIO1 supply has a minimum of 2.8 V and a maximum of 3.465 V. For Platform Manager 2, MachXO2 or MachXO3 designs, which include external ASCs, the PIO banks that are used to interface to the ASC must have a VCCIO supply between 2.8 V and 3.465 V. It is recommended to include a 0.1 uF capacitor located close to the VCCIO1 pin.

2.6. VCCIO3

This is the supply for FPGA Bank 3. For LPTM21L (100-Ball caBGA) devices Bank 3 is used to interface to the internal ASC section. Theretofore, for the LPTM21L (100-Ball caBGA) the VCCIO3 supply has a minimum of 2.8 V and a maximum of 3.465 V and for the LPTM21 (237-Ball ftBGA) the VCCIO3 supply has a minimum of 1.8 V and a maximum of 3.465 V. It is recommended to include a 0.1 uF capacitor located close to the VCCIO3 pin.

Table 2.1. Power Supply Description and Voltage Levels

Supply	LPTM21L 100-Ball caBGA	LPTM21 237-Ball ftBGA	Voltage (Nominal Value)	Description
VCC	✓	✓	3.3 V	Core power supply for FPGA section of Platform Manager 2
VCCA	✓	✓	3.3 V	Core power supply for Analog section (or ASC) of Platform Manager 2
VCCIO0	✓	✓	3.3 V	Power Supply for PIO Bank 0, JTAG, and I^2C pins
VCCIO1	—	✓	3.3 V	Power Supply for PIO Bank 1 and 3-wire ASC-I/F section of LPTM21
	✓	—	N/A	PIO Bank 1 is not supported in LPTM21L
VCCIO2	✓	✓	1.2 V to 3.3 V	Power Supply for PIO Bank 2 and SPI pins
VCCIO3	—	✓	1.2 V to 3.3 V	Power Supply for PIO Bank 3 of LPTM21
	✓	—	3.3 V	Power Supply for PIO Bank 3 and 3-wire ASC-I/F section of LPTM21L

2.7. Power Good Condition

The VCC, VCCA, and VCCIO0 power supplies determine the internal “power good” condition for the Platform Manager 2 device. All three of these supplies need to be at a valid and stable level before the device can become operational. In addition, when using external ASC devices which are “Mandatory”, these are required to be powered up fully before the Platform Manager 2 can become operational. If the system is using “Optional” external ASC devices, these do not have to be powered up fully before the Platform Manager 2 can become operational.

For most applications all supplies can be tied to a common VCC rail of 3.3 V, with added ferrite isolation on VCCA. When they are all common, the rails all come up at the same time and the device is set up for VCC, VCCIO, inputs/outputs, JTAG, etc. at the nominal range for 3.3 V logic interfaces.

2.8. Ground Pins

The Platform Manager 2 device uses both GND and GNDIO pins. The GNDIO0, GNDIO1, GNDIO2, and GNDIO3 pins are the ground pins for each of the PIO Banks of the device. All ground pins are required to be connected to a common ground plane.

2.9. External ASC Considerations

When using an external ASC device insure that the power supply for the external ASC has a common ground reference level with the Platform Manager 2 or MachXO2 device. This can be challenging if the external ASC is mounted on a separate card but is important. In addition, the power supplies for the ASC must have levels which are similar to the Platform Manager 2 VCCIO rails. Different voltage levels may adversely affect the signals between the Platform Manager 2 or MachXO2 and the external ASC devices. If programming external ASC devices in-system, insure that the VCC source to the external ASC devices are not turned off when the Platform Manager 2 enters a programming sequence and its outputs return to their safe state condition.

3. Power Estimation

Once the Platform Manager 2 device density, package and logic implementation is decided, power estimation can be performed using the Power Calculator tool which is provided as part of the Lattice Diamond® design software. While performing power estimation the user should keep two specific goals in mind.

- Power supply budgeting should be considered based on the maximum of the power-up in- rush current, configuration current or maximum DC and AC current for a given system environmental condition.
- The ability of the system environment and Platform Manager 2 device packaging to support the specified maximum operating junction temperature.

By determining these two criteria, system design planning can take the Platform Manager 2 power requirements into consideration early in the design phase.

This is explained in further detail in the respective FPGA technical notes:

- Power Estimation and Management for MachXO2 Devices (TN1198)
- Power and Thermal Estimation and Management for MachXO3 Devices (TN1289)

4. Configuration Considerations

Platform Manager 2 devices contain two types of memory, SRAM and non-volatile. SRAM is volatile memory and contains the active configuration. The non-volatile memory provides on-chip storage for the SRAM configuration data. The FPGA section uses flash memory for non-volatile storage while the ASC uses EEPROM for non-volatile storage.

The Platform Manager 2 is configured using the JTAG port but can also be configured from the primary I^2C port. The ASC devices are configured from the I^2C port. The Diamond Programmer software automatically sends the configuration data to the appropriate ports.

When using the Dual Boot mode (enabled in software), the *Golden Image* of the system configuration can be stored in an external SPI flash and the master SPI port is used.

For ease of prototype debugging it is recommended that every PCB should have easy access to the programming and configuration pins.

The use of external resistors is always needed if the configuration signals are being used to handshake with other devices. Pull-up and pull-down resistor (4.7K) recommendations on different configuration pins are listed below. External pull-up or pull-down resistors should be added to the pins shown in Table 4.1. if the configuration port is used in the design. If the optional pins are left as general purpose I/O then the external resistors are not needed.

When using JTAG programming, place a 4.7K pull-up on the TMS signal and a 4.7K pull-down on the TCK signal. For noisy environments, an optional R/C filter can be placed on the JTAG clock line, TCK. Use a 100 Ohm series resistor located close to the TCK pin and a 50 pF capacitor to ground.

Table 4.1. Default State of the sysCONFIG Pins

Pin Name	Pin Function (Configuration Mode)	Pin Direction (Configuration Mode)	Default Function (User Mode)
PROGRAMN	PROGRAMN	Input with weak pull-up, Add external pull-up	PROGRAMN
INITN	I/O	I/O with weak pull-up	User-defined I/O
DONE	I/O	I/O with weak pull-up	User-defined I/O
MCLK/CCLK	SSPI	Input with weak pull-up; Add external pull-up; Add external series resistor.	User-defined I/O
SN	SSPI	Input with weak pull-up; Add external pull-up	User-defined I/O
SI/SPISI	SSPI	Input	User-defined I/O
SO/SOSPI	SSPI	Output	User-defined I/O
CSSPIN	I/O	I/O with weak pull-up, Add external pull-up 10K	User-defined I/O
SCL	I^2C	Bi-Directional open drain, Add external pull-up	SCL
SDA	I^2C	Bi-Directional open drain, Add external pull-up	SDA
TDI	TDI	Input with weak pull-up	TDI
TDO	TDO	Output with weak pull-up	TDO
TCK	TCK	Input, Add external pull-down	TCK
TMS	TMS	Input with weak pull-up, Add external pull-up	TMS
JTAGENB	I/O	Input with weak pull-down, Add external pull-up	I/O

5. PROGRAMN Initial Power Considerations

The Platform Manager 2 PROGRAMN pin is permitted to become a general purpose I/O. The PROGRAMN only becomes a general purpose I/O after the configuration bitstream is loaded. When power is applied to the Platform Manager 2, the PROGRAMN input performs the PROGRAMN function. It is critical that any signal input to the PROGRAMN have a high-to-low transition period that is longer than the VCC (min) to INITN rising edge time period. Transitions faster than this time period prevent the Platform Manager 2 from becoming operational. It is recommended that the PROGRAMN pin be used for configuration only to avoid startup problems of the Platform Manager 2 device.

6. System Connections

When using a Platform Manager 2 design, there are a number of connections that must be made on the customer's board. Some are made between pins of the LPTM21 device. Others are made between the LPTM21, LPTM21L, MachXO2, or MachXO3 and the external ASC devices. The required connections are listed below along with the conditions for each.

6.1. RESETb Connections

The RESETb pins from all Mandatory ASC devices must be connected to the same PIO pin on the FPGA section or FPGA device. ASC0 is always Mandatory by design. The RESETb pins from all Optional ASC devices must be connected to individual PIO pins of the FPGA section or FPGA device. For examples of the required connections see Figure A.1 and Figure A.2. For more information, see L-ASC10 Data Sheet (FPGA-DS-02038) and Platform Manager 2 Data Sheet (FPGA-DS-02036).

The RESETb pin must not be used for the sequencer control logic reset. Instead, a separate FPGA PIO pin should be used along with equations or logic steps that reset the sequencer control logic. Any FPGA PIO pin can be used for this function though it must not be the same PIO pin that is connected to a RESETb pin.

6.1.1. LPTM21 (237-Ball ftBGA) Based Designs

When the LPTM21 (237-Ball ftBGA) device is the Central Controller of a Platform Manager 2 system, the designer MUST connect the RESETb pin from the ASC0 section to a PIO pin of FPGA section of the LPTM21 device in the customer schematic. This must be done external to the device package on the customer's board. If using external ASC devices the user must also connect the RESETb pin from the ASC to a PIO of the FPGA section.

6.1.2. LPTM21L (100-Ball caBGA) Based Designs

When the LPTM21L (100-Ball caBGA) device is the Central Controller of a Platform Manager 2 system, the RESETb pin from the ASC0 section is internally connected to the FPGA section pin C1. If using external ASC devices the user must also connect the RESETb pin from the ASC to a PIO of the FPGA.

6.1.3. MachXO2 or MachXO3 Based Designs

When either a MachXO2 or a MachXO3 device is the Central Controller of a Platform Manager 2 system, the designer MUST connect the RESETb pin from the ASC0 device to a PIO pin of MachXO2 or MachXO3 device. If using external ASC devices the user must also connect the RESETb pin from the ASC to a PIO of the MachXO2 or MachXO3 device.

6.2. ASC CLOCK Connections

The ASC Clock is an 8 MHz clock that synchronizes the three-wire interface (ASC-I/F) to each Hardware Expander (L-ASC10 or LPTM21L devices) to the Central Controller. For examples of the required connections, see Figure A.1 and Figure A.2. For more information, see L-ASC10 Data Sheet (FPGA-DS-02038) and Platform Manager 2 Data Sheet (FPGA-DS-02036).

6.2.1. LPTM21 (237-Ball ftBGA) Based Designs

When the LPTM21 (237-Ball ftBGA) device is the Central Controller of a Platform Manager 2 system, the ASCCLK pin is a NO CONNECT pin for all the Hardware Expanders and the LPTM21 device.

6.2.2. LPTM21L (100-Ball caBGA) Based Designs

When the LPTM21L (100-Ball caBGA) device is the Central Controller of a Platform Manager 2 system, the ASCCLK pin is a NO CONNECT pin for all the Hardware Expanders and the LPTM21L device.

6.2.3. MachXO2 or MachXO3 Based Designs

When either a MachXO2 or a MachXO3 device is the Central Controller of a Platform Manager 2 system, the user MUST connect the ASCCLK pin from ASC0 to a PCLK pin (True) on the MachXO2/3. For any other Hardware Expanders, the ASCCLK pin is a NO CONNECT pin.

6.3. ASC Interface Connections

The ASC Interface (ASC-I/F) is a three-wire connection that consists of an 8 MHz synchronous clock (MCLK), write data (WDAT), and read data (RDAT). The Central Controller uses the ASC-I/F to monitor and control the Hardware Expanders (L-ASC10 or LPTM21L) in the system. For examples of the required connections, see Figure A.1 and FFigure A.2. For more information, see L-ASC10 Data Sheet (FPGA-DS-02038) and Platform Manager 2 Data Sheet (FPGA-DS-02036).

6.3.1. LPTM21 (237-Ball ftBGA) Based Designs

When the LPTM21 (237-Ball ftBGA) device is the Central Controller of a Platform Manager 2 system, the ASC-I/F connection is made within the device. Note that the NC_FT1, NC_FT2, and NC_FT3 pins are NO CONNECT pins on the LPTM21 device. It is recommended to bring these pins out to test points close to the device for diagnostic purposes but these pins MUST NOT be connected to VCC, GND, or to any other devices in the system.

For all external Hardware Expanders, you MUST connect the WRCLK, WDAT, and RDAT pins to PIO pins on the FPGA section. Each Hardware Expander in the system MUST have its own three I/O pins assigned for these signals; the Hardware Expanders CANNOT share these I/O pins.

6.3.2. LPTM21L (100-Ball caBGA) Based Designs

When the LPTM21L (100-Ball caBGA) device is the Central Controller of a Platform Manager 2 system, the ASC-I/F connection is made within the device. Note that the NC_FT1, NC_FT2, NC_FT3, and NC_FT4 pins are NO CONNECT pins on the LPTM21L device. It is recommended to bring these pins out to test points close to the device for diagnostic purposes but these pins MUST NOT be connected to VCC, GND, or to any other devices in the system.

For all external Hardware Expanders, you MUST connect the WRCLK, WDAT, and RDAT pins to PIO pins on the FPGA section. Each Hardware Expander in the system MUST have its own three I/O pins assigned for these signals; the Hardware Expanders CANNOT share these I/O pins.

6.3.3. MachXO2 or MachXO3 Based Designs

When either a MachXO2 or a MachXO3 device is the Central Controller of a Platform Manager 2 system, no internal connections are possible for the ASC-I/F. For all external Hardware Expanders, you MUST connect the WRCLK, WDAT, and RDAT pins to PIO pins on the MachXO2/3. Each Hardware Expander in the system MUST have its own three I/O pins assigned for these signals; the Hardware Expanders CANNOT share these I/O pins.

6.4. I²C Connections

In all Platform Manager 2 Designs, the Central Controller and Hardware Expanders MUST be connected to a common I²C bus. Make sure there are external pull-up resistors (typically 2.2K to 3.3K) on the SDA and SCL lines of the I²C bus. The common I²C bus is used to support programming and features such as Dual Boot and VID. For examples of the required connections, see Figure A.1 and Figure A.2. For more information, see L-ASC10 Data Sheet (FPGA-DS-02038) and Platform Manager 2 Data Sheet (FPGA-DS-02036).

6.4.1. LPTM21 (237-Ball ftBGA) Based Designs

When the LPTM21 (237-Ball ftBGA) device is the Central Controller of a Platform Manager 2 system, you MUST connect on the package the SDA_S and SCL_S pins of the ASC section to the SDA_M and SCL_M pins of the FPGA section. This must be done external to the device package on the customer's board.

All external Hardware Expanders (L-ASC10 or LPTM21L) must also connect the SDA and SCL pins to the SDA_M and SCL_M pins on the LPTM21 device.

It is recommended to add a 50 ns filter to the I²C lines which connect to the SDA_M and SCL_M pins of the LPTM21 device to insure compliance with the I²C specification.

6.4.2. LPTM21L (100-Ball caBGA) Based Designs

When the LPTM21L (100-Ball caBGA) device is the Central Controller of a Platform Manager 2 system, the SDA and SCL pins of the ASC section and FPGA section are connected within the device.

All external Hardware Expanders (L-ASC10 or LPTM21L) must also connect the SDA and SCL pins to the SDA and SCL pins on the LPTM21L device.

It is recommended to add a 50 ns filter to the I²C lines which connect to the SDA and SCL pins on the LPTM21L device to insure compliance with the I²C specification.

6.4.3. MachXO2 or MachXO3 Based Designs

When either a MachXO2 or a MachXO3 device is the Central Controller of a Platform Manager 2 system, you MUST connect the SDA and SCL pins of all external Hardware Expanders (L-ASC10 or LPTM21L) to the SDA/PCLKC0_0 and SCL/PCLKT0_0 pins on the MachXO2/3 device.

It is recommended to add a 50 ns filter to the I²C lines which connect to the SDA/PCLKC0_0 and SCL/PCLKT0_0 pins on the MachXO2/3 device to insure compliance with the I²C specification.

6.5. I²C Write Protect

If using the I²C write protect feature in your design, you MUST connect the ASC GPIO1 pin to a PIO pin on the FPGA section. For examples of the required connections see Figure A.1 and Figure A.2. For more information, see L-ASC10 Data Sheet (FPGA-DS-02038) and Platform Manager 2 Data Sheet (FPGA-DS-02036).

6.6. Setting the I²C Address

6.6.1. ASC Section I²C Address

When using external ASC devices, you MUST connect the appropriate resistor to the I2C_ADDR pin on the ASC or ASC section of the LPTM2L (100-Ball caBGA). See Table 6.1 for a listing of the required resistor values for each ASC in the system.

Table 6.1. Resistor Values for External ASC I2C_ADDR Pin

ASC Device Number	R_{addr} Value[1]
0[2]	Tie to GND
1	2.2 kΩ
2	4.4 kΩ[3]
3	7 kΩ[4]
4	10 kΩ
5	13.7 kΩ
6	17.8 kΩ
7	Tie to +3.3 V[5]

Notes:

1. All resistor values should be +/– 1% tolerance or better.
2. For LPTM21 projects, the External ASCs start with ASC1. The Internal ASC of the LPTM21 has the I2C_ADDR pin connected On-Chip and is always designated as ASC0.
3. For designs that utilize E-96 resistors, a value of 4.42 kΩ can also be used.
4. For designs that utilize E-96 resistors, a value of 7.15 kΩ can also be used.
5. Tie to same supply used for VCCA of the ASC device.

6.6.2. FPGA Section I²C Address

When using the LPTM21L (100-Ball caBGA package) Platform Manager 2 as a hardware expander, the FPGA section I²C device address can be changed to avoid bus conflicts. Three pins are sampled at power up to determine the address range occupied by the FPGA section, as listed in Table 6.2 and shown in Figure A.3.

Table 6.2. LPTM21L (100-Ball caBGA Package) Setting the FPGA Section I²C Address Range

Logical State of Input at Power Up*			FPGA Section I²C Address Used
B2 I2C_ADDR2	E1 I2C_ADDR1	D3 I2C_ADDR0	
0	0	0	0x20 – 0x23
0	0	1	0x24 – 0x27
0	1	0	0x28 – 0x2B
0	1	1	0x2C – 0x2F
1	0	0	0x30 – 0x33
1	0	1	0x34 – 0x37
1	1	0	0x38 – 0x3B
1	1	1	0x3C – 0x3F

***Note:** Install a 1 kΩ pull up resistor to VCC to set the input to logic 1.

The LPTM21L (100-Ball caBGA Package) also provides a method of setting the I²C address of the FPGA section. The LPTM21L is configured from the factory with an algorithm in the FPGA section that reads the logic level of three pins at power up. Based on the decoding of the three pins, a unique I²C address is written into EEPROM, as listed in Table 24. The FPGA section I²C address remains in effect even after you flash memory (UFM) or con-figuration array (CFG) is erased.

WARNING: If the entire FPGA section is erased, then both the algorithm and the unique I²C address are removed and the FPGA section only responds to the default I²C address of 0x40.

Figure A.3 shows the required connections for an LPTM21L central controller with three LPTM21L hardware expanders. At power up, the rdat signal from each hardware expander is low so that the FPGA section I^2C address of the central controller is set to 0x20 (see Table 6.2). The three hardware expanders use the same three pins (D3, E1, and B2) of each device, with 1 kΩ pull-up resistor used to set the I^2C address of their respective FPGA sections. The pins are configured with an internal weak pull-down so that unconnected pins are a logic zero (0).

6.7. External ASC Die Pad

The die pad of the external ASC package (48 pin QFN) is the ground connection for this package and MUST BE connected to the ground of the PCB by the user. This pin is listed as pin 49 in L-ASC10 Data Sheet (FPGA-DS-02038).

7. I/O Pins

There are several types of I/O pins on the Platform Manager 2 device. These range from special function pins to standard inputs and outputs. Designers need to pay attention to the different types of pins to understand their functions and how they interface to other analog or digital circuits on the board. Listed below is a summary of the different pin types and their typical configuration requirements. Refer to Platform Manager 2 Data Sheet (FPGA-DS-02036) for detailed information.

7.1. GPIO Pins

The GPIO1 through GPIO10 pins can be configured either as input or output pins (but not as true bi-directional pins). When configured as outputs these are open-drain type outputs. These pins are controlled by the logic equations defined in the Platform Designer tool or in HDL. In addition, GPIO2 and GPIO3 can be controlled though the ASC Output control block if desired. The GPIO1 pin can be used as the I^2C write protect pin if this feature is selected. In this mode it becomes a dedicated input pin.

The GPIO pins require an external pull-up resistor tied to a power rail when used as outputs. The outputs can be pulled as high as 5.5 V. Unused output pins can be left floating.

7.2. HVOUT Pins

The HVOUT pins are N-Channel MOSFET drivers for generating a controlled power supply ramp. These pins can also be programmed as open-drain logic outputs. When used as a MOSFET driver, place a 10-100 Ohm series resistor in the gate path. Place the resistor as close to the MOSFET gate lead as possible. This helps prevent high-speed parasitic oscillations. When used as open-drain outputs, the output requires an external pull-up resistor. HVOUTs in open-drain mode can be pulled up to a max of 13 V. Unused HVOUTs can be left floating or connected to ground.

7.3. GPIO and HVOUT Safe State

Be sure to review the Safe-State of the GPIO and HVOUT pins to insure the connected device has the correct behavior. The safe-state of the GPIO and HVOUT pins is shown in Table 7.1. See the data sheet for more details.

Table 7.1. GPIO and HVOUT Safe-State Definitions

I/O	Safe-State
HVOUT1	Low
HVOUT2	Low
HVOUT3	Low
HVOUT4	Low
GPIO1	Low
GPIO2	Low
GPIO3	Low
GPIO4	Low
GPIO5	Low
GPIO6	Low
GPIO7[1]	Hi-Z
GPIO8	Hi-Z
GPIO9	Hi-Z
GPIO10	Low

Note: GPIO7 is not bonded out on the QFN48 package ASC device.

Note that if the Safe-state of a GPIO or HVOUT pin is *Low*, then any external pull-up resistor is overridden by the Safe-state during the power-up process of the Platform Manager 2 system. See Platform Manager 2 Data Sheet (FPGA-DS-02036) for more information about the Platform Manager 2 system power-up process.

7.4. Open Drain Loading

The external loading on the GPIO, PIO, and HVOUT pins in Open Drain mode must have a pull-up resistor for the output to function. The value of the resistor should be large enough so the sink current does not exceed the data sheet specifications. In some designs, a soft-start capacitor may be connected to the DC/DC converter enable pin. In applications that have a capacitor connected to the open-drain output, designers should include a resistor (RLimit) to limit the sink current when discharging the capacitor, as shown in Figure 7.1. For example; a limit resistor with a value of 220 Ω limits the discharge current to a maximum of 15 mA when the pull-up resistor is connected to 3.3 V. Also, the value of 220 Ω is small enough that the DC/DC Enable pin sees a logic "0" when the open-drain is low (provided that the pull-up resistor value is greater than 2.2 kΩ).

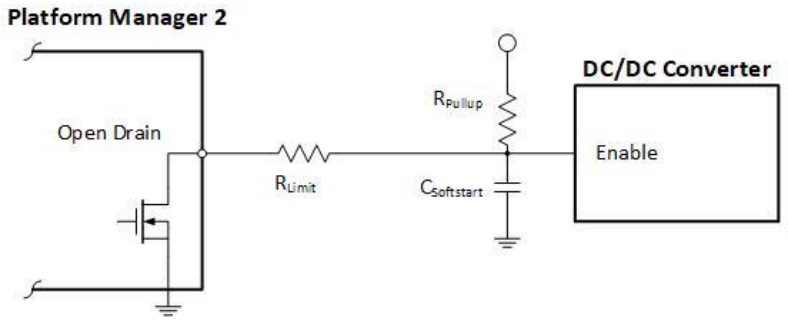

Figure 7.1. Open Drain Current Limit with Capacitor Load

7.5. VMON Pins

VMON pins are used for voltage monitoring. The VMON1 through VMON4 signals are differential and the remaining VMON signals (including HVMON) are single-ended. Connect the VMONx pins to the voltage being monitored, near the load side. For the differential signals the VMONGSx pins are required to be connected to ground. Tie the VMONGS lines close to the low side of the load being measured for accurate differential measurement. Unused VMON pins can be left floating or grounded. There is an internal impedance of 55-75 kΩ to ground on the VMON pins.

When monitoring a voltage or current from a higher voltage source, only the HVIMONN_HVMON and HVIMONP pins can be connected directly to a voltage source which is greater than 5.9 Volts. A voltage divider circuit or other means of isolation is required if using VMON1-9 to monitor a voltage source greater than 5.734 Volts (this is the maximum trip point setting).

7.6. TRIM Pins

Trim pins are special function pins from the TRIM DACs. These pins are used in conjunction with the internal TRIM blocks and use a set of external resistors to bias the reference or feedback node of power supplies. Care should be taken in layout to minimize the parasitic board trace capacitance. TRIM resistors should be located near the DC-DC power supply that is under TRIM control. TRIM pins are associated with a specific VMON input. TRIM1 is associated with VMON1; TRIM2 is associated with VMON2, and so on. Unused TRIM pins can be left floating.

7.7. FPGA PIO Pins

The PIO pins of the FPGA section support various logic standards, both single-ended and differential. There are four PIO banks and each bank has an associated set of VCCIO power supply and ground pins. All PIOs in a given bank are referenced to the VCCIO for that bank. When configured as outputs the PIO output standard must match the VCCIO for that bank (that is, LVCMOS25 outputs must reside in a bank which has VCCIO of 2.5 V). If a PIO is not programmed for use in the software, that pin defaults to an input pin with an internal pull-down resistor. Unused pins can be left floating or tied to GND. The voltage level at the FPGA PIO pin must not exceed 3.6 V. The average DC current drawn by FPGA PIO pins should not exceed 8 mA per pin.

8. Checklist

	Platform Manager 2 Hardware Checklist Item	OK	N/A
1. Power Supply			
1.1	Core Supply VCC and VCCA are at 3.3 V		
1.2	Ferrite bead isolating VCCA from the VCC supply		
1.3	I/O power supply VCCIO0 and VCCIO1 at 3.3 V for LPTM21 (237-Ball ftBGA) based designs		
1.4	I/O power supply VCCIO0 and VCCIO3 at 3.3 V for LPTM21L (100-Ball caBGA) based designs		
1.5	I/O Power supply VCCIO2 at 1.2 V to 3.3 V		
1.6	I/O power supply VCCIO3 at 1.2 V to 3.3 V for LPTM21 (237-Ball ftBGA) based designs		
1.7	All Ground pins connected to ground plane		
1.8	External ASC* has a common ground reference level		
1.9	External ASC* has similar voltage levels		
1.10	Power Estimation		
2. Configuration			
2.1	Configuration options		
2.2	Pull-up on PROGRAMN		
2.3	Pull-up on SPI mode pins		
2.4	Transmission line matching resistor on SPI MCLK output when using the Dual-Boot feature		
2.5	Pull-up on I^2C mode pins		
2.6	JTAG logic levels at 3.3 V and proper pull-up or pull-down resistors used		
2.7	PROGRAMN high-to-low transition time period is larger than the VCC (min) to INITN rising edge time period		
3. ASC Interface and I^2C			
3.1	RESETb connection from all ASCs* to FPGA section, MachXO2, or MachXO3		
3.2	ASCCLK connection only from ASC0 to primary clock pin of MachXO2 or MachXO3 based designs. No ASCCLK connections on LPTM21 or LPTM21L designs		
3.3	Connect external ASC*pins WDAT, RDAT, and WRCLK to Platform Manager 2 FPGA section, MachXO2, or MachXO3 PIO pins		
3.4	SDA_M and SCL_M connected to SDA_S and SCL_S pins on LPTM21 (237-Ball ftBGA) design		
3.5	Connect ASC* SDA and SCL pins to Central Controller (LPTM21, LPTM21L, MachXO2, or MachXO3) SDA and SCL pins		
3.6	Connect ASC* GPIO1 to FPGA PIO pin if using I^2C write protect feature		
3.7	Correct resistor value installed on ASC I2C_ADDR pin for external ACS* devices		
3.8	Connect pullup resistors to set the FPGA section I^2C address on LPTM21L (100-Ball caBGA) Hardware Expanders		
3.9	The die pad of all external ASC devices connected to ground		
4. Analog and I/O Pins			
4.1	Pull up resistors on GPIO pins configured as outputs. Pull-up to 5.5 V or less		
4.2	Series resistor installed near gate for HVOUT pin used in MOSFET driver mode		
4.3	Pull up resistors on HVOUT pins configured as Open-Drain outputs. Pull-up to 13 V or less		
4.4	Series or limit resistor installed on Open-Drain outputs connected to a capacitor load		
4.5	Safe-state of GPIO and HVOUT pins is correct for design		
4.6	VMONGS pins connected to ground for VMON1-VMON4		
4.7	Only HVIMONN_HVMON and HVIMONP pins connected directly to voltages over 5.9 V		
4.8	Trim output 1 matched up to VMON input 1, TRIM2 to VMON2, and others		
4.9	Maximum voltage at FPGA PIO pins is 3.6 V or less		
4.10	Average current drawn by FPGA PIO pins should not exceed 8 mA per pin		

***Note**: External ASC applies to either Hardware Expander; L-ASC10 or LPTM21L.

Appendix A. System Connections Examples

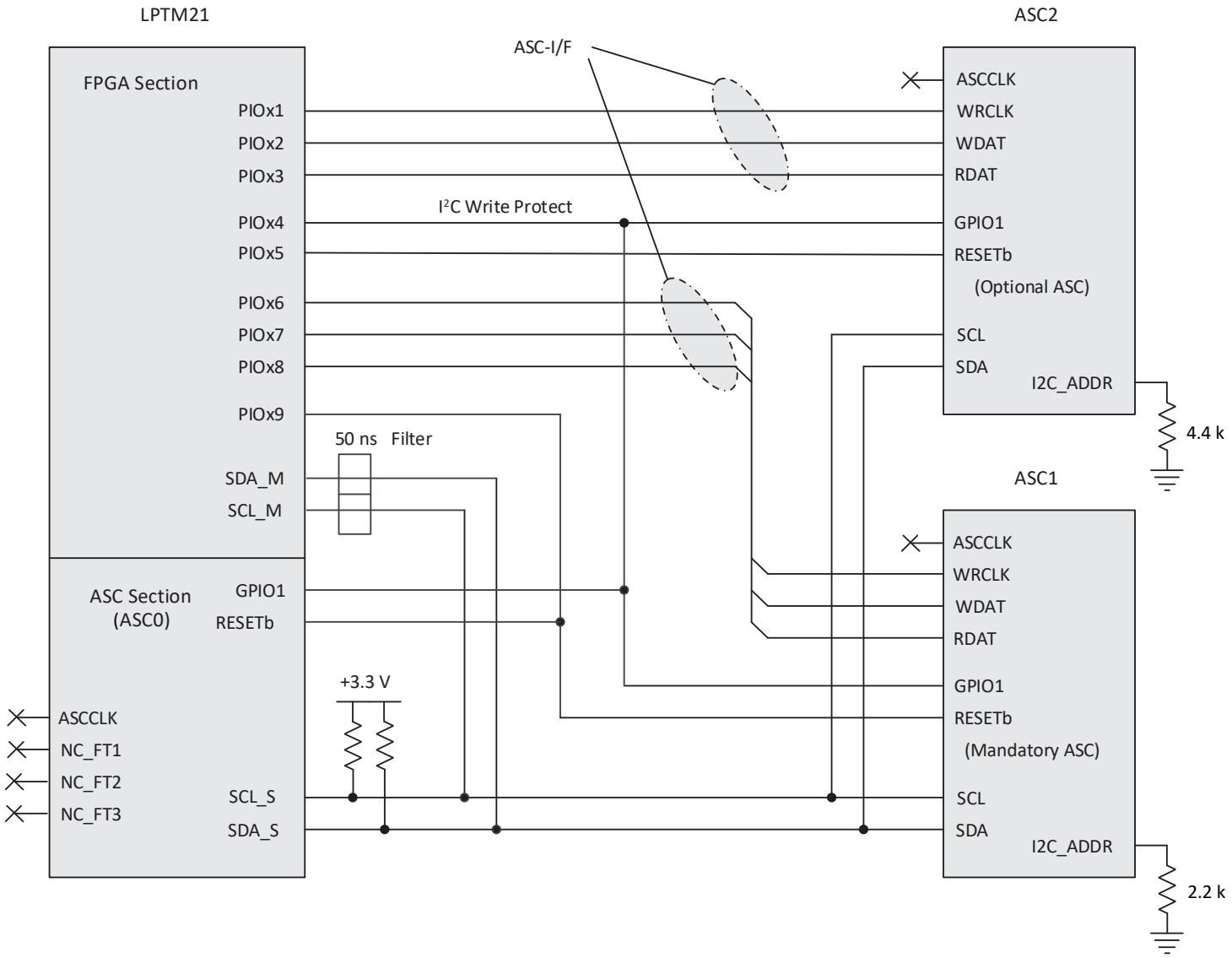

Figure A.1. LPTM21 System Connections Example

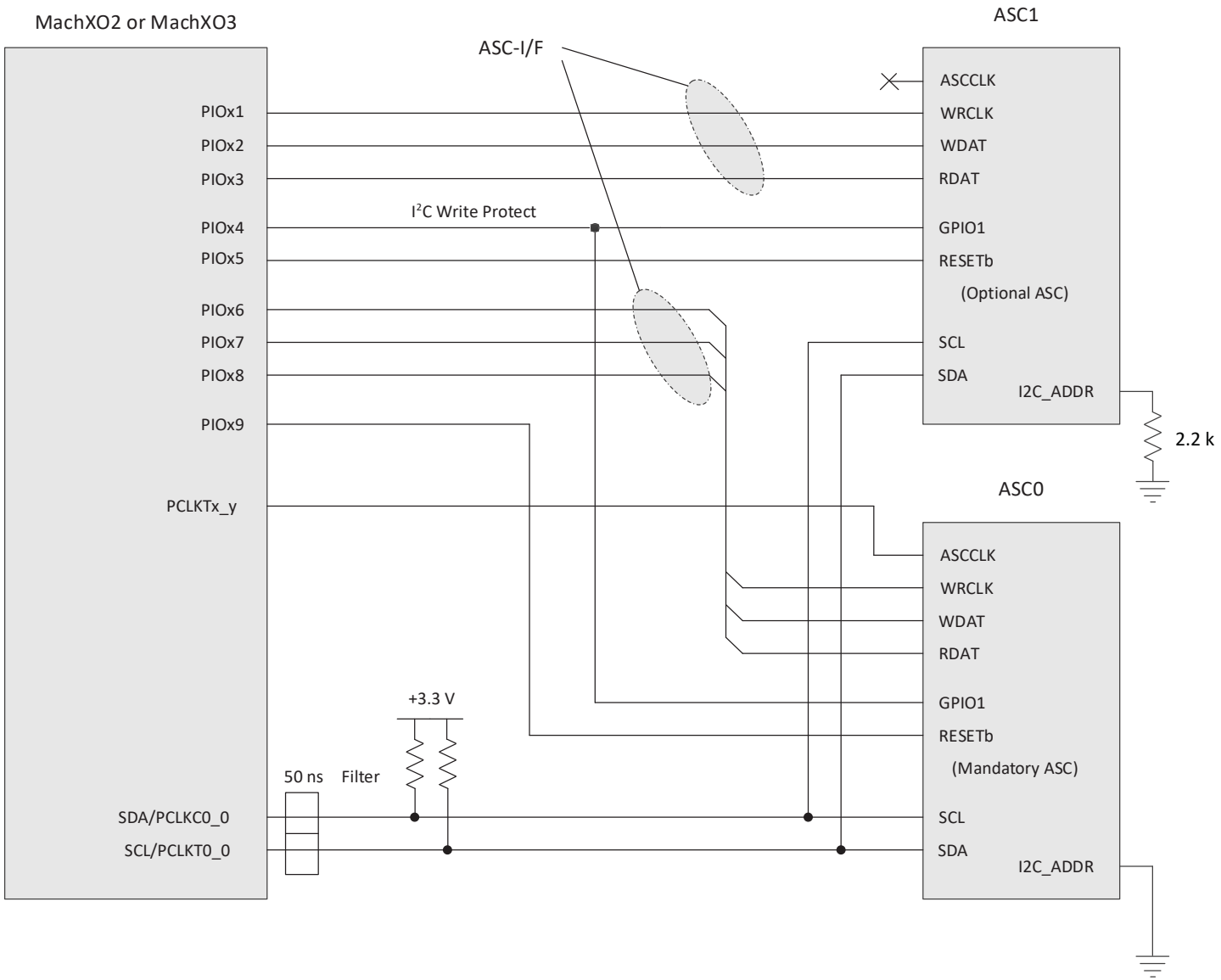

Figure A.2. MachXO2 or MachXO3 and ASC System Connections Example

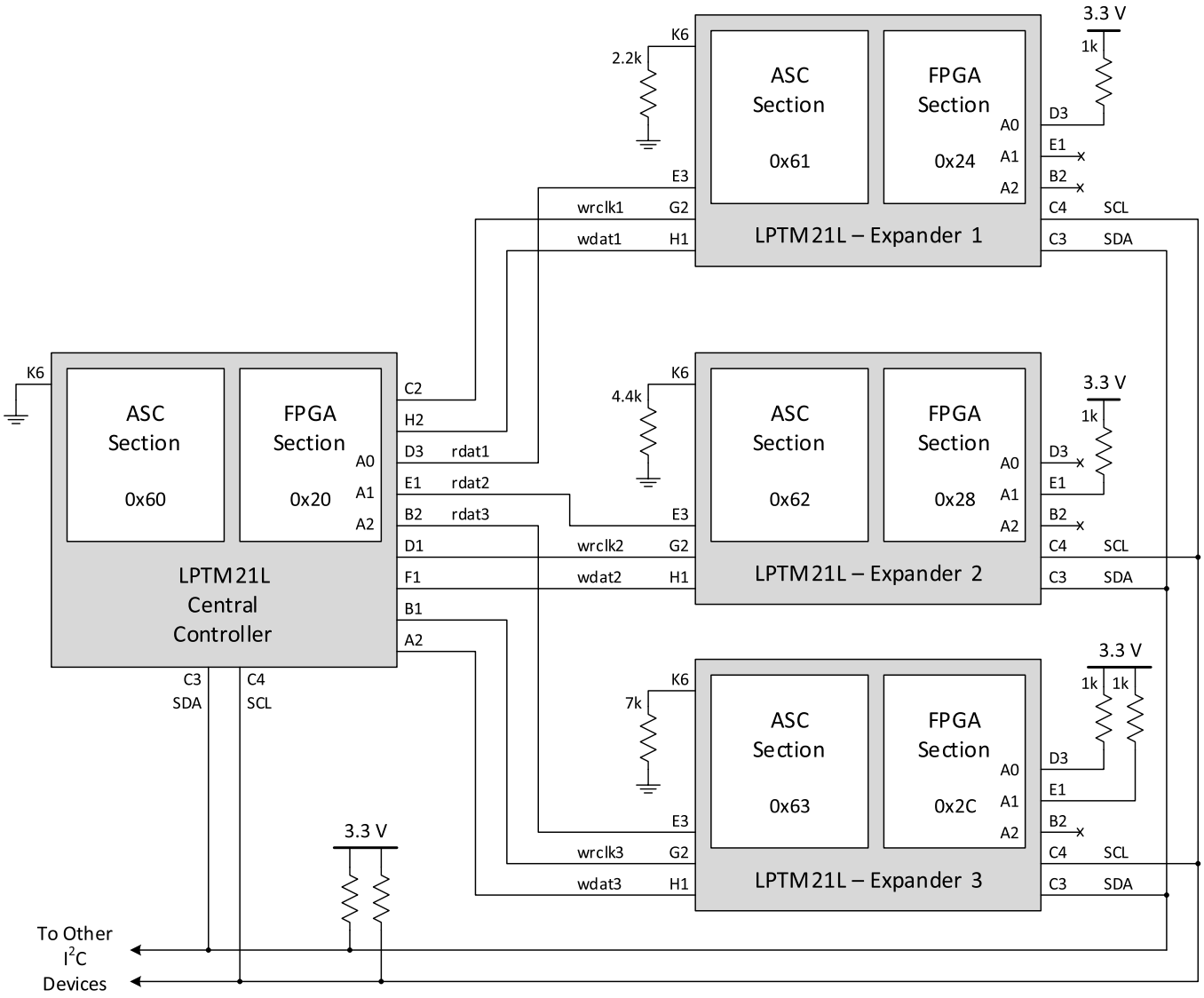

Figure A.3. LPTM21L I²C and ASC-I/F Connections with Three Expander Devices

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Revision 1.2, January 2020

Section	Change Summary
All	• Changed document number from to TN1225 to FPGA-TN-02175. • Updated document template. • Added reference to MachXO3.
Disclaimers	Added this section.
Acronyms in This Document	Added this section.
Introduction	Added references.
Power Supplies	Updated Table 2.1. Power Supply Description and Voltage Levels.
System Connections	• Changed section heading to Setting the I2C Address. • Added ASC Section I2C Address section heading. • Updated Table 6.1. Resistor Values for External ASC I2C_ADDR Pin. • Added FPGA Section I2C Address section.
Checklist	Updated hardware checklist table.
Appendix A. System Connections Examples	• Updated Figure A.1. LPTM21 System Connections Example and Figure A.2. MachXO2 or MachXO3 and ASC System Connections Example. • Added Figure A.3. LPTM21L I2C and ASC-I/F Connections with Three Expander Devices.

Revision 1.1, March 2015

Section	Change Summary
All	General updates: • Changed document title to L-ASC10 and Platform Manager 2 Hardware Checklist. • Added references to L-ASC10. • Removed references to LPTM20. • Updated links to DS1042 and DS1043.
System Connections	Updated I^2C Address Pin section. Clarified I2C_ADDR pin usage in Table 6.1., Resistor Sizes for External ASC I2C_ADDR Pin.
Appendix A	Updated Appendix: System Connections Examples section. Clarified I2C_ADDR pin usage in the following figures: • Figure A.1., LPTM21 System Connections Example • Figure A.2., MachXO2 and ASC System Connections Example Removed the LPTM20 System Connections Example figure.

Revision 1.0, November 2013

Section	Change Summary
All	Initial release.

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