LatticeECP3 Digital Front End Demonstration Design

User's Guide

September 2013
UG68_01.0

Introduction

This document provides technical information and operating instructions for LatticeECP3 Digital Front End (DFE) demonstration (demo) design based on Lattice ECP3 I/O Protocol Board. Lattice DFE demo provides a digital solution consisting of CPRI (Common Public Radio Interface), DUC (Digital Up Converter) and CFR (Crest Factor Reduction) for 2 antenna, LTE (Long-Term Evolution) 2x2 MIMO (Multiple-Input, Multiple-Output) application. The demo design has been designed to work with the LatticeECP3 I/O Protocol Board. The demo uses Ethernet to transfer DFE stimulus and output data between a PC and the board. The stimulus and output data of DFE are stored in on-board DDR3 memory. This document also includes test flow instructions for running the demo on the LatticeECP3 I/O Protocol Board.

Features

- 2.45Gbps CPRI line rate: 2 x 20MHz LTE baseband signals
- Input 20MHz LTE baseband signal bandwidth with 30.72Msps sample rate
- Output data with 122.88Msps sample rate
- DUC (Digital Up Conversion): two antennas, parallel processing
- CFR (Crest Factor Reduction): two stages with total 10 clip engines with two antennas
- DUC and CFR work frequency: 122.88MHz
- Input signed 15-bit I/Q data
- Output signed 16-bit I/Q data
- Gigabit Ethernet connection
- 500Mbps DDR3 data rate

The demo package includes the following:

- Bitstream (in .bit format) for the LatticeECP3-150EA-7, 1156 device
- Scripts and tools for transferring stimulus and output data between a PC and the board
- MATLAB® programs to evaluate the performance of the DFE demo

Demo design hardware requirements:

- LatticeECP3 I/O Protocol Board (revision C) with LatticeECP3-150EA-7, 1156-pin device
- 4GB DDR3 DIMM
- SMA cables for CPRI loopback
- 12V DC power supply
- PC with Gigabit Ethernet connection
- JTAG download cable
- 122.88MHz external clock generator

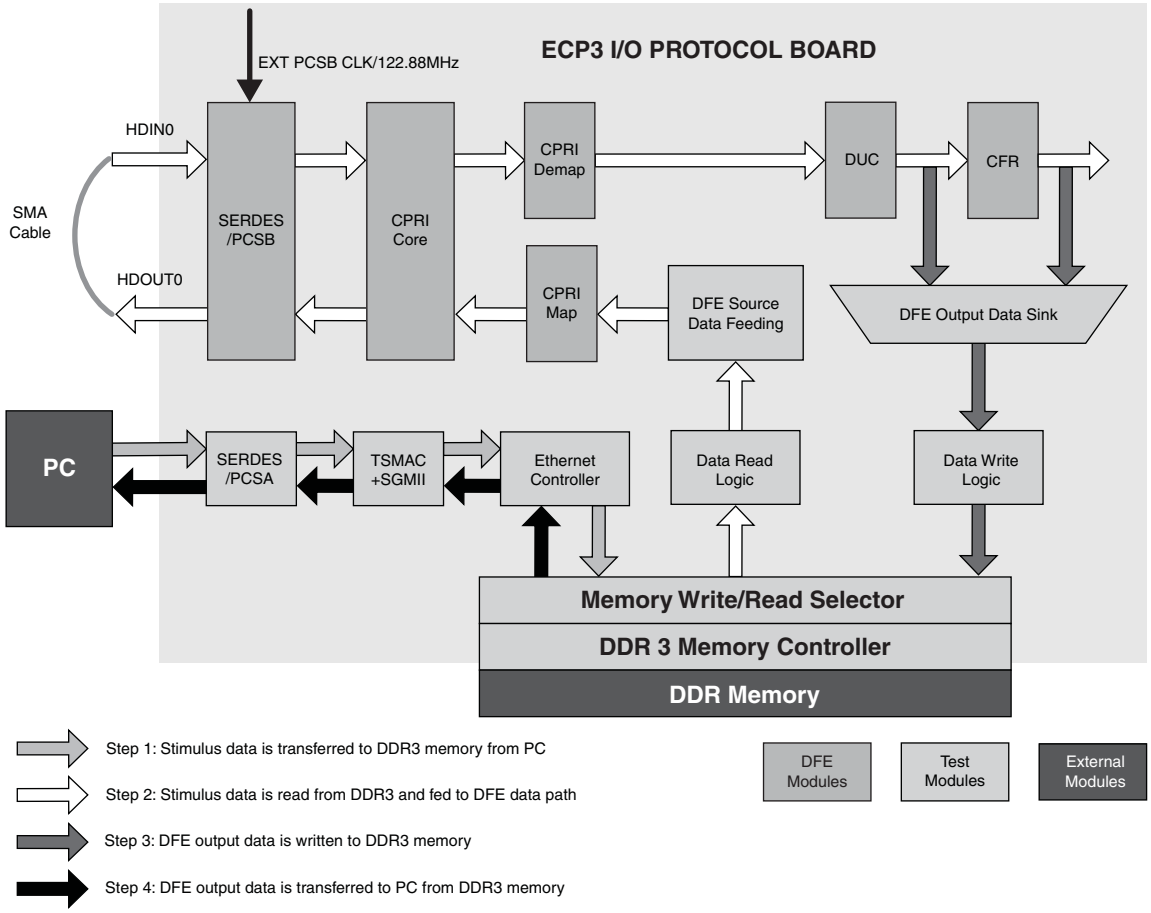
Demo design software requirements:

- Lattice Diamond Programmer (version 2.1 or later) for FPGA bitstream download
- WinPcap (free open source software, version 4.1.2 or later)
- MATLAB (version R2011b or later) or MATLAB Compiler Runtime (version R2012b 32-bit only)

DFE Demo Design Overview

A block diagram of the DFE demo structure is provided in Figure 1.

Figure 1. DFE Demo Structure



The DFE demo consists of three major parts: DFE data path modules, test modules and external modules.

The PCS Quad B (channel 0) on the device is used for CPRI TX/RX with 2.4576 Gbps. Its output (PCSB HDOUT0) is looped back to its input (PCSB HDIN0) by SMA cables. Also the PCS Quad B uses external reference clock with 122.88MHz for CPRI mode.

The PCS Quad A on the device is used in Ethernet mode for Gigabit Ethernet connection.

One 4GB DDR3 DIMM is located on DIMM1 position of the ECP3 I/O Protocol Board.

The DFE data path modules implement CPRI TX/RX, DUC and CFR functions with 2 antennas for LTE transmit downlink application. The input baseband data is a 20MHz bandwidth signal with 30.72Msps sample rate. The DFE output sample rate is 122.88Msps. The DFE input baseband data is 15-bit signed I/Q samples and the output data is 16-bit signed I/Q samples. The internal processing of DUC and CFR uses 18-bit precision.

The test modules implement the hardware test-bench and the test environment, including DFE stimulus / output data transfer between PC and on-board DDR3 memory, DFE input data feed from DDR3 memory and output data sink to DDR3 memory. DFE stimulus data is a 20MHz baseband signal with 30.72Msps (FFT size is 2048, modulation scheme is 16 QAM). The number of DFE stimulus is 22K I/Q pairs.

CPRI Interface

DFE data path uses a single-channel CPRI core with 2.4576Gbps. The CPRI core is configured as REC (Radio Equipment Control) for loopback function. The PCSB serializes the data in the transmit direction, and de-serializes it in the receive direction. The encoded serial data stream can be looped back externally via I/O buffer serial loop-back or via cables using the on-board SMA connectors. In this demo, we use external SMA cables for loopback.

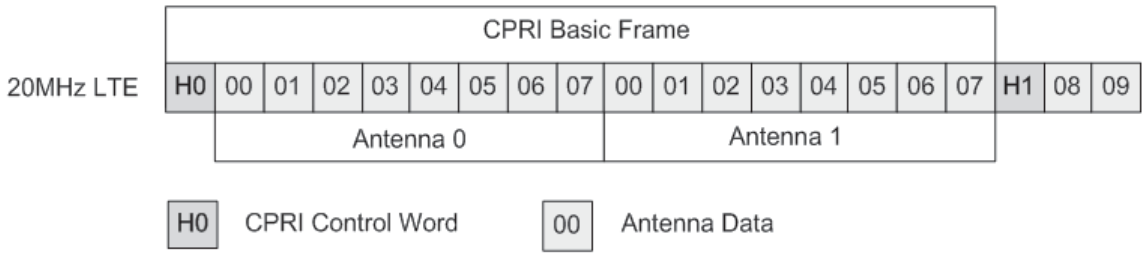
Figure 2 shows the CPRI data mapping format. Figure 3 shows the CPRI LTE sample packing for 2 x 20MHz antennas. The CPRI data mapping format is compatible with TI AIF2 (Antenna Interface 2).

The bit-width of the I/Q samples is 15 bits. CPRI basic frame has 16 words. The word with the index W=0, 1/16 of the basic frame, is used for one control word. Each basic frame contains 8 I/Q sample pairs for antenna 0 and antenna 1. The total 16 I/Q sample pairs are mapped into 15 words in each basic frame.

Figure 2. CPRI Data Mapping

		Antenna 0								Antenna 1							
	CW	A0	A1	A2	A3	A4	A5	A6	A7	A0	A1	A2	A3	A4	A5	A6	A7
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
LSB:0	Control Word	I0,0	I1,1	I2,2	I3,3	I4,4	I5,5	I6,6	I7,7	I0,8	I1,9	I2,10	I3,11	I4,12	I5,13	I6,14	
		Q0,0	Q1,1	Q2,2	Q3,3	Q4,4	Q5,5	Q6,6	Q7,7	Q0,8	Q1,9	Q2,10	Q3,11	Q4,12	Q5,13	Q6,14	
		I0,1	I1,2	I2,3	I3,4	I4,5	I5,6	I6,7	I7,8	I0,9	I1,10	I2,11	I3,12	I4,13	I5,14	I7,0	
		Q0,1	Q1,2	Q2,3	Q3,4	Q4,5	Q5,6	Q6,7	Q7,8	Q0,9	Q1,10	Q2,11	Q3,12	Q4,13	Q5,14	Q7,0	
		I0,2	I1,3	I2,4	I3,5	I4,6	I5,7	I6,8	I7,9	I0,10	I1,11	I2,12	I3,13	I4,14	I6,0	I7,1	
		Q0,2	Q1,3	Q2,4	Q3,5	Q4,6	Q5,7	Q6,8	Q7,9	Q0,10	Q1,11	Q2,12	Q3,13	Q4,14	Q6,0	Q7,1	
		I0,3	I1,4	I2,5	I3,6	I4,7	I5,8	I6,9	I7,10	I0,11	I1,12	I2,13	I3,14	I5,0	I6,1	I7,2	
		Q0,3	Q1,4	Q2,5	Q3,6	Q4,7	Q5,8	Q6,9	Q7,10	Q0,11	Q1,12	Q2,13	Q3,14	Q5,0	Q6,1	Q7,2	
	Control Word	I0,4	I1,5	I2,6	I3,7	I4,8	I5,9	I6,10	I7,11	I0,12	I1,13	I2,14	I4,0	I5,1	I6,2	I7,3	
		Q0,4	Q1,5	Q2,6	Q3,7	Q4,8	Q5,9	Q6,10	Q7,11	Q0,12	Q1,13	Q2,14	Q4,0	Q5,1	Q6,2	Q7,3	
		I0,5	I1,6	I2,7	I3,8	I4,9	I5,10	I6,11	I7,12	I0,13	I1,14	I3,0	I4,1	I5,2	I6,3	I7,4	
		Q0,5	Q1,6	Q2,7	Q3,8	Q4,9	Q5,10	Q6,11	Q7,12	Q0,13	Q1,14	Q3,0	Q4,1	Q5,2	Q6,3	Q7,4	
		I0,6	I1,7	I2,8	I3,9	I4,10	I5,11	I6,12	I7,13	I0,14	I2,0	I3,1	I4,2	I5,3	I6,4	I7,5	
		Q0,6	Q1,7	Q2,8	Q3,9	Q4,10	Q5,11	Q6,12	Q7,13	Q0,14	Q2,0	Q3,1	Q4,2	Q5,3	Q6,4	Q7,5	
		I0,7	I1,8	I2,9	I3,10	I4,11	I5,12	I6,13	I7,14	I1,0	I2,1	I3,2	I4,3	I5,4	I6,5	I7,6	
		Q0,7	Q1,8	Q2,9	Q3,10	Q4,11	Q5,12	Q6,13	Q7,14	Q1,0	Q2,1	Q3,2	Q4,3	Q5,4	Q6,5	Q7,6	
	Control Word	I0,8	I1,9	I2,10	I3,11	I4,12	I5,13	I6,14	I0,0	I1,1	I2,2	I3,3	I4,4	I5,5	I6,6	I7,7	
		Q0,8	Q1,9	Q2,10	Q3,11	Q4,12	Q5,13	Q6,14	Q0,0	Q1,1	Q2,2	Q3,3	Q4,4	Q5,5	Q6,6	Q7,7	
		I0,9	I1,10	I2,11	I3,12	I4,13	I5,14	I7,0	I0,1	I1,2	I2,3	I3,4	I4,5	I5,6	I6,7	I7,8	
		Q0,9	Q1,10	Q2,11	Q3,12	Q4,13	Q5,14	Q7,0	Q0,1	Q1,2	Q2,3	Q3,4	Q4,5	Q5,6	Q6,7	Q7,8	
		I0,10	I1,11	I2,12	I3,13	I4,14	I6,0	I7,1	I0,2	I1,3	I2,4	I3,5	I4,6	I5,7	I6,8	I7,9	
		Q0,10	Q1,11	Q2,12	Q3,13	Q4,14	Q6,0	Q7,1	Q0,2	Q1,3	Q2,4	Q3,5	Q4,6	Q5,7	Q6,8	Q7,9	
		I0,11	I1,12	I2,13	I3,14	I5,0	I6,1	I7,2	I0,3	I1,4	I2,5	I3,6	I4,7	I5,8	I6,9	I7,10	
		Q0,11	Q1,12	Q2,13	Q3,14	Q5,0	Q6,1	Q7,2	Q0,3	Q1,4	Q2,5	Q3,6	Q4,7	Q5,8	Q6,9	Q7,10	
	Control Word	I0,12	I1,13	I2,14	I4,0	I5,1	I6,2	I7,3	I0,4	I1,5	I2,6	I3,7	I4,8	I5,9	I6,10	I7,11	
		Q0,12	Q1,13	Q2,14	Q4,0	Q5,1	Q6,2	Q7,3	Q0,4	Q1,5	Q2,6	Q3,7	Q4,8	Q5,9	Q6,10	Q7,11	
		I0,13	I1,14	I3,0	I4,1	I5,2	I6,3	I7,4	I0,5	I1,6	I2,7	I3,8	I4,9	I5,10	I6,11	I7,12	
		Q0,13	Q1,14	Q3,0	Q4,1	Q5,2	Q6,3	Q7,4	Q0,5	Q1,6	Q2,7	Q3,8	Q4,9	Q5,10	Q6,11	Q7,12	
		I0,14	I2,0	I3,1	I4,2	I5,3	I6,4	I7,5	I0,6	I1,7	I2,8	I3,9	I4,10	I5,11	I6,12	I7,13	
		Q0,14	Q2,0	Q3,1	Q4,2	Q5,3	Q6,4	Q7,5	Q0,6	Q1,7	Q2,8	Q3,9	Q4,10	Q5,11	Q6,12	Q7,13	
		I1,0	I2,1	I3,2	I4,3	I5,4	I6,5	I7,6	I0,7	I1,8	I2,9	I3,10	I4,11	I5,12	I6,13	I7,14	
MSB:31		Q1,0	Q2,1	Q3,2	Q4,3	Q5,4	Q6,5	Q7,6	Q0,7	Q1,8	Q2,9	Q3,10	Q4,11	Q5,12	Q6,13	Q7,14	

Figure 3. CPRI LTE Sample Packing

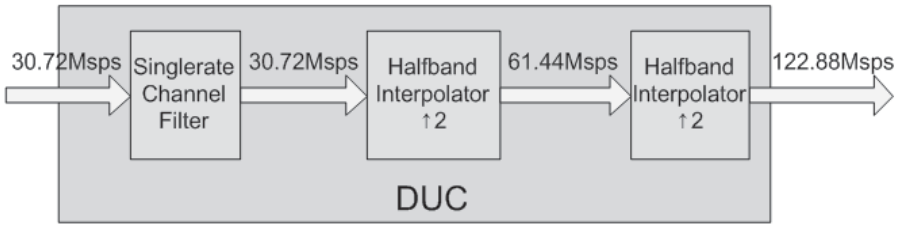


DUC Module

Figure 4 shows the overview block diagram of the DUC.

Channel filter is a single rate filter, used to filter the input LTE baseband data to attenuate the out-of-band power to meet the spectral mask requirements. After the channel filter, two stages of halfband interpolation filters are used to remove the aliasing effect produced by up sampling. And each halfband filter's interpolation factor is 2, which has an optimized implementation structure to save resource. The input data sample rate of DUC is 30.72Msps and the output sample rate is 122.88Msps, while the DUC modules' operational frequency is 122.88MHz. The channel filter and the first halfband interpolator use TDM (Time Division Multiplexing) mode to save resource.

Figure 4. Structure of DUC



CFR Core

Lattice CFR core is a PC-CFR (Peak Cancellation Crest Factor Reduction) design. CFR core selectively reduces the peak-to-average ratio (PAR) of wideband digital signals, such as those used in 3G CDMA (third-generation Code Division Multiple Access) or LTE (Long Term Evolution) wireless applications.

In the DFE demo, CFR is configured as two stages with total 10 clip engines for performance, resource and latency trade-off. For increased PAR reduction, the CFR core can be configured with more number of stages and/or clip engines. The target peak threshold is 7dB. The coefficients of the cancellation pulse filter are real type. CFR operational frequency is 122.88MHz.

Ethernet Interface

The Ethernet interface of the demo is Gigabit Ethernet connection. LED D15 on the board is Gigabit connection indicator. When the board is powered on and connected with a PC Gigabit network card, LED D15 will be lit.

DFE demo package provides tools for sending and capturing Ethernet packets and extracting data from the packets. The software WinPcap must be installed in the PC as Ethernet driver before running the demo. It is free software and can be downloaded at www.winpcap.org.

DDR3 Memory

DFE demo uses one 4GB DDR3 DIMM on DIMM1 of the board. The DDR3 memory data rate is 500Mbps. Since both Ethernet and DFE access the DDR3 memory, a simple memory read/write selector is used for arbitration.

The demo has 4 main steps of operation. The first step is transferring DFE stimulus data from PC to the board DDR3 memory by Ethernet interface. Then the stimulus data is read from DDR3 memory and fed to the DFE data path. When the DFE sink detects the output of DUC and CFR, it gathers the output data and sends it to DDR3 memory. In the final step, the output data of DUC and CFR is read from the DDR3 memory to the PC through the Ethernet interface.

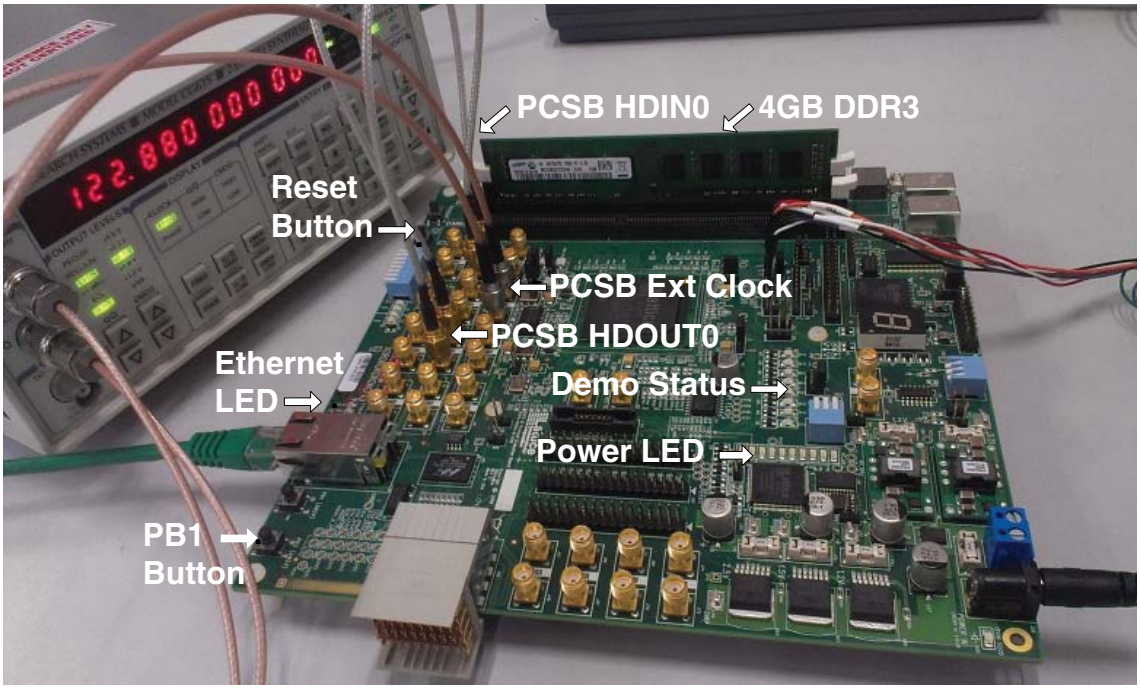
The demo package provides the scripts and tools for sending and reading data between PC and on board DDR3 memory. Also the demo package provides some Matlab programs to evaluate the performance metrics for the DFE design, including source LTE baseband data PSD (Power Spectral Density), post-DUC output data PSD, post-CFR output data PSD and CCDF (Complementary Cumulative Distribution Function) between CFR input data and CFR output data. These performance metrics can be used to verify if the DFE design meets the spectral mask requirements of LTE.

LatticeECP3 I/O Protocol Board (Version C) Setup

The DFE demo transfers and receives data between a PC and on board DDR3 memory. Figure 5 shows LatticeECP3 I/O Protocol Board setup and connections. The setup assumes the following:

- Lattice Diamond Programmer (version 2.1 or later) is installed on the PC.
- WinPcap (version 4.1.2 or later) is installed on the PC.
- 4GB DDR3 memory DIMM is installed in the DIMM1 slot of the board.
- PCSB HDOUT0 is connected with PSCB HDIN0 through SMA cables.
- 122.88 MHz external differential clock source is connected with PCSB Ext Clock input through SMA cables.
- The JTAG Connector on the board is connected to an USB port of the PC using a Lattice USB download cable
- The RJ45 slot on the board is connected to PC network card using an Ethernet cable.
- Power is applied to the board via the provided power supply.

Figure 5. LatticeECP3 I/O Protocol Board Setup



DFE Demo Control Signals and Status Descriptions

Table 1 lists all the DFE Demo control signals and status LEDs. Table 2 shows the detailed description of Demo status LEDs.

Table 1. DFE Demo Control Signals and Status LEDs

Name	Board Connection	Description
Reset Button	GSRN	FPGA global active low reset.
Power LED	On board power good LEDs	Power good indicator.
Ethernet LED	DUPLEX, LINK 1000	Gigabit Ethernet connection indicator.
Demo Status	LED D6 - D12, D14	DFE demo status indicators. See Table 2 for details.
PCSB HDIN0	PCSB HDIN0	CPRI input port for DFE stimulus data.
PCSB HDOUT0	PCSB HDOUT0	CPRI output port for DFE stimulus data.
PCSB Ext Clock	PCSB Ext Clock	CPRI external reference clock.

Table 2. Description of Demo Status LEDs

Name	Board Connection	Description
LED7	D7	CFR done. Off: Not finished. On: CFR output data written to memory.
LED6	D8	DUC done. Off: Not finished. On: DUC output data written to memory.
LED5	D11	Ethernet Write. Off: No activity; On: Ethernet writing data to the DDR3 memory.
LED4	D14	CPRI link status. Off: Failed; On: Link OK.
LED3	D12	Ethernet Auto Negotiation. Off: Failed; On: AutoNeg done.
LED2	D10	Not used.
LED1	D9	Not used.
LED0	D6	Not used.

DFE Demo Package Directory Structure

Figure 6 shows DFE demo package directory and Table 3 gives the detailed description.

Figure 6. DFE Demo Package Directory

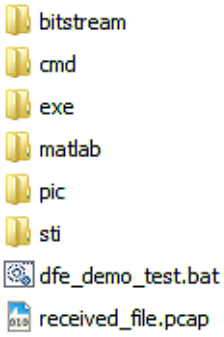


Table 3. DFE Demo Package Directory Description

Files	Description
\bitstream\ dfe_demo_eclk.bit	DFE demo bitstream with external CPRI reference clock.
\bitstream\ dfe_demo_iclk.bit	DFE demo bitstream with internal CPRI reference clock.
\bitstream\ dfe_demo_iclk_1.5db.bit	DFE demo bitstream with internal CPRI reference clock with 1.5dB PAR reduction.
\bitstream\ dfe_demo_iclk_3db.bit	DFE demo bitstream with internal CPRI reference clock with 3dB PAR reduction.
\cmd	Ethernet command packets for data write/read.
\exe	Exe files for send and capture Ethernet packets.
\matlab	DFE performance evaluating files.
\matlab\demo_in.dat	DFE stimulus data file.
\matlab\demo_test.exe	Standalone executable DFE performance evaluation tool.
\matlab\demo_test.m	DFE performance evaluation tool.
\matlab\plotCCDF.p	Plot CCDF curve tool.
\matlab\plotPSD.p	Plot PSD curve tool.
\pic	DFE demo photo
\sti	DFE input stimulus in Ethernet packets format.
dfe_demo_test.bat	Batch file for DFE demo test.
received_file.pcap	Packets captured file by running demo test

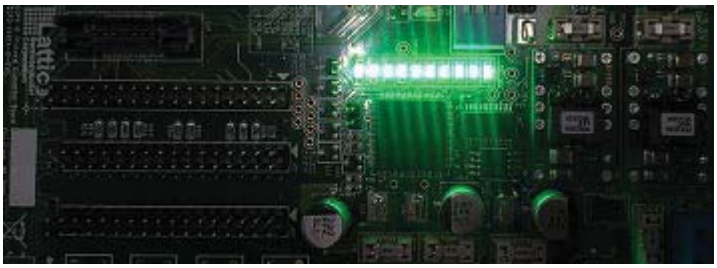
Running the DFE Demo

This section describes the detailed test flow of the DFE demo.

1. Make sure that the demo connection is established and operating correctly.

Power on the LatticeECP3 I/O Protocol Board. Check whether the power LEDs are ON.

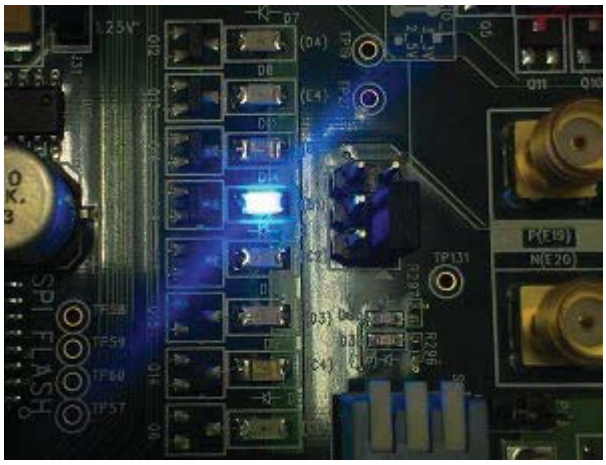
Figure 7. Power ON LEDs



2. Download the demo bitstream.

Use Fast Program in the Diamond Programmer tool to download the bitstream under \bitstream\dfe_demo_iclk.bit or \bitstream\dfe_demo_eclk.bit to the SRAM. After downloading the bitstream, the DFE status LED is shown in Figure 8.

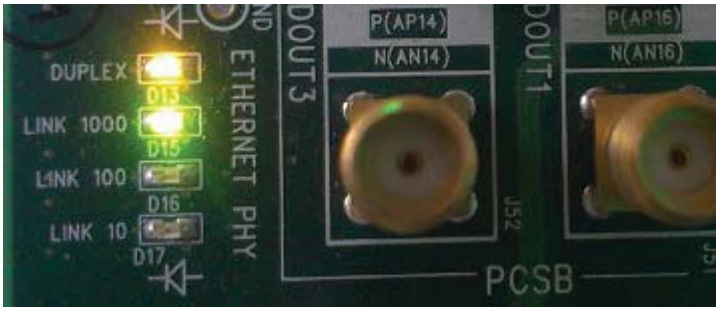
Figure 8. DFE Status LEDs after the Demo Bitstream is Downloaded



3. Check Ethernet status indicator.

Check whether then Ethernet status indicator is ON and the link 1000 is ON. The demo will only work with the 1G Ethernet link, so need to make sure the PC network adapter card supports that. Normally, after powering on the board, the Ethernet status indicator lights up as shown in Figure 9.

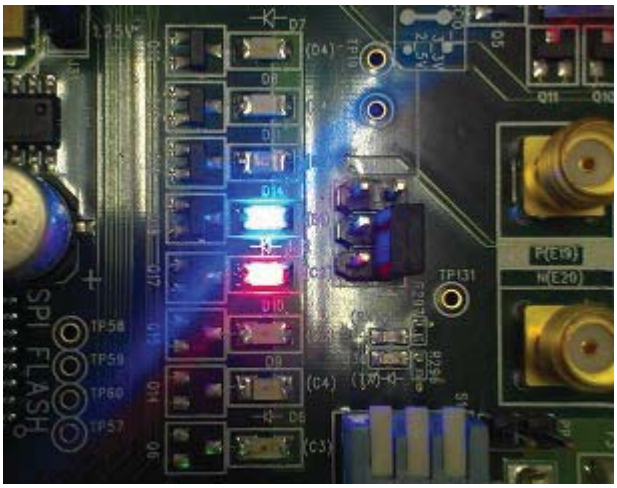
Figure 9. Ethernet Link 1000 Indicator



If the status indicator does not light up, after downloading the bitstream, press the PB1 button on the board to reset the Ethernet PHY. The status indicator lights up after a few seconds.

4. Press the reset button to make sure that the Ethernet Auto Negotiation is done and CPRI link is established. Figure 10 shows the DFE status LEDs after the reset button is pressed.

Figure 10. DFE Status LEDs After the Reset Button is Pressed



After these are checked, you can be assured that the board is working correctly.

5. Run the Demo test.

Run the *dfe_demo_test.bat* file to view the ID of the network cards. Below is an example:

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C:\temp\dfe_demo>exe\capture_packet.exe

1.   rpcap://\Device\NPF_{139B229C-1D20-4FB6-9E77-0D6C9323F4E2}   (Network   adapter
'Microsoft' on local host)

2.   rpcap://\Device\NPF_{DEA99698-A1DA-445A-A04F-285E52FBD9C7}   (Network   adapter
'Intel(R) 82577LM Gigabit Network Connection' on local host)

3.   rpcap://\Device\NPF_{58568485-AF5B-4776-B858-28C5A966C5C9}   (Network   adapter
'Microsoft' on local host)

Enter the interface number (1-3):

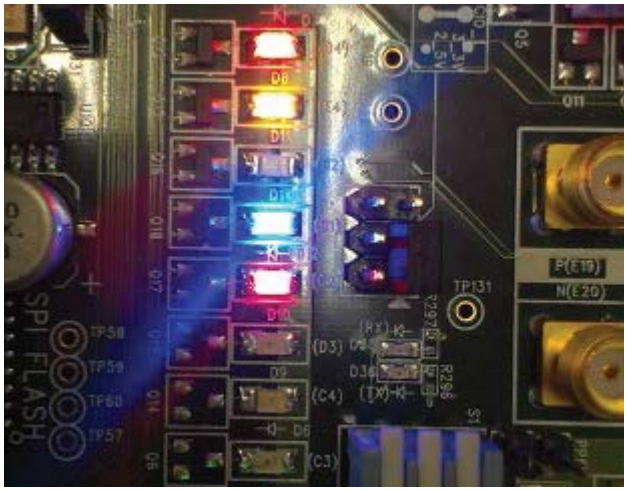
-------------------------------------------------------------------------------------------------------------
```

You can identify that the Gigabit Network Card is on interface 2.

Select the correct network card ID to capture the Ethernet packets. This starts the DFE demo test. Depending on PC performance, the DFE demo test takes about 15 seconds to 1 minute to complete.

After the test is completed, the command window closes and LED7 and LED8 light up as shown in Figure 11.

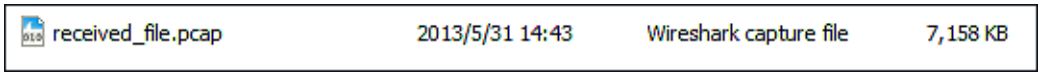
Figure 11. DFE Status LEDs After the Test is Completed



If LED7 and LED8 do not light up, press the reset button and re-run the demo test.

When the demo test is completed, the *received_file.pcap* packet file is generated. Refresh and check that the file size of the *received_file.pcap* is 7,158KB.

Figure 12. Packet File Size



6. Evaluate the DFE performance.

Run MATLAB software and go to the path *dfe_demo\matlab*.

Run *demo_test.m*. The script runs the evaluation and the diagrams of PSD and CCDF are shown.

if you do not have MATLAB license, you may install MATLAB Compiler Runtime first and run demo_test.exe to evaluate the demo. MATLAB Compiler Runtime can be downloaded at www.mathworks.com/products/compiler/mcr/.

Evaluating the DFE Demo Performance

Figure 13 to Figure 15 show the PSD of DFE demo input (LTE baseband data), post-DUC output data, and post-CFR output data.

Figure 13. PSD of the LTE Baseband Data with 20MHz Bandwidth

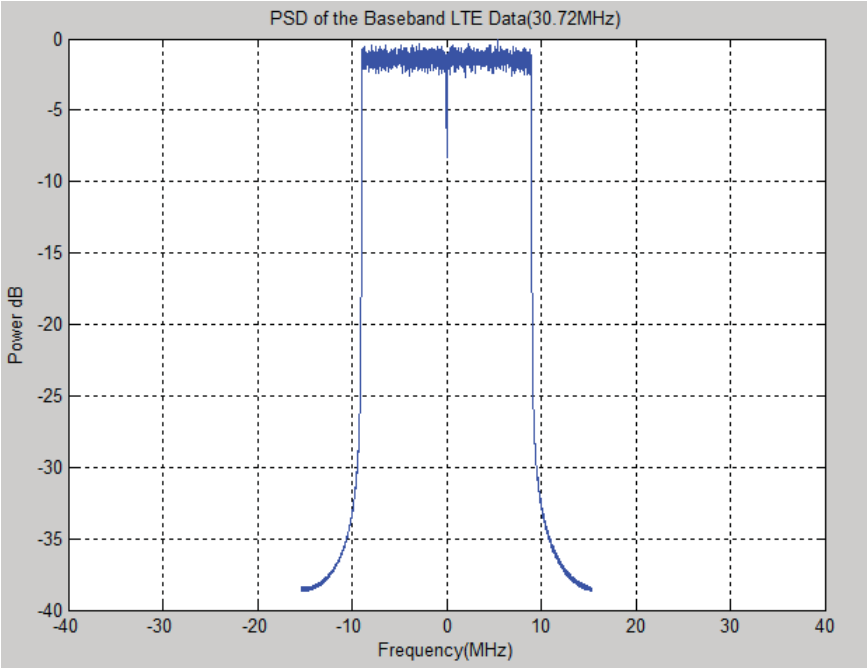


Figure 14. PSD of the Post-DUC Data with 20MHz Bandwidth

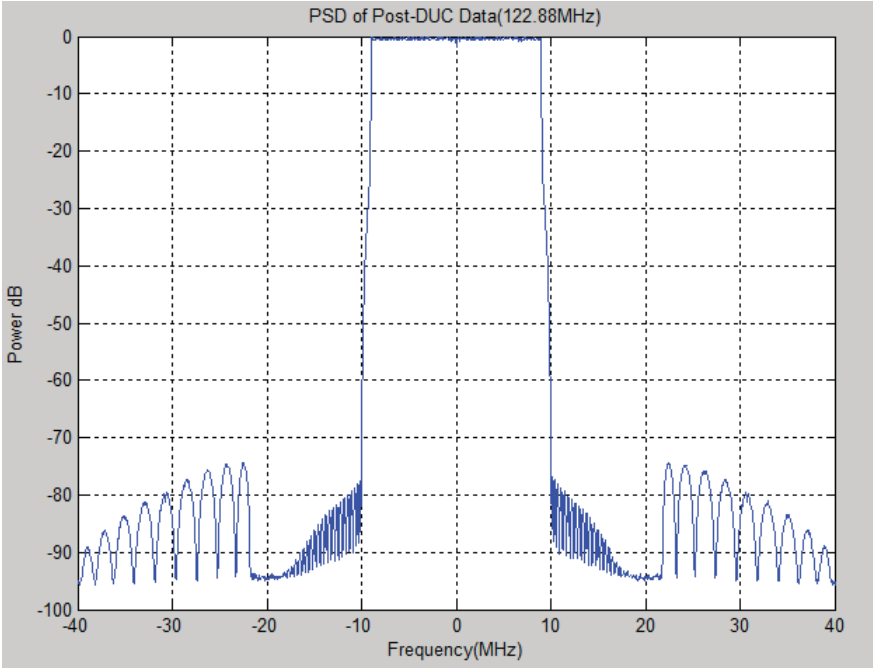


Figure 15. PSD of the Post-CFR Data with 20MHz Bandwidth

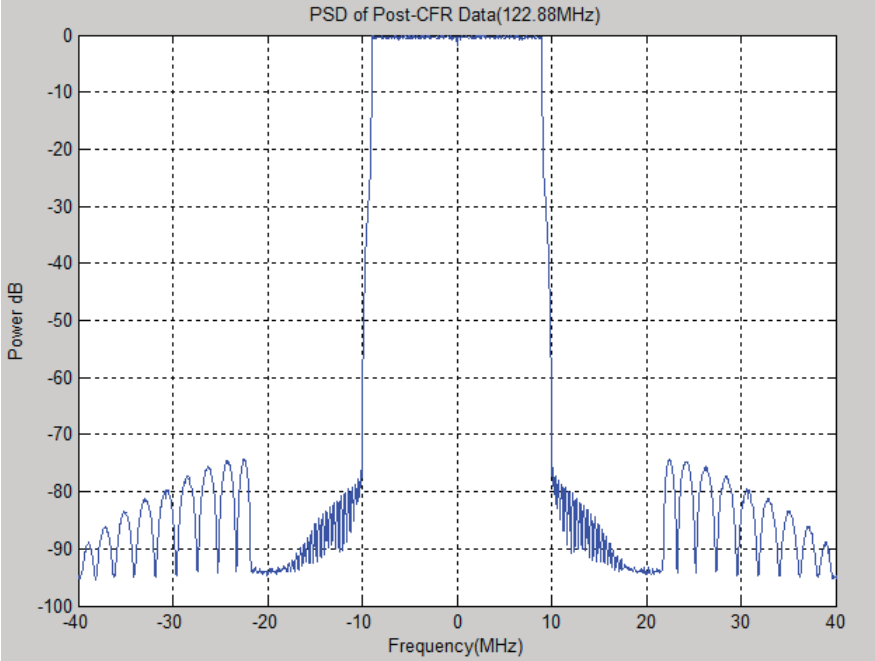


Figure 16 and Figure 18 show the CCDF and signal amplitudes of CFR input and output data. Figure 18 shows the EVM (Error Vector Magnitude) vs PAR of CFR performance. We can see that the demo could achieve CFR performance of 4 dB PAR reduction.

Figure 16. CCDF of CFR Input and Output with 20MHz Bandwidth

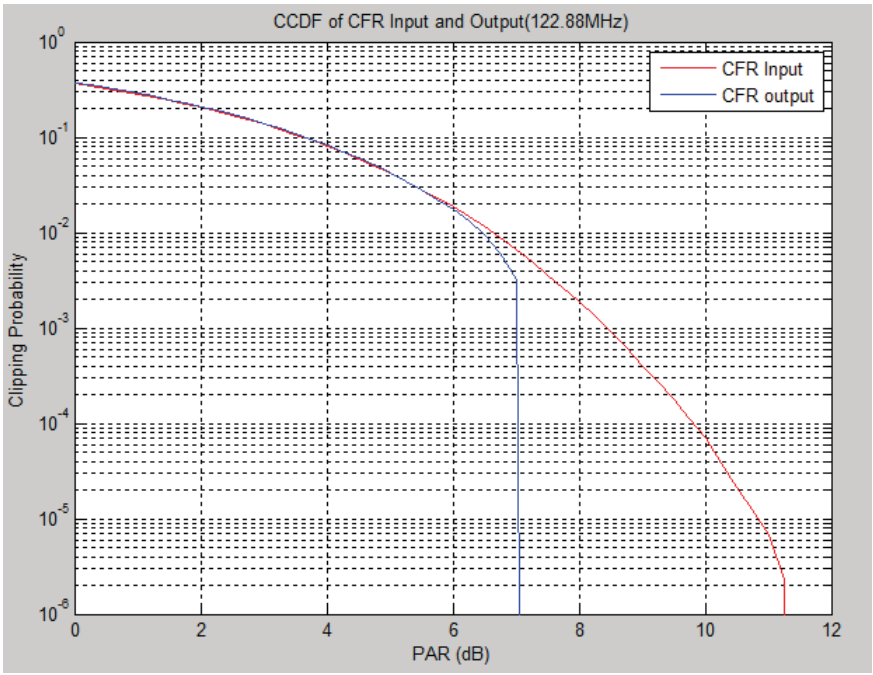


Figure 17. Signal Amplitudes of CFR Input and Output

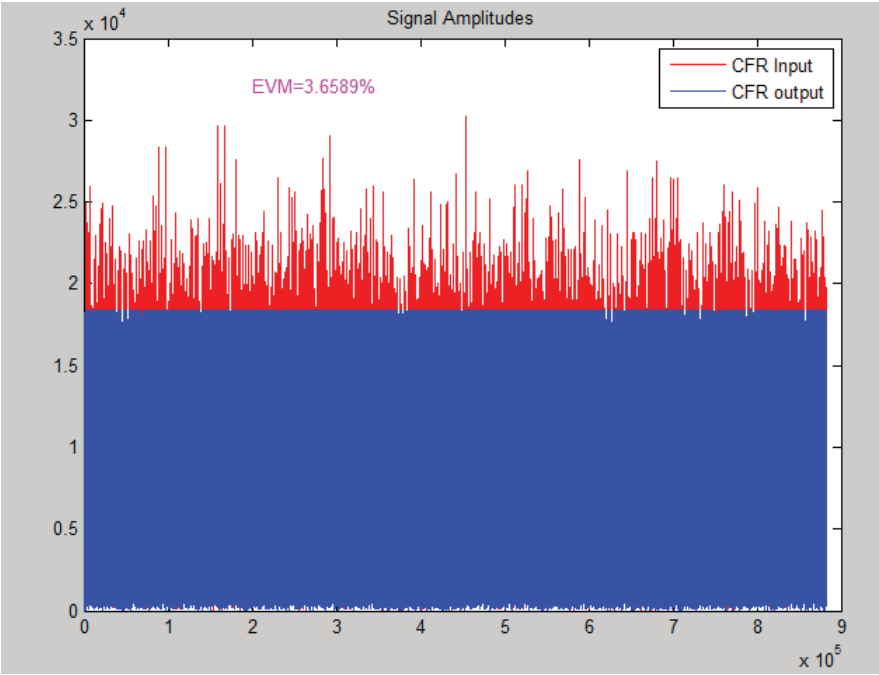
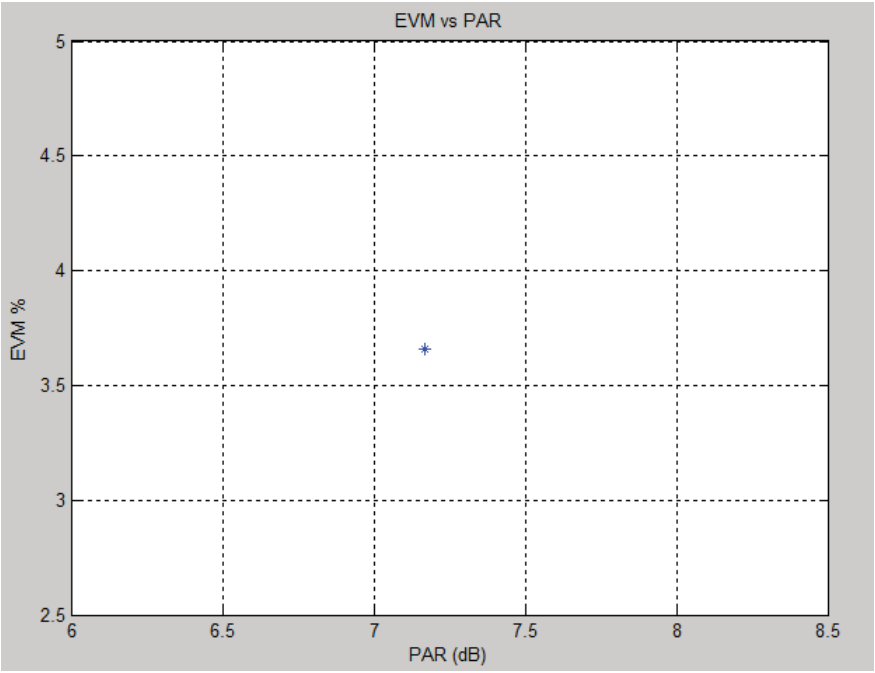


Figure 18. EVM vs PAR of CFR



There are also two other bitstreams for CFR performance and resource cost trade-off.

Running the demo with *dfe_demo_iclk_3db.bit* results in a CFR performance shown in Figure 19 and Figure 20.

Figure 19. CCDF of CFR Input and Output for dfe_demo_iclk_3db.bit

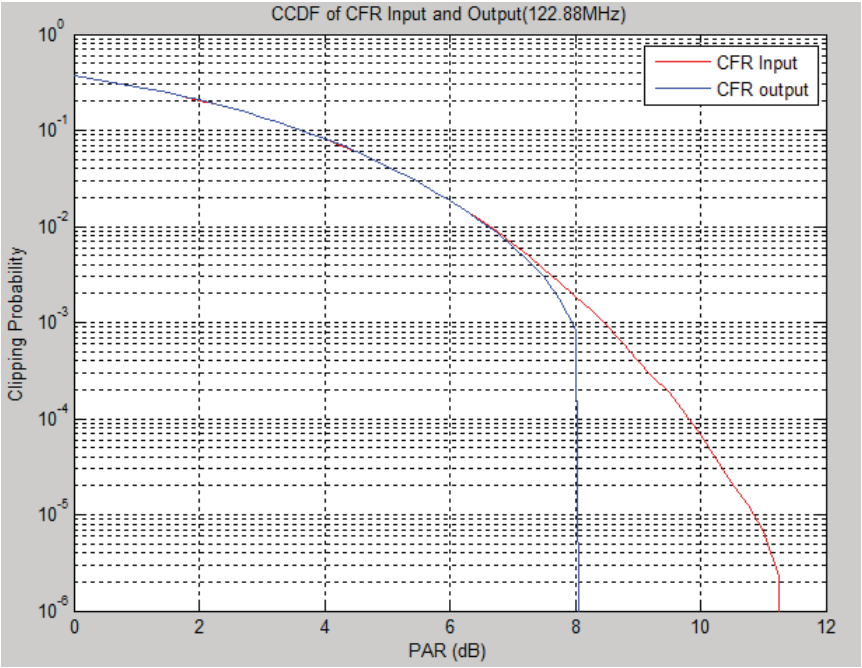
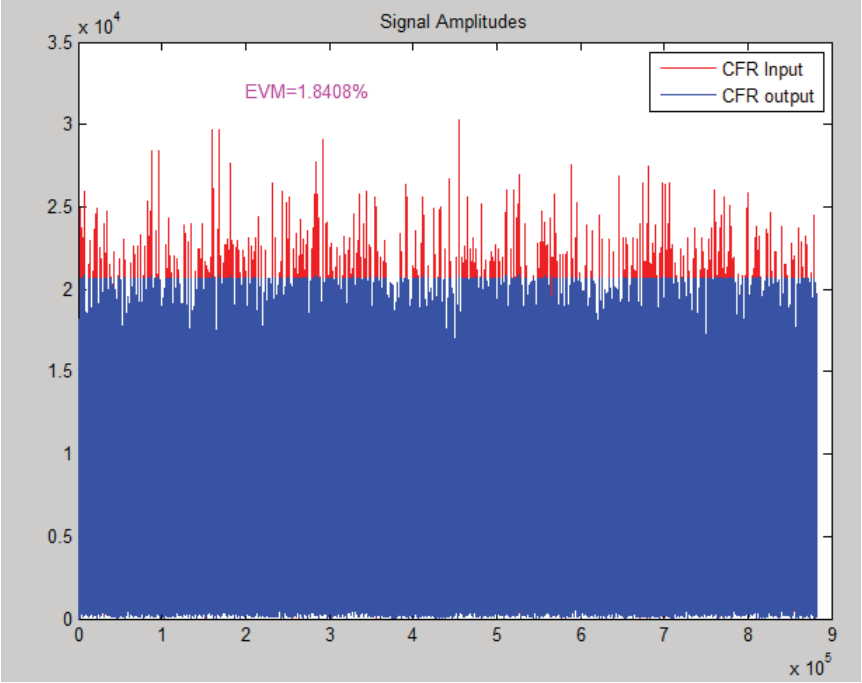


Figure 20. Signal Amplitudes of CFR Input and Output for dfe_demo_iclk_3db.bit



Running the demo with *dfe_demo_iclk_1.5db.bit* results in CFR performance shown in Figure 21 and Figure 22.

Figure 21. CCDF of CFR Input and Output for dfe_demo_iclk_1.5db.bit

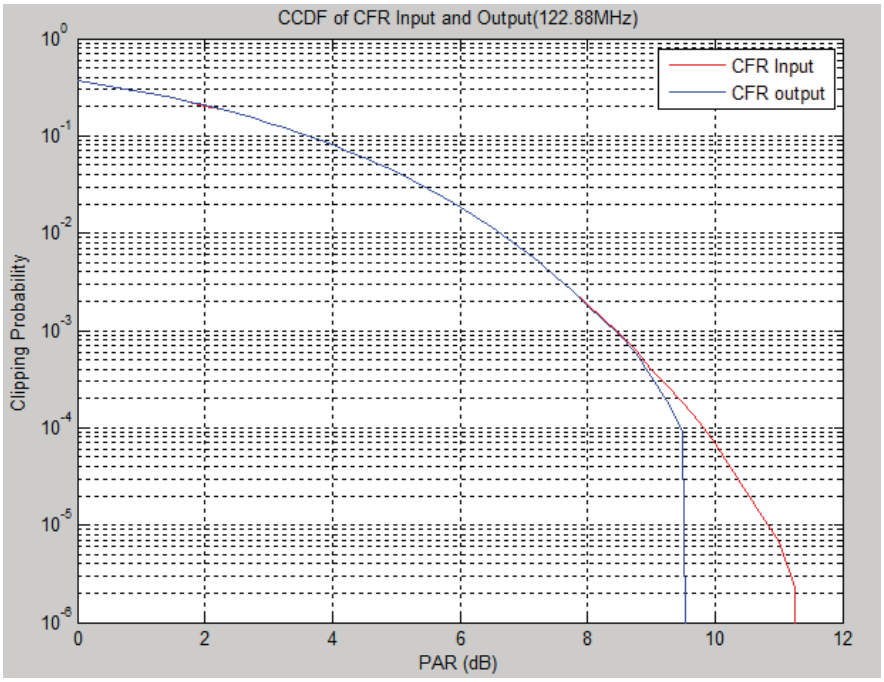
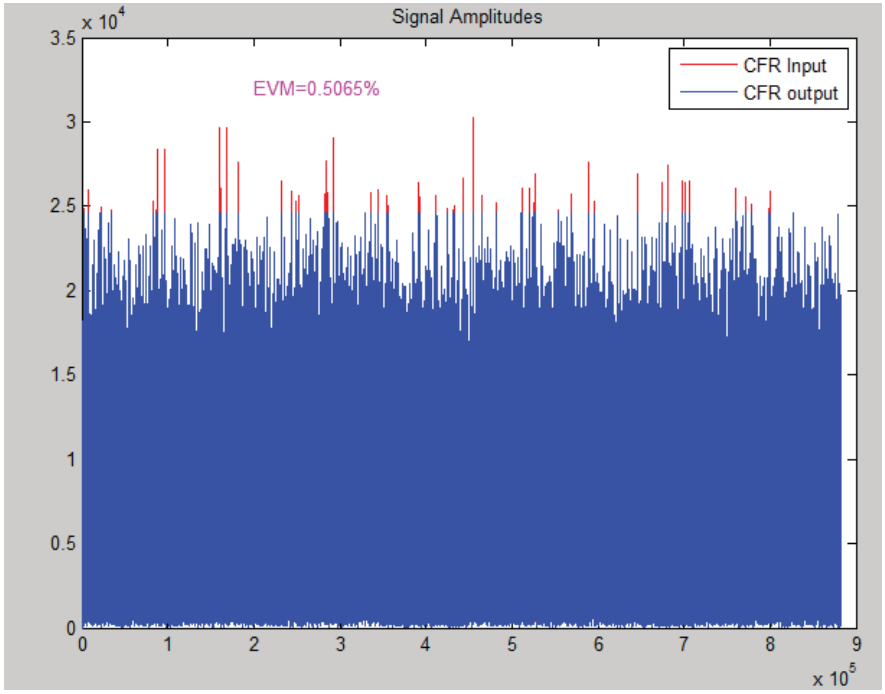


Figure 22. Signal Amplitudes of CFR Input and Output for dfe_demo_iclk_1.5db.bit



DFE Data Path Resource Estimation

Table 4 shows the resource estimation of DFE data path, including CPRI TX/RX, CPRI map/de-map, DUC and CFR, 2 antennas parallel processing.

Table 4. DFE Data Path Resource Estimation

Case	dfe_demo_iclk.bit		dfe_demo_iclk_3db.bit		dfe_demo_iclk_1.5db.bit	
Resource	**Number**	**Percent of the device**	**Number**	**Percent of the device**	**Number**	**Percent of the device**
Registers	16980	15.2%	11584	10.36%	10361	9.27%
LUTs	14638	9.9%	11562	7.76%	11174	7.5%
EBRs	94	25%	86	24%	84	23%
MULT18X18C	124 (DUC60 + CFR64)	38%	88 (DUC60 + CFR28)	27%	80 (DUC60 + CFR20)	25%
PCS (SerDes)	1	25%	1	25%	1	25%

References

The following documents provide more information:

- TN1176, LatticeECP3 SERDES/PCS Usage Guide
- EB48, LatticeECP3 I/O Protocol Board - Revision C User's Guide.
- IPUG56, CPRI IP Core User's Guide

Technical Support Assistance

e-mail: techsupport@latticesemi.com
Internet: www.latticesemi.com

Revision History

Date	Version	Change Summary
September 2013	01.0	Initial release.