MxN Channel PWM

February 2015 Reference Design RD1175

Introduction

Pulse Width Modulation (PWM) of a signal involves the modulation of its duty cycle, to convey either information over a communication channel or control the amount of power sent to a load. PWM is employed in a variety of applications, ranging from measurements and communications to power control and conversion, mainly because of its low power, noise-free and low cost characteristics. In order to supply multiple PWM signals driving a number of power control applications, a cost-effective approach is required where one can have individual control over the duty cycle of each of the output PWM signals. This is a generic MxN PWM Controller, where the numbers of PWM outputs are configurable using generic parameters. This document provides a brief description of Generic MxN Channel PWM Controller and its implementation.

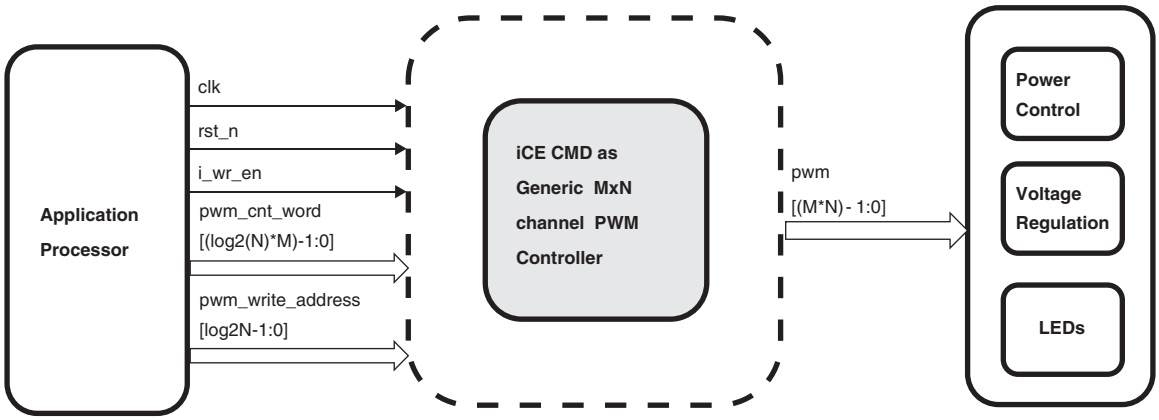
The design is implemented in VHDL. The Lattice iCEcube2™ Place and Route tool integrated with the Synopsys Synplify Pro® synthesis tool is used for the implementation of the design. The design can be targeted to other iCE40™ FPGA product family devices.

Features

- User configurable PWM Resolution
- Configurable PWM output channels

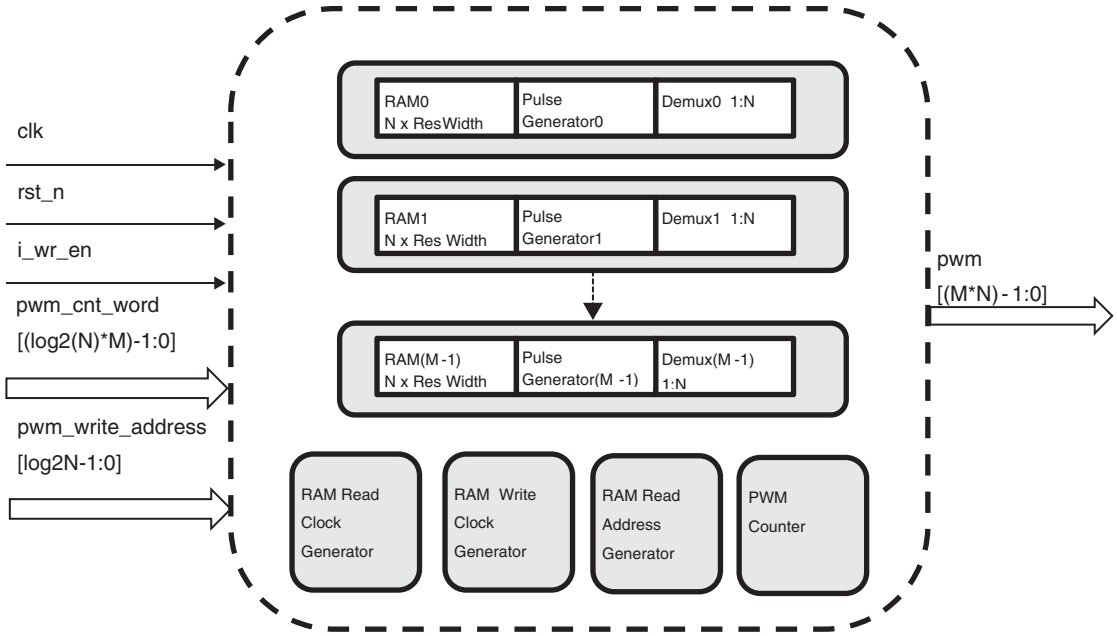
System Block Diagram

Figure 1. System Block Diagram



Functional Description

Figure 2. Functional Block Diagram



The following are brief descriptions of the internal blocks.

RAM

'M' RAMs, each of size 'N' x PWM Resolution is used to store all the control words. The size of the RAM is dependent on the value of 'N' (number of output channels) and the PWM resolution required. All the 'N' control words are read in a single write clock cycle. Hence the write clock to the RAM is divided by a factor of 'N'.

Pulse Generator

This is required to compare the two input words (Control word from the RAM and the 'count' value from the Counter), and generate the PWM signal. If the Control word is greater than or equal to the 'count' value, the output is '0', otherwise it is '1'.

1 : N De-multiplexer

This is used to route the appropriate PWM signal to one of the 'N' output channels, using the read address of the RAM as the select line to the De-multiplexer.

Counter

This is a free running counter. The generated count value is compared with the control word from the RAM in order to generate the PWM signal. It is also used to generate the Read Address to the RAM. In Figure 2, it is depicted as PWM Counter and Read Address Generator

RAM Write Clock Generator

This divides the System Clock by a factor of 'N', so that for every write cycle (one Control word written to the RAM), there are 'N' read cycles ('N' Control words are read out from the RAM).

The values of 'N' are such that they have to be in powers of two i.e. 8, 16, 32 etc. This is because the size of the RAM depends on 'N'. 'M' can take any positive number. Examples can include 2 x 4, 5 x 32, 4 x 16 etc.

Signal Description

Table 1. Signal Description

Signal	Width	Type	Description
clk	1	Input	System Clock
rst_n	1	Input	Asynchronous active low system reset
i_wr_en	1	Input	Active high write enable
pwm_cnt_word	12	Input	Control word
pwm_write_address	4	Input	Write address for the control word
pwm	48	Output	PWM signals

Operation Sequence

Initialization Condition

When 'rst_n' is Low, 'pwm [47 : 0]' will be Low.

Example #1

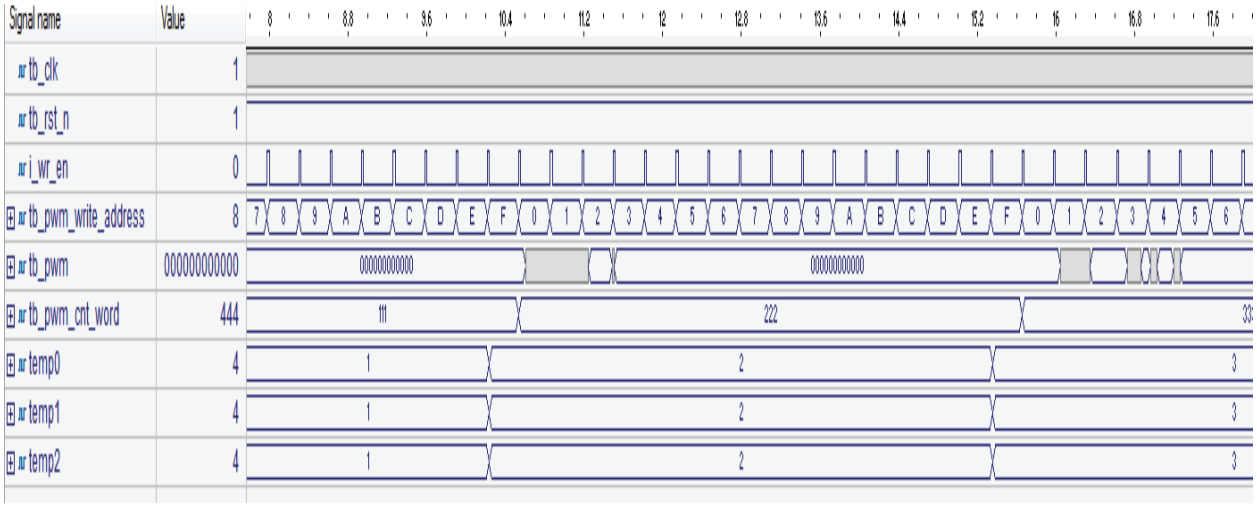
Consider a 2 x 2 voltage regulator regulating voltage between 0V and 5V. In this case, we can assume M = 2 and N = 2. Hence, the Control word will be 2 bits long.

Table 2. Voltage generated for different Control Words

Control Word	Duty Cycle(%)	Voltage Generator (V)
00	25	1.25
01	50	2.5
10	75	3.75
11	100	5

Simulation Waveforms

Figure 3. Simulation Waveforms



Implementation

This design is implemented in VHDL. When using this design in a different device, density, speed or grade, performance and utilization may vary.

Table 3. Performance and Resource Utilization

Device Family	Language	Synthesis Tool	Utilization (LUTs)	fMAX (MHz)	I/Os	Architecture Resources
iCE40[1]	VHDL	LSE	110	>50	71	(57/160) PLBs
		Syn Pro	110	>50	71	(62/160) PLBs

1. Performance and utilization characteristics are generated using iCE40LP1K-CM121 with iCEcube2 2014.12 design software and LSE support.

References

- DS1040, iCE40 LP/HX Family Data Sheet

Technical Support Assistance

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Revision History

Date	Version	Change Summary
February 2015	1.1	Updated Implementation section. Updated Table 3, Performance and Resource Utilization. — Added LSE support.
		Updated References section.
		Updated Technical Support Assistance information.
April 2013	01.0	Initial release.