UART 16450 Transceiver

April 2013 **Reference Design RD1169**

Introduction

UART is an acronym for Universal Asynchronous Receiver/Transmitter. The UART performs serial-to-parallel conversion on data characters received from a peripheral device or a MODEM, and parallel-to-serial conversion on data characters received from the CPU. The CPU can read the complete status of the UART at any time during the functional operation. Status information reported includes the type and condition of the transfer operations being performed by the UART, as well as any error conditions (parity, framing, or break interrupt).

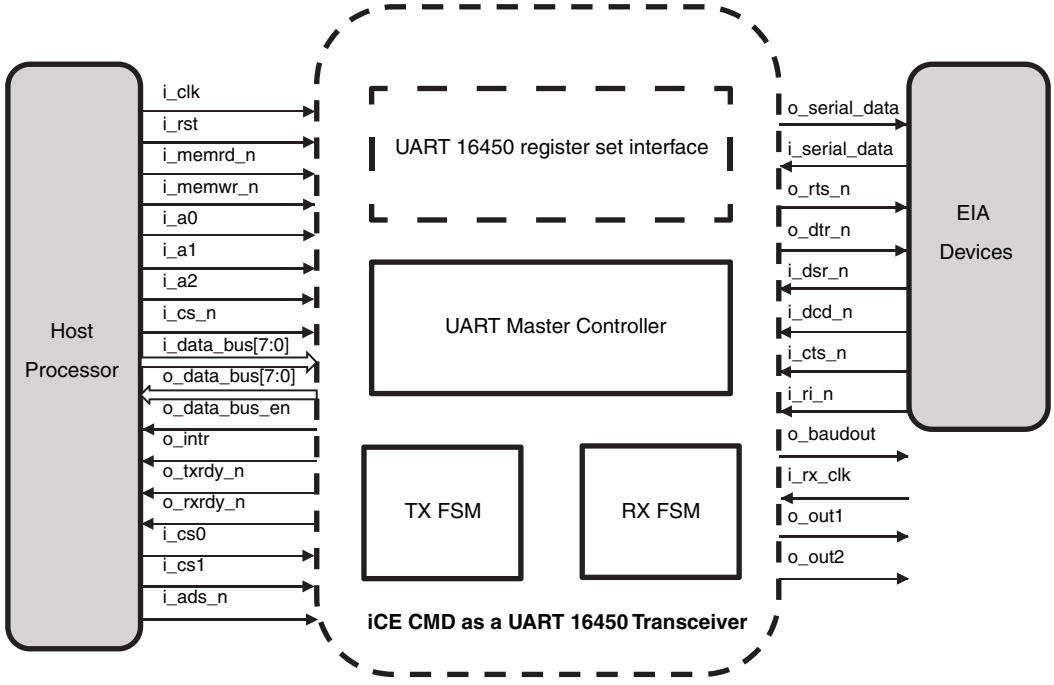
The UART has complete MODEM-control capability, and a processor-interrupt system. Interrupts can be programmed to the user's requirements, minimizing the computing required to handle the communications link. This iCE40™ design's register set and data transfer protocol is compatible with National Semiconductor 16450 UART.

Features

- Compatible with National Semiconductor 16450 UART
- Configurable data width at 5, 6, 7 or 8 bit
- Configurable stop bits - 1, 1.5 or 2 bit for transmit operations
- Even parity, odd parity or stick parity configuration for transmit and receive operations
- Programmable Divisor latch for custom baud rates
- Interrupt generation logic with readable interrupt identification register
- Verilog RTL, testbench and do file for simulation

System Block Diagram

Figure 1. System Block Diagram



Signal Description

Table 1. Signal Description

Name	Type	Description
i_clk	Input	System Clock
i_rst	Input	Asynchronous Active High System Reset
i_memrd_n	Input	Active low signal to read data or status from the selected UART16450 register
i_memwr_n	Input	Active low signal to write data or control word to the selected UART 16450 register
i_a0	Input	LSB of 3 bit register select
i_a1	Input	Bit 1 of 3 bit register select
i_a2	Input	MSB of 3 bit register select
i_cs_n	Input	Active low chip select line
i_cs0	Input	Active high chip select. This pin is tied to Vcc
i_cs1	Input	Active high chip select. This pin is tied to Vcc
i_ads_n	Input	Active low address strobe line. This pin is tied to GND.
i_data_bus[7:0]	Input	7 bit input data bus
o_data_bus[7:0]	Output	7 bit output data bus
o_data_bus_en	Output	Data bus enable signal connecting i_data_bus and o_data_bus to a tri stated io_data_bus
o_txrdy_n	Output	Active low when the Transmit holding register is empty
o_rxrdy_n	Output	Active low when data is available within the Receive buffer register
o_intr	Output	Active high interrupt signal generated whenever corresponding interrupt types are active high in the Interrupt Enable register. This is reset low on Master reset or on a Interrupt service
o_baudout	Output	16xbaud rate clock from transmitter side of the design
i_serial_data	Input	Serial data input from communication link
o_serial_data	Output	Serial data output to the communication link
o_dtr_n	Output	Active low data terminal ready signal. When low, this informs the MODEM that the UART is ready to establish a communication link. This can be made active low by programming bit 1 of the MODEM control register. On reset this bit is set to ‘1’.
o_rts_n	Output	Active low request to send signal. When low this informs the MODEM that UART is ready to exchange data. This can be made active low by programming bit 1 of the MODEM control register. On reset this bit is set to ‘1’.
i_ri_n	Input	Active low ring indicator signal. When active low indicates that the MODEM has received a telephone ringing signal.
i_dsr_n	Input	Active low data set ready signal. When low this indicates that the MODEM is ready to establish a communication link with the UART.
i_dcd_n	Input	Active low data carrier detect. When low, indicates that the MODEM has detected the data carrier.
i_cts_n	Input	Active low clear to send signal. When low, indicates that the MODEM is ready to exchange data.
i_rx_clk	Input	Receiver clock is 16xBaud rate clock for the receiver section.

Register Map

Table 2. UART 16450 Register Mapping

DLAB	i_a2	i_a1	i_a0	Register
0	0	0	0	Receive Buffer Register(read) Transmitter holding register(write)
0	0	0	1	Interrupt enable register
X	0	1	0	Interrupt Identification Register (read)
X	0	1	1	Line control register
X	1	0	0	MODEM control register
X	1	0	1	Line status register
X	1	1	0	MODEM status register
1	0	0	0	Divisor Latch (LSB)
1	0	0	1	Divisor Latch (MSB)

The 3-bit register select bits are used to select a UART register for the CPU to read from or write to during data transfer. Note that the state of the Divisor Latch Access Bit (DLAB), which is the most significant bit of the Line control register, affects the selection of certain UART 16450 registers. The DLAB must be set high by the system software to access the Baud Generator Divisor Latches.

Receive Buffer Register(RBR) / Transmitter Holding Register(THR)

In UART 16450 mode, the data received will be stored in this register. A read operation will give the received data. Data to be transmitted will be written to this register.

Interrupt Enable Register (IER)

This register enables the four types of UART interrupts. Each interrupt can individually activate the interrupt (o_intr) output signal.

- Bit 0: This bit enables the Received Data Available Interrupt when set to logic 1.
- Bit 1: This bit enables the Transmitter Holding Register Empty Interrupt when set to logic 1.
- Bit 2: This bit enables the Receiver Line Status Interrupt when set to logic 1.
- Bit 3: This bit enables the MODEM Status Interrupt when set to logic 1.
- Bits [7:4]: These four bits are always logic 0.

Interrupt Identification Register (IIR)

The Interrupt conditions and priority are summarized in Table 3

Table 3. Interrupt Identification Register

Interrupt Identification Register			Interrupt set reset functions			
Bit2	**Bit1**	**Bit0**	**Priority level**	**Interrupt type**	**Interrupt source**	**Interrupt reset control**
0	0	1	-	None	None	-
1	1	0	Highest	Receiver line status	Overrun Error or Parity Error or Framing Error or Break Interrupt	Reading line status register
1	0	0	Second	Received data available	Received data available or trigger level reached	Reading the Receiver buffer register
0	1	0	Third	Transmitter holding register empty	Transmitter holding register empty	Writing to Transmitter holding register
0	0	0	Fourth	MODEM status	Clear to send or Data set ready or RI or Data Carrier detect	Reading the modem status register

In order to provide minimum software overhead during data character transfers, the UART prioritizes interrupts into four levels and records these in the interrupt Identification Register. The four levels of interrupt conditions in order of priority are Receiver Line Status; Received Data Ready; Transmitter Holding Register Empty; and MODEM Status.

Line Control Register (LCR)

- Bits 0 and 1: These two bits specify the number of bits in each transmitted or received serial character.

Table 4. Character Length Programming Bits

Bit1	Bit0	Character Length
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

- Bit 2: This bit specifies the number of Stop bits transmitted and received in each serial character. If bit 2 is a logic0, one Stop bit is generated in the transmitted data. If bit 2 is a logic1 when a 5-bit word length is selected via bits 0 and 1, one and a half Stop bits are generated. If bit 2 is a logic1 when either a 6-, 7-, or 8-bit word length is selected, two Stop bits are generated. The Receiver checks the first Stop bit only, regardless of the number of Stop bits selected.
- Bit 3: This bit is the Parity Enable bit. When bit 3 is a logic 1, a Parity bit is generated (transmit data) or checked (receive data) between the last data word bit and Stop bit of the serial data. (The Parity bit is used to produce an even or odd number of 1s when the data word bits and the Parity bit are summed.)
- Bit 4: This bit is the Even Parity Select bit. When bit 3 is a logic1 and bit 4 is a logic0, an odd number of logic 1s is transmitted or checked in the data word bits and Parity bit. When bit 3 is a logic1 and bit 4 is a logic1, an even number of logic 1s is transmitted or checked.
- Bit 5: This bit is the Stick Parity bit. When bits 3, 4 and 5 are logic 1 the Parity bit is transmitted and checked as a logic0. If bits 3 and 5 are 1 and bit 4 is a logic0 then the Parity bit is transmitted and checked as a logic1. If bit 5 is a logic0 Stick Parity is disabled.
- Bit 6: This bit is the Break Control bit. It causes a break condition to be transmitted to the receiving UART. When

it is set to a logic1, the serial output (o_serial_data) is forced to the Spacing (logic 0) state. The break is disabled by setting bit 6 to a logic0. The Break Control bit acts only on o_serial_data and has no effect on the transmitter logic.

- Bit 7: This bit is the Divisor Latch Access Bit (DLAB). It must be set high (logic 1) to access the Divisor Latches of the Baud Generator during a Read or Write operation. It must be set low (logic 0) to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

MODEM Control Register (MCR):

This register controls the interface with the MODEM or data set (or a peripheral device emulating a MODEM).

- Bit 0: This bit controls the Data Terminal Ready (DTR) output. When bit 0 is set to a logic1, the DTR output is forced to a logic0. When bit 0 is reset to a logic0, the DTR output is forced to a logic 1.
- Bit 1: This bit controls the Request to Send (RTS) output. Bit 1 affects the RTS output in a manner identical to that described above for bit 0.

Line Status Register (LSR):

This register provides status information to the CPU concerning the data transfer.

- Bit 0: This bit is the receiver Data Ready (DR) indicator. Bit0 is set to a logic1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register. Bit0 is reset to a logic0 by reading the data in the Receiver buffer register.
- Bit 1: This bit is the Overrun Error (OE) indicator. Bit 1 indicates that data in the Receiver buffer register was not read by the CPU before the next character was transferred into the Receiver buffer register, thereby destroying the previous character. The OE indicator is set to a logic1 upon detection of an overrun condition and reset when-ever the CPU reads the contents of the Line status register.
- Bit 2: This bit is the Parity Error (PE) indicator. Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even-parity select bit. The PE bit is set to a logic1 upon detection of a parity error and is reset to a logic0 whenever the CPU reads the contents of the Line status register.
- Bit 3: This bit is the Framing Error (FE) indicator. Bit 3 indicates that the received character did not have a valid Stop bit. Bit3 is set to a logic1 whenever the Stop bit following the last data bit or parity bit is detected as a logic0 bit (Spacing level). The FE indicator is reset whenever the CPU reads the contents of the Line status register.
- Bit 4: This bit is the Break Interrupt (BI) indicator. Bit4 is set to a logic1 whenever the received data input is held in the Spacing (logic 0) state for longer than a full word transmission time (that is, the total time of Start bit a data bits a Parity a Stop bits). The BI indicator is reset whenever the CPU reads the contents of the Line Status Register. The next character transfer is enabled after i_serial_data goes to the marking state and receives the next valid start bit.
- Bit 5: This bit is the Transmitter Holding Register Empty (THRE) indicator. Bit 5 indicates that the UART is ready to accept a new character for transmission. In addition, this bit causes the UART to issue an interrupt to the CPU when the Transmit Holding Register Empty Interrupt enable is set high. The THRE bit is set to a logic1 when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to logic 0 concurrently with the loading of the Transmitter Holding Register by the CPU.
- Bit 6: This bit is the Transmitter Empty (TEMT) indicator. Bit6 is set to a logic1 whenever the Transmitter Holding Register (THR) and the Transmitter Shift Register (TSR) are both empty. It is reset to a logic0 whenever either the THR or TSR contains a data character.
- Bit 7: This bit is a 0.

MODEM Status Register (MSR):

This register provides the current state of the control lines from the MODEM (or peripheral device) to the CPU. In addition to this current-state information, four bits of the MODEM Status Register provide change information. These bits are set to a logic1 whenever a control input from the MODEM changes state. They are reset to logic 0 whenever the CPU reads the MODEM Status Register.

- Bit 0: This bit is the Delta Clear to Send (DCTS) indicator. Bit 0 indicates that the CTS input to the chip has changed state since the last time it was read by the CPU.
- Bit 1: This bit is the Delta Data Set Ready (DDSR) indicator. Bit 1 indicates that the DSR input to the chip has changed state since the last time it was read by the CPU.
- Bit 2: This bit is the Trailing Edge of Ring Indicator (TERI) detector. Bit 2 indicates that the RI input to the chip has changed from a low to a high state.
- Bit 3: This bit is the Delta Data Carrier Detect (DDCD) indicator. Bit 3 indicates that the DCD input to the chip has changed state.
- Bit 4: This bit is the complement of the Clear to Send (CTS) input.
- Bit 5: This bit is the complement of the Data Set Ready (DSR) input.
- Bit 6: This bit is the complement of the Ring Indicator (RI) input.
- Bit 7: This bit is the complement of the Data Carrier Detect (DCD) input.

Divisor Latch Register (DLR)

The UART contains a programmable baud generator that is capable of taking any clock input (< 24MHz). Two 8-bit latches store the divisor in a 16-bit binary format. These Divisor Latch Registers must be loaded during initialization to ensure proper operation of the baud generator. Upon loading either of the Divisor Latch Registers, a 16-bit Baud counter is immediately loaded. The divisor is calculated as follows: Divisor = (frequency input)/ (baud rate x 16). Table5 is an example showing the values of the Divisor Latch Register for the supported baud rates at system clock of 18.432MHz.

Table 5. Supported Baud Rates with Equivalent Divisor Latch Inputs

Baud Rate	Divisor_Latch (MSB,LSB)
50	23040
75	15360
110	10473
134.5	8565
150	7680
300	3840
600	1920
1200	920
1800	640
2000	576
2400	480
3600	320
4800	240
7200	160
9600	120
19200	60
38400	30
56000	21
128000	9

Design Details

The UART 16450 transceiver consists of a register set interface block, UART Master Controller block, UART Tx FSM block and UART Rx FSM block. The main function of the register set interface block is to receive and transmit information to the host processor using the asynchronous processor interface. The register set interface block delivers control information to the UART Master Controller. It also gathers status information and up-dates the register set. This block is responsible for generation of the interrupt.

The UART Master Controller block forms the heart of the design. This block decodes the control data and configures the UART Rx FSM block and the UART Tx FSM block as per configuration data. The steps involved in transmit and receive operations is briefly outlined below:

UART Transmit Operation

To start a transmit operation, the user sets bit 1 of Modem Control Register (MCR). This de-asserts the o_rts_n. In response to o_rts_n, the MODEM de-asserts the i_cts_n line. The UART 16450 IP detects this and a start condition is generated followed by the data transfer and termination of operation as per the UART protocol. The format of the transmit data by the user is shown in Table 6.

Table 6. Tx Data Format

5-Bit Data	0	0	0	D4	D3	D2	D1	D0
6-Bit Data	0	0	D5	D4	D3	D2	D1	D0
7-Bit Data	0	D7	D5	D4	D3	D2	D1	D0
8-Bit Data	D8	D7	D5	D4	D3	D2	D1	D0

UART Receive Operation

On receiving the i_dsr_n signal, the user sets bit 0 of the MODEM Control Register. This de-asserts the o_dtr_n signal. The UART 16450 IP then waits for the start condition on the i_serial_data line. Once the operation is terminated, the receive data is validated and the valid data is made available in the Receive Buffer Register. The format of the received data stored in the Receive Buffer Register is shown in Table 7.

Table 7. Rx Data Format

5-Bit Data	0	0	0	D4	D3	D2	D1	D0
6-Bit Data	0	0	D5	D4	D3	D2	D1	D0
7-Bit Data	0	D7	D5	D4	D3	D2	D1	D0
8-Bit Data	D8	D7	D5	D4	D3	D2	D1	D0

Timing Diagram

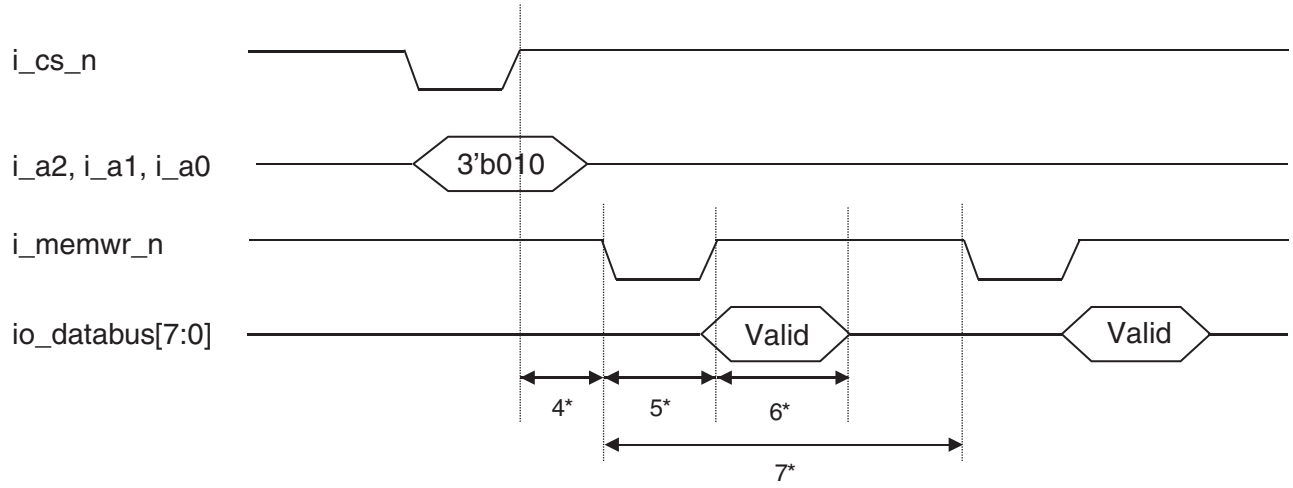
Timing Diagram of Write Cycle

Figure 2 shows the timing diagram of the write cycle to an internal register (For example: Line Control Register with address 3'b011) of the UART 16450 transceiver IP.

The timing to be maintained is listed below:

- 1* - Between Rising edge of i_cs_n and following falling edge of i_memwr_n should be at least 1 system clock period
- 2* - Between falling edge of i_memwr_n and it rising edge should be at least 1 system clock period
- 3* - Between falling edge of i_memwr_n and the next falling edge should be at least 4 system clock periods.

Figure 2. Timing Diagram of Write Cycle



Timing Diagram of Read Cycle

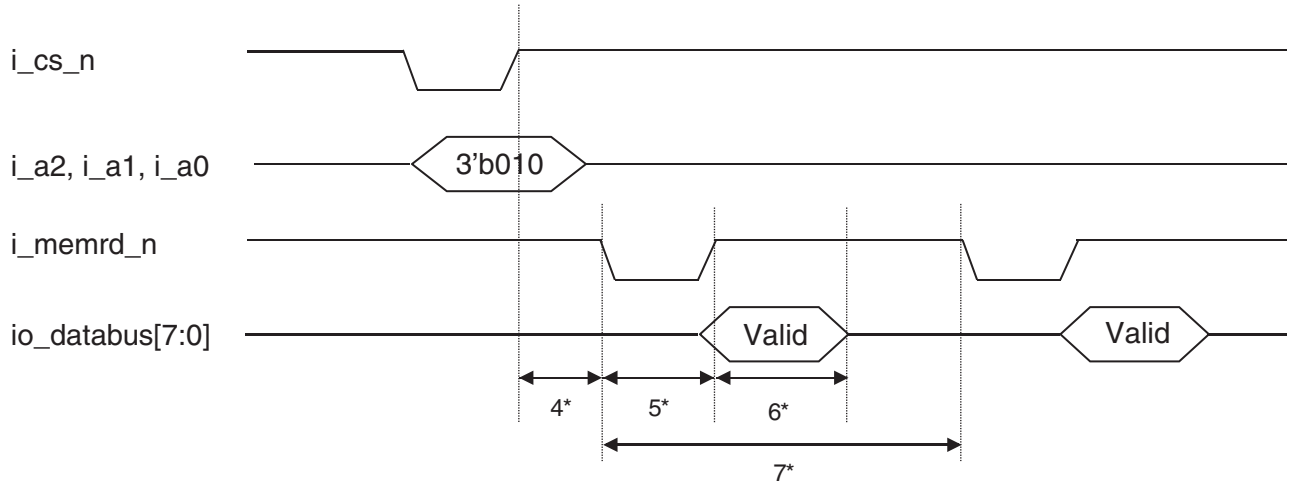
Figure 3 shows the timing diagram of the read cycle to an internal register (For example: Line Status Register with address 3'b101) of the UART 16450 transceiver IP.

The timing to be maintained is listed below:

- 4* - Between Rising edge of i_cs_n and following falling edge of i_memrd_n should be atleast 1 system clock period
- 5* - Between falling edge of i_memrd_n and it rising edge should be at-least 3 system clock periods

- 6* - Valid data availability after i_memrd_n is pulled high is a minimum of 1 clock period and a max of 1.5 clock periods
- 7* - Between falling edge of i_memrd_n and the next falling edge should be at least 4 system clock periods.

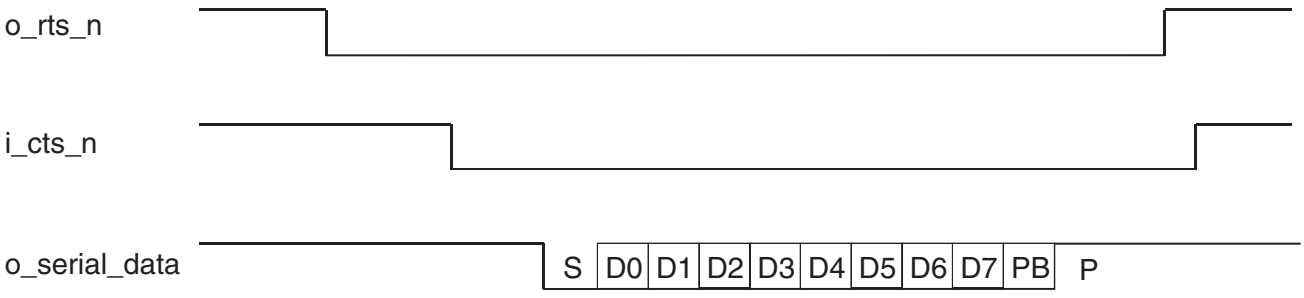
Figure 3. Timing Diagram of Read Cycle



Timing Diagram of MODEM-Side Receive Operation

Figure 6 shows the receive operation from the MODEM side. In response to the o_rts_n de-asserted by the UART, the MODEM de-asserts the i_cts_n line. The master then sends the data on the o_serial_data line as per the UART Data format as shown in Figure8.

Figure 4. Timing Diagram of MODEM-Side Receive Operation



Timing Diagram of MODEM-Side Transmit Operation

Figure7 shows the transmit operation from the MODEM side. The slave de-asserts the i_dsr_n line signaling to the UART that it has data to send. The UART then de-asserts the o_dtr_n line when it is ready to receive data. The MODEM then initiates the transaction on the i_serial_data.

Figure 5. Timing Diagram of MODEM-Side Transmit Operation

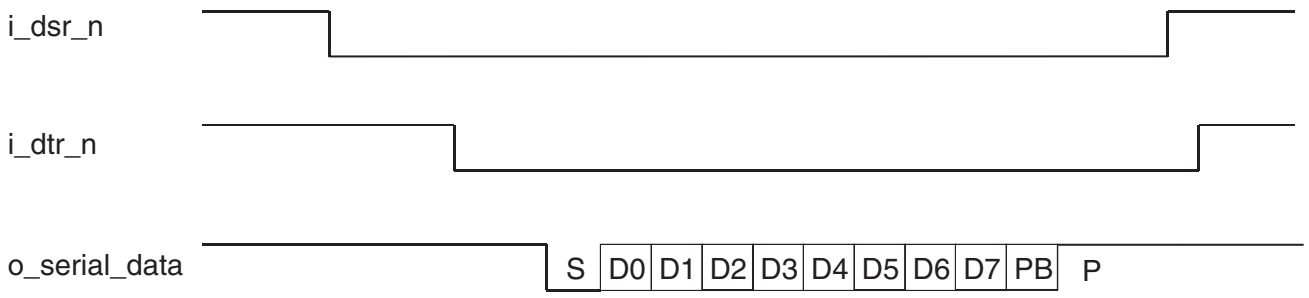
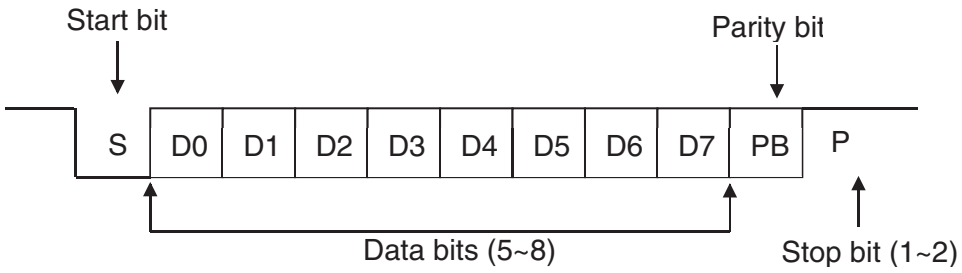
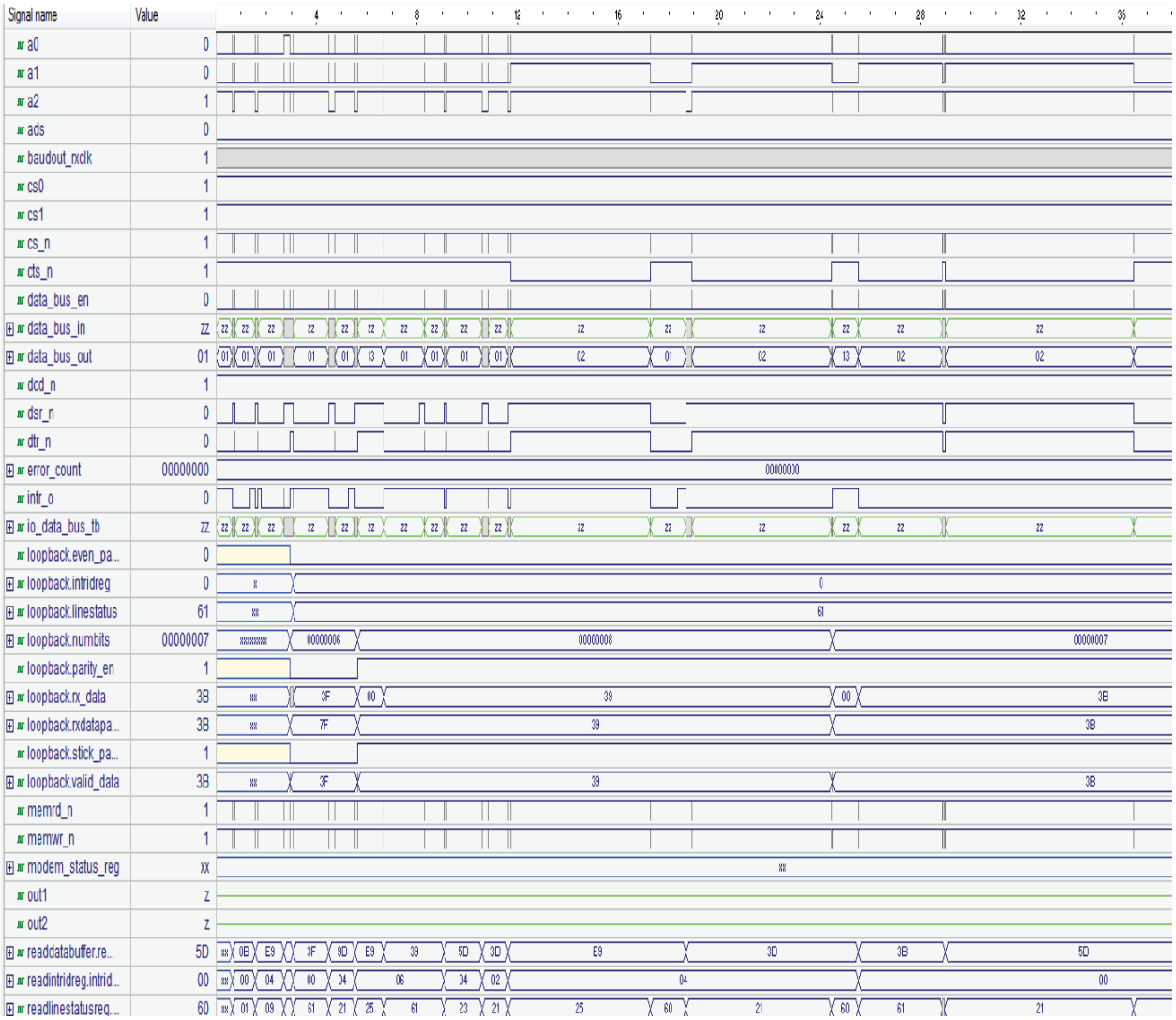


Figure 6. UART Data Format



Simulation Waveforms

Figure 7. Simulation Waveforms



Operation Sequence

This design is implemented in VHDL. When using this design in a different device, density, speed or grade, performance and utilization may vary.

UART 16450 are used for implementing the interface for serial communications. It is frequently used in implementation of serial ports which is then used for connections with MODEMS, serial mice, printers and similar peripherals using RS-232 interface.

Figure 1 shows one of the possible scenarios in which the UART 16450 can be used.

The procedure for transmit and receive operations is outlined as below:

Transmit Operation

Let us consider an example of a transmit operation at baud rate of 9600. The data format is: Data width of 5 bits with even parity enabled and 1.5 stop bits. Interrupt is disabled. The system clock is 18.432MHz. All write and read to/from the internal register set are as per Figure 2 and Figure 3.

The following steps are to be followed for carrying out this transaction.

1. De-assert the system reset i_rst signal.
2. 2. Set baud rate of operation to 9600. This is a three step procedure :

   Step 1: A write to Line Control Register.

   DLAB bit i.e bit 7 of Line Control Register is first set to logic 1. Register select inputs i_a2, i_a1 and i_a0 are set to logic 0, logic 1 and logic 1 respectively. The data on the io_data_bus is 8'b1000_0000.

   Step 2: A write to Divisor Latch (LSB) and Divisor Latch (MSB).

   To write to DLR (LSB), the register select inputs i_a2, i_a1 and i_a0 are set to logic 0, logic 0 and logic 0. 8'd120 is written to the Divisor Latch Register (LSB). To write to DLR (MSB), the register select inputs i_a2, i_a1 and i_a0 are set to logic 0, logic 0 and logic 1. 8'd0 is written to the Di-visor Latch Register (MSB).

   Step 3: A write to Line Control Register

   DLAB bit i.e bit 7 of Line Control Register is reset to logic 0. The register select inputs i_a2, i_a1 and i_a0 are set to logic 0, logic 1 and logic 1 respectively. The data on the io_data_bus is 8'b0000_0000.
3. A write to Line Control register to configure for the required data format i.e. Data width of 5 bits with even parity enabled and 1.5 stop bits.
   - Address select bits i_a2, i_a1 and i_a0 are set to logic 0, logic 1, logic 1
   - For 5 bit operation, bit0 and bit1 of LCR is set to logic 0 and logic 0
   - For even parity enable, bit3 and bit4 of LCR is set to logic 1
   - For enabling 1.5 stop bits, bit 2 of LCR is set to logic 1
   - Thus data written to LCR is 8'b000_11_1_00
4. A write to Interrupt Enable Register to configure for interrupt disable
   - Address select bits i_a2, i_a1 and i_a0 are set to logic 0, logic 0 and logic 1
   - Data written to IER is 8'b0000_0000

5. A write to Transmitter Holding Register (THR).
   - Address select bits i_a2, i_a1 and i_a0 are set to logic 0, logic 0 and logic 0
   - Data written to THR is transmit data
6. A write to MODEM Control Register. To start the transmission procedure, set the Request to Send (RTS) bit, i.e. MCR bit 1.
   - Address select bits i_a2, i_a1 and i_a0 are set to logic 1, logic 0 and logic 0
   - Data written to MCR is 8'b0000_0010
7. When the Clear To Send (CTS) is pulled low by the MODEM the transmit process begins and terminates with the transmission of stop bits.
8. Line Status Register read. If bit 5 is set to one then the Transmitter Holding Register is empty.
   - Address select bits i_a2, i_a1 and i_a0 are set to logic 1, logic 0 and logic 1
   - If bit 5 is set to one then, data has been transmitted and the Transmitter Holding Register is now empty.
9. A write to MODEM Control Register. Reset the Request to Send (RTS) bit, i.e. MCR bit 1.
   - Address select bits i_a2, i_a1 and i_a0 are set to logic 1, logic 0 and logic 0
   - Data written to MCR is 8'b0000_0000

Receive Operation:

Let us consider an example of a receive operation at baud rate of 7200. The data format is : Data width of 8 bits with even stick parity enabled and 1 stop bits. Interrupt is disabled. The system clock is 18.432MHz. All write and read to/from the internal register set are as per Figure4 and Figure5.

1. De-assert the system reset i_rst signal.
2. Set baud rate of operation to 7200. This is a three step procedure :

   Step 1 : A write to Line Control Register

   DLAB bit i.e bit 7 of Line Control Register is first set to logic 1. Register select inputs i_a2, i_a1 and i_a0 are set to logic 0, logic 1 and logic 1 respectively. The data on the io_data_bus is 8'b1000_0000.

   Step 2 : A write to Divisor Latch(LSB) and Divisor Latch(MSB)

   To write to DLR (LSB), the register select inputs i_a2, i_a1 and i_a0 are set to logic 0, logic 0 and logic 0. 8'd160 is written to the Divisor Latch Register (LSB).

   To write to DLR (MSB), the register select inputs i_a2, i_a1 and i_a0 are set to logic 0, logic 0 and logic 1. 8'd0 is written to the Divisor Latch Register (MSB).

   Step 3 : A write to Line Control Register

   DLAB bit i.e bit 7 of Line Control Register is reset to logic 0. The register select inputs i_a2, i_a1 and i_a0 are set to logic 0, logic 1 and logic 1 respectively. The data on the io_data_bus is 8'b0000_0000.
3. A write to Line Control register to configure for the required data format i.e. Data width of 8 bits with even stick parity enabled and 1 stop bits.
   - Address select bits i_a2, i_a1 and i_a0 are set to logic 0, logic 1, logic 1

- For 8 bit operation, bit 0 and bit 1 of LCR is set to logic 1 and logic 1
- For even stick parity enable, bit 3, bit 4 and bit 5 of LCR are set to logic 1
- For enabling 1 stop bits, bit 2 of LCR is set to logic 0
- Thus data written to LCR is 8'b00111_0_11

4. A write to Interrupt Enable Register to configure for interrupt disable.
   - Address select bits i_a2, i_a1 and i_a0 are set to logic 0, logic 0 and logic 1
   - Data written to IER is 8'b0000_0000
5. MODEM Status Register read.
   - Address select bits i_a2, i_a1 and i_a0 are set to logic 1, logic 1 and logic 0
   - If bit 5 is set to '1' then the MODEM is ready to send data
6. A write to MODEM Control Register. Logic '1' written to MCR bit 0. This is Data Terminal Ready which is a response to MODEM's Data Set Ready.
   - Address select bits i_a2, i_a1 and i_a0 are set to logic 1, logic 0 and logic 0
   - Data written to MCR is 8'b0000_0001
7. Serial data receive operation takes place on the MODEM side. This is invisible on the processor side.
8. MODEM Status Register read.
   - Address select bits i_a2, i_a1 and i_a0 are set to logic 1, logic 1 and logic 0
   - If bit 5 is set to '1' then the MODEM isn't ready to send data
9. A write to MODEM Control Register. Logic '0' written to MCR bit 0. This is Data Terminal Ready which is a response to MODEM's Data Set Ready. This is pulled high as MODEM isn't ready to send new data yet.
   - Address select bits i_a2, i_a1 and i_a0 are set to logic 1, logic 0 and logic 0
   - Data written to MCR is 8'b0000_0000
10. Receive Buffer Register (RBR) read. o_rxrdy_n is active low when there is data available in the FIFO to read.
    - Address select bits i_a2, i_a1 and i_a0 are set to logic 0, logic 0 and logic 0.
    - Data is read until o_rxrdy_n goes high.

Implementation

This design is implemented in VHDL. When using this design in a different device, density, speed or grade, performance and utilization may vary.

Table 8. Performance and Resource Utilization

Family	Language	Utilization (LUTs)	f_{MAX} (MHz)	I/Os	Architectural Resources
iCE40[1]	Verilog	513	>50	43	(104/160)PLBs

1. Performance and utilization characteristics are generated using iCE40LP1K-CM121 with iCEcube2 design software.

References

- iCE40 Family Handbook

Technical Support Assistance

Hotline: 1-800-LATTICE (North America)
+1-503-268-8001 (Outside North America)
e-mail: techsupport@latticesemi.com
Internet: www.latticesemi.com

Revision History

Date	Version	Change Summary
April 2013	01.0	Initial release.