

## Introduction

The Secure Digital (SD) Card is a Flash-based memory card that is widely used in today's consumer electronic devices. Its high-capacity, compact package and security make it a suitable candidate for both audio and video applications in electronic products. Some common consumer products that make use of SD cards include digital cameras, personal computers, printers, mobile phones and car navigations systems. The SD technology is considered a de-facto standard in the industry for data storage. There is high demand for SD cards in both portable and desktop consumer products.

The interface of the SD Host Controller is through a generic processor interface allowing the designer to easily interface the design with SoC systems.

The design is implemented in VHDL. The Lattice iCEcube2™ Place and Route tool integrated with the Synopsys Synplify Pro® synthesis tool is used for the implementation of the design. The design can be targeted to other iCE40™ FPGA product family devices.

Figure 1 shows the System Block Diagram for the SD Host Controller interface.

## Features

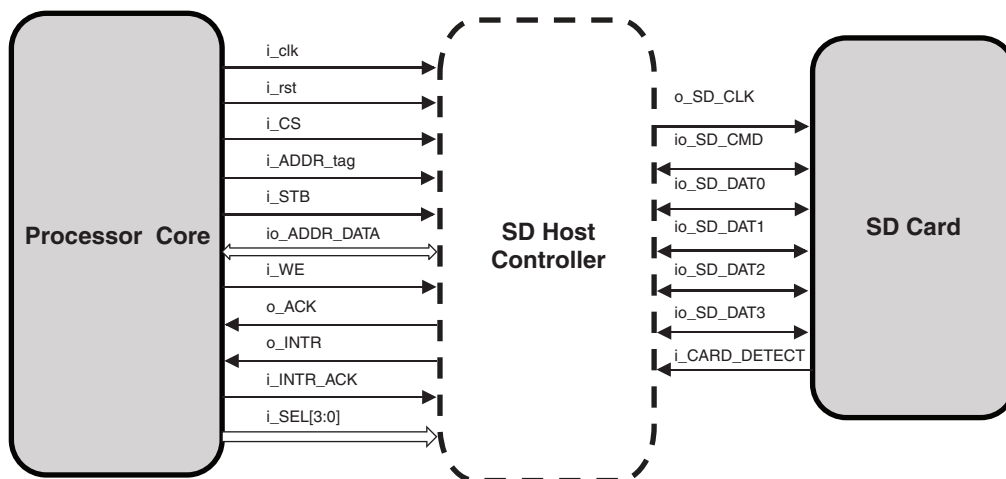
- Meets SD standard specifications 2.0
- Auto Card detect and SD card detection
- Forced initialization from processor
- Operates under SD 1-bit, SD 4-bit and SPI mode for SD cards
- Operates at the normal mode of 25Mhz and also at an optional high speed mode of 50MHz
- Features a 32 bit processor bus interface so that the processor isn't tied to the controller for the low speed transfers on the SD physical layer
- Features an 8K Read/Write buffer for processor initiated writes and reads
- Supports single block read and write operations
- Supports multi block read and write operations

## System Block Diagram

The SD Host Controller is used to setup communication between a processor and a SD card. It supports the translation protocol from a serial peripheral interface (SPI) bus to SD task.

Figure 1 shows the System Interface of this reference design.

Figure 1. System Block Diagram



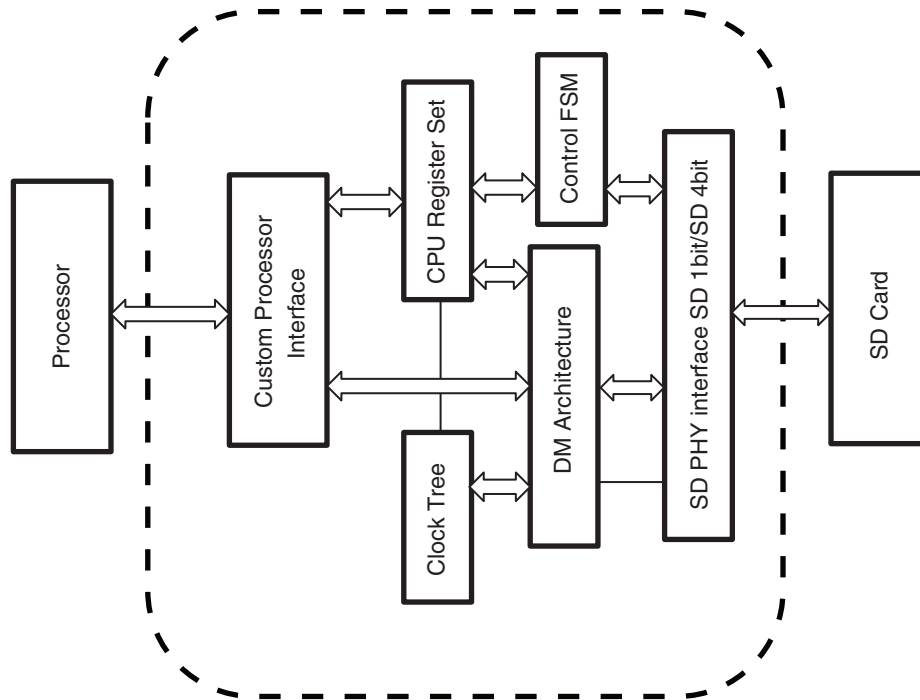
## Signal Description

Table 1. Signal Description

| Signal        | Width | Type   | Description                                                                                                                    |
|---------------|-------|--------|--------------------------------------------------------------------------------------------------------------------------------|
| i_clk         | 1     | Input  | System Clock                                                                                                                   |
| i_rst         | 1     | Input  | Asynchronous Active high clock reset                                                                                           |
| i_cs          | 1     | Input  | Active low chip select signal from the processor interface which shall be asserted for all transactions on processor interface |
| i_ADDR_tag    | 1     | Input  | Active high address latch enable signal indicating that the value of io_ADDR_DATA bus is an address for the transaction        |
| i_STB         | 1     | Input  | Active low strobe input which indicates that a valid transaction is on the processor bus interface                             |
| io_ADDR_DATA  | 32    | Inout  | Multiplexed 32 bit address/data bus which can be used to transfer data for processor initiated transactions                    |
| i_WE          | 1     | Input  | Active high write enable signal                                                                                                |
| o_ACK         | 1     | Output | Active high acknowledge indicating that the host controller has accepted the invitation                                        |
| o_INTR        | 1     | Output | Active high interrupt signal that may be asserted for conveying error/information to the processor                             |
| i_INTR_ACK    | 1     | Input  | Active high interrupt acknowledge to de-assert the interrupt that was raised by the host controller                            |
| i_SEL[3:0]    | 4     | Input  | Byte enables select for indicating the bytes that are enabled in the io_ADDR_DATA bus                                          |
| o_SD_CLK      | 1     | Output | SD card clock input. The line is at 400kHz during initialization and afterwards at data transfer frequency(<25 or <50 MHz)     |
| io_SD_CMD     | 1     | Inout  | The command/response bus of the SD bus interface                                                                               |
| io_SD_DAT0    | 1     | Inout  | The data line 0 of the SD bus interface                                                                                        |
| io_SD_DAT1    | 1     | Inout  | The data line 1 of the SD bus interface                                                                                        |
| io_SD_DAT2    | 1     | Inout  | The data line 2 of the SD bus interface                                                                                        |
| io_SD_DAT3    | 1     | Inout  | The data line 3 of the SD bus interface                                                                                        |
| i_CARD_DETECT | 1     | Input  | The card detect pin of the SD bus interface                                                                                    |

## Design Module Description

Figure 2. Functional Block Diagram



### Custom Processor Interface

The custom processor interface used here is a general purpose 32-bit multiplexed address and data bus interface. The processor shall issue the address and data for read and write operation on the same multiplexed bus. The processor is informed about the Host Controller status using “read only” status registers in the CPU registers map. The processor can configure the Host Controller by writing different configuration registers.

### CPU Register Set

The CPU register set consists of the SD Host Controller register set which can be used by the Host Driver running on the Processor.

### DMA Architecture

The DMA Architecture is used for buffering the data to be read/written from/to SD Card through the Host Controller. The processor may hence operate at a higher rate compared to data transfer between the Host Controller and the SD Card.

### Control FSM

Control FSM is used for initialization and command posting mechanism.

### SD PHY Interface

The SD PHY Interface is used for SD memory side physical interface that handles the SD data transfer modes (SD 1 bit Mode, SD 4-bit Mode, SPI Mode).

## Register Map

The SD Host Controller Configuration can be performed on run-time as well as during compile time depending on the designs requirements and also resource consumption. Table below lists the SD HCI registers and their address mapping.

| Register name                              | Address | Width | Mode | Register Description                                                                                                           |
|--------------------------------------------|---------|-------|------|--------------------------------------------------------------------------------------------------------------------------------|
| Block Size Register                        | 0x04    | 16    | RW   | The register can be used to indicate the block size of transfer                                                                |
| Block Count Register                       | 0x06    | 16    | RW   | The register is used for configuring the number of blocks that are to be transferred to/from the processor from/to the SD card |
| SDIO configuration Register                | 0x07    | 8     | NA   | The register is used to configure SDIO data transactions to the SD card                                                        |
| iCE Design Specific Configuration Register | 0x64    | 8     | RW   | The register is used for configuring the SD host controller operations                                                         |
| iCE Design Specific Status Register        | 0x80    | 8     | RW   | The register is used for identifying the status of SD Host Controller Initialization modules                                   |
| Explicit Command Register                  | 0x0E    | 16    | RW   | The register is used to configure any commands that the processor wants to execute from its side                               |
| SD Argument Register (LS Word)             | 0x08    | 16    | RW   | The argument 0 of the SD command shall be programmed in the register                                                           |
| SD Argument Register (LS Word)             | 0x0A    | 16    | RW   | The argument 1 of the SD command shall be programmed in the register                                                           |
| Response Register                          | 0x10    | 128   | RO   | The response register can be read by the processor once the command is posted                                                  |

Here are the details on various bits of these registers.

SD Argument Register (LS Word), SD Argument Register (MS Word), and Response Register are 16, 16 and 128-bit registers respectively.

- Block Count Registers(8-bits)
  - Block Count: Allowed Values are 0x00–0x0F. A maximum of 16 blocks can be transmitted.
- Block Size Register (16 bits)
  - Block Size: The register is a 16 bit register and the value in this register indicates the number of bytes that accessed to/from the SD card. A 0x0000 value in the register would imply an access of 512 bytes to/from the card. A 0x0200 implies an access of 1024 bytes per access on the SD interface.
- Specific Configuration Register (16 bits)
  - Bus Width: A 00 indicates SD 1 bit mode, 01 indicates SD4 bit mode, 11 indicates SPI mode
  - Reset\_init\_stats: A 1 written to this bit shall reset all internal flags of the Host Controller and processor should initiate an initialization all over again
  - Force\_init: This bit shall be made to 1 for forcible initialization of the SD card
  - Speed Class: This bit shall be programmed to 1 for High Speed mode of operation for both SD and 0 for a normal mode of operation.
- Specific Status Register (16 bits)
  - Init\_done: This bit indicates an initialization done indication to the processor
  - Err\_in\_init: This bit indicates that the initialization was unsuccessful
  - Unusable Card: This bit shall indicate a voltage mismatch or continuous ERC error observed during initial-

ization and indicate it as an unusable card

- SD Standard Legacy Card: Indicates that the card is SD and a Legacy card
  - SD Normal Capacity Card: Indicates that the card is SD and normal capacity (upto 2Gb)
  - SD High Capacity Card : Indicates that the card is SD and High Capacity(over 2Gb)
  - High Voltage MMC Card: When 1 indicates that the card is a High voltage MMC card else it represents Dual voltage MMC card when all SD status are 0 and init done is 1
  - MMC Version 4.1x: Indicates that the MMC is of version4.1x
  - SDIO Flag: Indicates that there is an SDIO section in the card that is inserted
  - Memory Flag: Indicates that there is a memory section in the card that is inserted. This flag can be used with the SDIO Flag bit to check if the card inserted is a Combo Card.
- Explicit Command Register (16 bits)
    - SDMMC\_Command: The command that has to be posted. The SD specification shall be referred for command op-codes
    - Command\_Request: The bit shall indicate the validity of the command value in the Command Index section of the register.

The register set information for the design of the Software driver is shown in next table.

**Table 2. Register Set Information**

| Sl. No. | Register                    | Register Address | Register Size (bits) | Bit Range (Access) | Register Description                                                                                                                                                                                                                                                  |
|---------|-----------------------------|------------------|----------------------|--------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1       | Block Size Register         | 0x04             | 16                   | [7:0] RW           | Block size register MS byte (address=0x04)                                                                                                                                                                                                                            |
|         |                             |                  |                      | [15:0] RW          | Block size register LS byte (address=0x05)                                                                                                                                                                                                                            |
| 2       | Block Count Register        | 0x06             | 8                    | [7:4] RO           | Reserved for future use                                                                                                                                                                                                                                               |
|         |                             |                  |                      | [3:0] RW           | Block count which indicates the number of blocks of data (each of size indicated by the Block Size register) for a read/write transaction on the SD interface. This is only applicable in case of SD accesses. For SDIO accesses the value is treated as “don’t care” |
| 3       | SDIO Configuration Register | 0x07             | 8                    | [7:4] RO           | Reserved for future use                                                                                                                                                                                                                                               |
|         |                             |                  |                      | [3] NA             | SDIO access flag. This bit shall be set to one before the processor posts a read/write access to the SDIO register space. If this bit is not set, then the processor transaction is interpreted to be targeted to the SD/MMC space of the card                        |
|         |                             |                  |                      | [2:0] NA           | SDIO function number: The function number to which the processor wants to issue the access to. This field is used in the argument for the SDIO commands CMD53/CMD52.                                                                                                  |
| 4       | SD Argument Register        | 0x08             | 2                    | [7:0] RW           | LS byte of LS word of the argument register (address 0x08)                                                                                                                                                                                                            |
|         |                             |                  |                      | [15:8] RW          | MS byte of LS word of the argument register (address 0x09)                                                                                                                                                                                                            |
|         |                             |                  |                      | [23:16] RW         | LS byte of MS word of the argument register (address 0xA)                                                                                                                                                                                                             |
|         |                             |                  |                      | [31:24] RW         | MS byte of MS word of the argument register (address 0xB)                                                                                                                                                                                                             |
|         |                             |                  |                      | NA                 | The argument register can be used to send a processor intended command to the SD card without the interference of the controller. The processor can use the command register for sending an explicit command. The register is byte as well as word accessible         |

|   |                                 |      |    |            |                                                                                                                                                                                                                                                                                                                                                  |
|---|---------------------------------|------|----|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 5 | Specific Configuration Register | 0x64 | 16 | [15:6] RO  | Reserved for future use                                                                                                                                                                                                                                                                                                                          |
|   |                                 |      |    | [5] WO     | Auto Detect, Asserted if Auto Detect is required                                                                                                                                                                                                                                                                                                 |
|   |                                 |      |    | [4] WO     | Speed class, 0 for Standard Mode, 1 for High Speed Mode                                                                                                                                                                                                                                                                                          |
|   |                                 |      |    | [3:2] RW   | Bus width configuration on the PHY interface A 00 indicates a SD 1 bit mode, 01 indicates a SD 4 bit mode, a 11 indicates SPI mode of operation                                                                                                                                                                                                  |
|   |                                 |      |    | [1] RW     | Reset initialization Statistics: The bit is used as a soft reset for resetting any initialization flags that are set by the host controller when it was used to initialize any other card. The processor is expected to set this bit at least once before a second initialization is forced on the Host controller initialization state machines |
|   |                                 |      |    | [0] RW     | Force initialization: This bit is used to control the initialization flow of the Host controller. Only when the software driver sets this bit, the host controller starts the initialization process.                                                                                                                                            |
| 6 | Specific Status Register        | 0x80 | 16 | [15:11] RO | Reserved for future use                                                                                                                                                                                                                                                                                                                          |
|   |                                 |      |    | [10] NA    | Memory Flag: When set indicates that the card inserted has a memory section. (The bit is of importance in case of SDIO operation to make sure if the card is a combo card)                                                                                                                                                                       |
|   |                                 |      |    | [9] NA     | SDIO Flag: When set indicates that the card inserted has an SDIO section                                                                                                                                                                                                                                                                         |
|   |                                 |      |    | [8] NA     | MMC Card version above 4.1x. Indicates that the card inserted is above MMC version 4.1x                                                                                                                                                                                                                                                          |
|   |                                 |      |    | [7] RO     | Unusable card: This is an error bit and indicates that the card is unusable for various reasons such as repeated errors during etc                                                                                                                                                                                                               |
|   |                                 |      |    | [6] RO     | Card Capacity: When set indicates that the card is a high capacity card.                                                                                                                                                                                                                                                                         |
|   |                                 |      |    | [5] NA     | MMC Dual Voltage supported: When Set indicates that the card supports dual voltage.                                                                                                                                                                                                                                                              |
|   |                                 |      |    | [4] RO     | SD Legacy Card: When set indicates that the card is a legacy SD card                                                                                                                                                                                                                                                                             |
|   |                                 |      |    | [3] NA     | MMC Card: Indicates that the card inserted is an MMC Card                                                                                                                                                                                                                                                                                        |
|   |                                 |      |    | [2] RO     | CMD Sent: This bit is an acknowledge bit indicating that the explicit command is sent by the Host Controller and the received response is updated in the Response register. The processor may have to poll this bit at regular intervals after posting a request for an explicit command to enquire the status of the request.                   |

|                                                                                                              |                           |      |     |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|--------------------------------------------------------------------------------------------------------------|---------------------------|------|-----|------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7                                                                                                            | Response Register         | 0x10 | 128 | [127:0] RO | This register is the response register for an explicit command posted by the processor.                                                                                                                                                                                                                                                                                                                                                                                |
| 8                                                                                                            | Explicit Command Register | 0x0E | 16  | [15:8] RO  | Reserved for future use                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|                                                                                                              |                           |      |     | [7] RW     | Command Request: This bit when set indicates that the processor is posting a explicit command whose index is indicated by the Command index section of the Explicit Command Register. The processor must set this bit only after setting all the command argument and command index sections of the register set. As soon as the request bit is set the Host controller frames a command and sends it to the Card. The response is updated in to the Response Register |
|                                                                                                              |                           |      |     | [6] RO     | Reserved for future use                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|                                                                                                              |                           |      |     | [5:0] RW   | Command Index Register: This section is the command index of the explicit command that the processor intends to post to the card. The section is evaluated only when the Command Request bit of the Explicit Command register is set.                                                                                                                                                                                                                                  |
| Note: In Bit Range (Access), RW stands for Read and Write, RO stands for Read Only and NA is Not Applicable. |                           |      |     |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |

Run-time/Compile time Configurations details for the hardware IP are as shown below:

## Initialization

The Initialization can be forced by the processor by writing a value 1 to force\_init bit of the iCE Design Specific Configuration Register (Address = 0x64). The package file shall have CNTRL\_FSM\_CARD\_DETECT\_SUPPORTED parameter set to 0. For an auto initialization feature, the CNTRL\_FSM\_CARD\_DETECT\_SUPPORTED parameter shall be set to a 1.

## iCE Design Specific Status Register

This is the SD Controller Status register(Address=0x80) which shall indicate a Initialization done on its init\_done bit. The processor shall read this register to check if initialization is done. The Register also has the err\_int\_init bit indicating that the initialization was unsuccessful.

## Bus width for SD operation

The processor can run-time configure the bus width for the SD operation by writing the Bus Width section bit of the iCE Design Specific Configuration Register (Address = 0x64). A value of "00" indicates a 1 bit mode of operation, a value of "01" indicates a 4-bit mode of operation and a value of "11" shall indicate a SPI mode of operation. The Controller automatically detects if the card is a SD card. The registers shall be programmed before performing the forced initialization. For compile time configuration of the bus width only the CNTRL\_FSM\_BUS\_PKG\_CONFIGURABLE parameter in the package shall be set to a 1 and CNTRL\_FSM\_BUS\_WIDTH\_SUPPORTED shall be set to corresponding values that point to 1 bit, 4 bit, SPI mode of operation.

## High speed operation

The SD Host Controller can be configured to operate at normal data rate(25MHz) and also in a High Speed data rate mode(50MHz). For run time configuration, the CNTRL\_FSM\_SPEED\_CLASS\_PKG\_CONFIGURABLE parameter in the package shall be set to a 0, and the processor can program the Speed Class section of iCE Design Specific Configuration Register. A "1" in this register indicates a switch to a high speed operation after initialization and a "0" indicates a switch to a normal transfer rate of 25MHz. For compile time configuration, the

CNTRL\_FSM\_SPEED\_CLASS\_PKG\_CONFIGURABLE shall be set to a “1” and parameter CNTRL\_FSM\_SPEED\_CLASS\_SUPPORTED shall be set to what mode is required.

### **Reset initialization statistics**

The processor can reset the initialization statistics by programming the iCE Design Specific Configuration Register bit 1 to a 1. The processor shall de-assert it once it is written. The bit acts as a soft reset to the status registers.

### **Clocking factors**

The SD Host Controller shall be operating in 3 different frequencies. When the Controller is in the initialization mode, it operates at 400KHz, and under data transfer, depending on the Speed class that is configured in the iCE Design Specific Configuration Register (Address = 0x64), the Host Controller operates at around 25MHz for normal data rate, and at 50MHz for High Speed operation. The controller uses the i\_clk provided to the system to derive the 3 clocks. The division factors are defined in the package and can be compile time programmable and depending on the frequency that can be provided to the system.

The CLK\_TREE\_INITIALIZATION\_CLK\_DIV\_FACTOR defined in the package shall be set to a value which is used to divide the system clock to extract the initialization clock of 400 KHz.

The CLK\_TREE\_DEFAULT\_SPEED\_CLK\_DIV\_FACTOR shall be used to extract the default speed clock for normal data rate operation.

The CLK\_TREE\_HIGH\_SPEED\_CLK\_DIV\_FACTOR shall be used to extract the high speed clock for High speed operation.

### **VDD window configuration**

The VDD voltage window can be configured depending on the board VDD supply voltage. This is necessary since the SD card shall operation only under matching VDD conditions which are negotiated by the SD Controller. The CNTRL\_FSM\_VDD\_WINDOW\_SUPPORTED parameter shall be set depending on the board VDD supply. The value is set to “0100” which indicates a 2.4–3.6v VDD range.

### **Command registers**

The processor can execute a SD command using a system driver environment using this register. The processor shall program the Argument0 [15:0](Address=0x08) and Argument1[15:0](Address = 0x0A) with the command arguments that shall be inserted for the command that will be posted. The processor then shall program the Command register [15:0](Address=0x0E). For posting the command, the processor can then check the response on the Response Register[127:0](Address 0x10) by using the single block read transactions multiple times to read the entire 16 bytes of response register using the single block read transactions multiple times to read the entire 16 bytes of response register.

### **SDHC support**

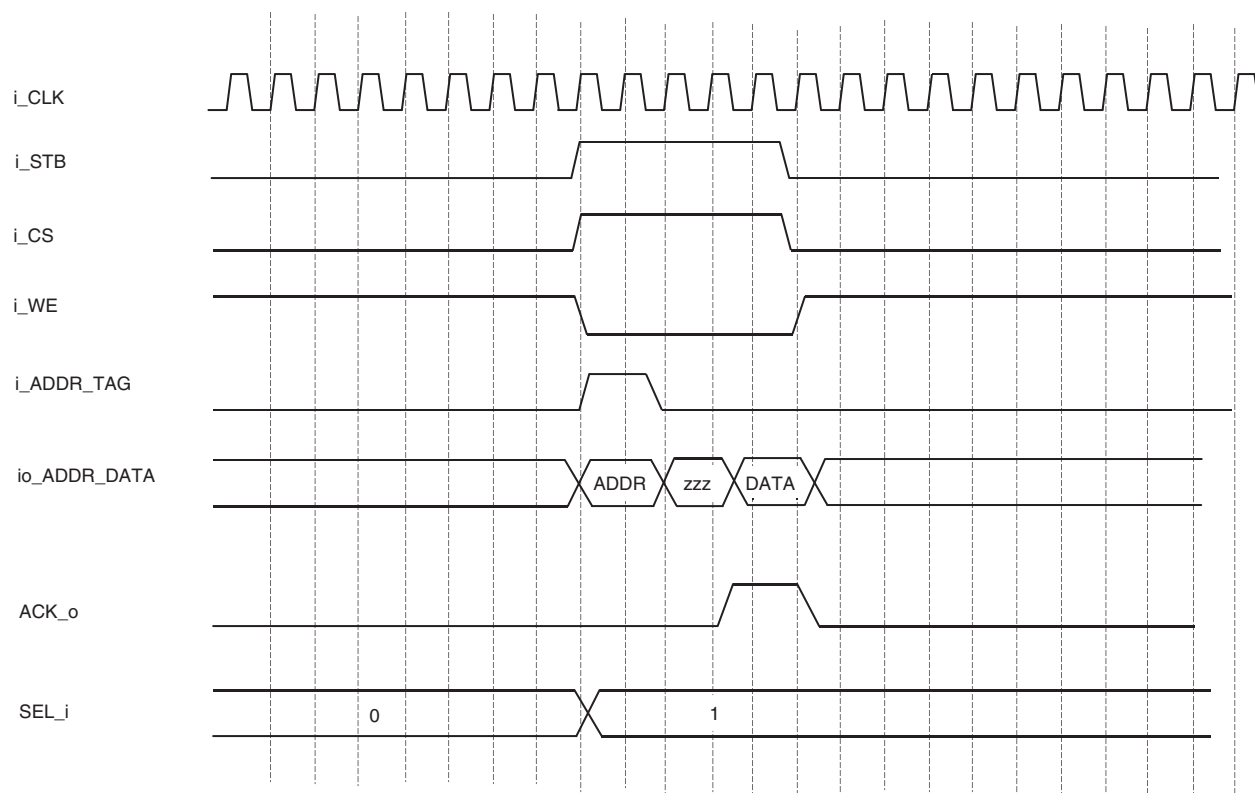
The SD Host Controller shall identify a SDHC Card (High Capacity SD Card). The information is conveyed to the processor via the CPU registers. The iCE Design Specific Status Register shall contain Card related flags and information. When the Card is detected to be SDHC card, the processor shall make sure that the BLOCK SIZE Register is always set to a value corresponding to a 512Byte block size.

## Timing Diagram

### Single Word Read Transaction

This transaction can be used to access a single 32 bit word from the SD Host Controller. This transaction is mainly used for accessing the CPU register set for reading response bytes, status registers, read write register values. The timing diagram of the transaction is shown in figure below.

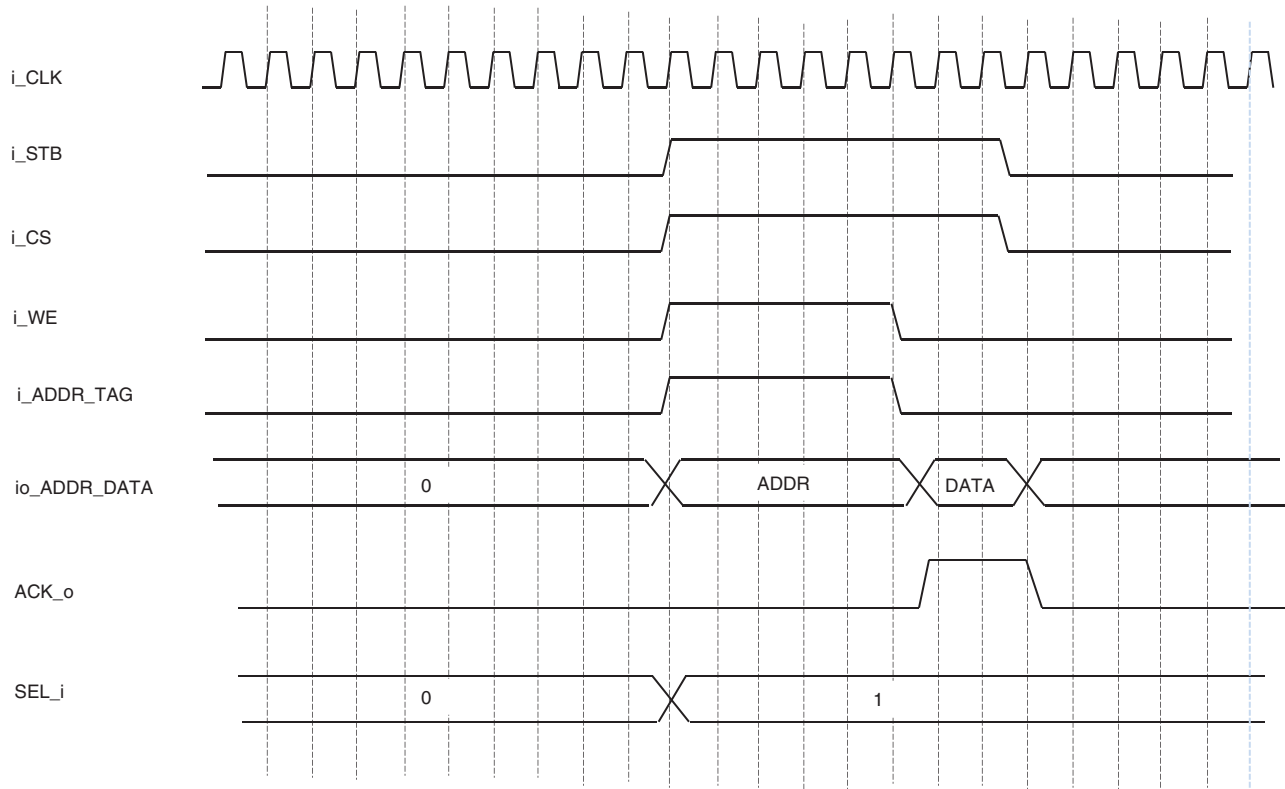
**Figure 3. Single Word Read Transaction**



## Single word write transaction

This transaction can be used to access a single 32 bit word from the SD Host Controller for programming purposes. This transaction is mainly used for writing configuration registers for forcing initialization of the SD memory, for executing SD commands from processor if required, for clearing status registers using soft resets. The timing diagram of the Single Word Write transaction is shown in figure below:

**Figure 4. Single Word Write Transaction**



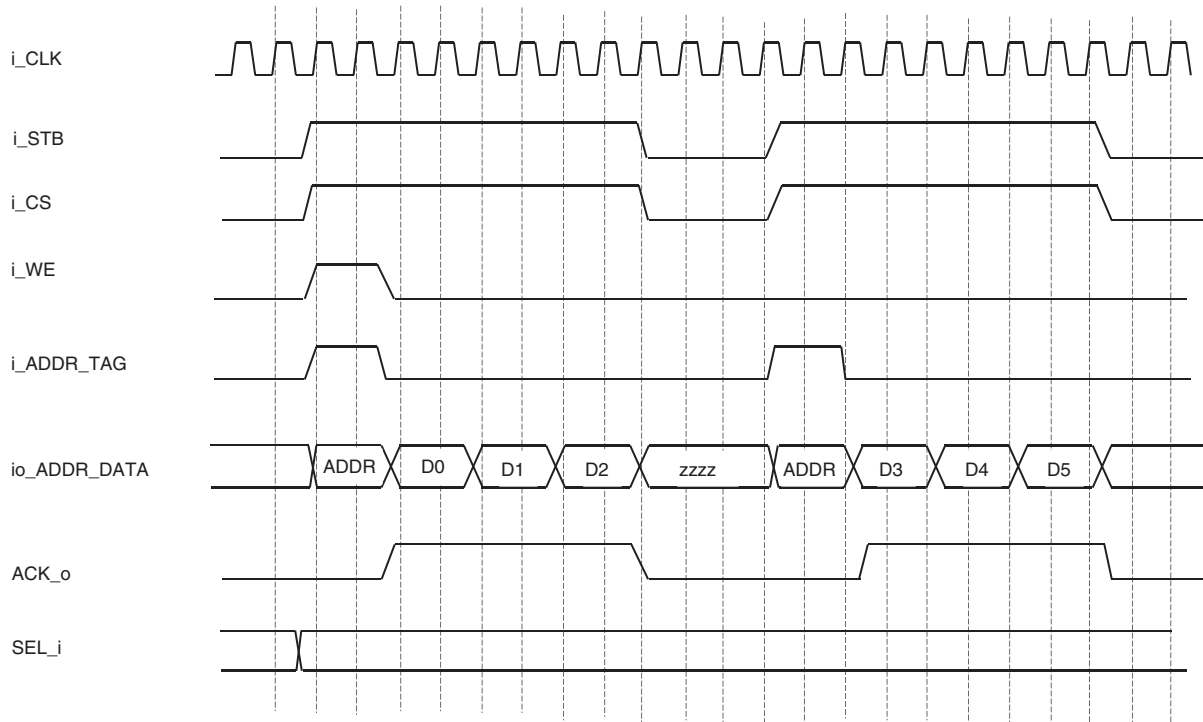
## Multiblock Read Transaction

The Processor can transfer multiple blocks of data from the SD card via the Host Controller using this transaction. The processor shall write the Block count register before performing this transaction. The host Controller shall transfer the number of blocks configured in the Block Count Register, from the SD card to the Read Write buffer and then transfer it to the processor. The sequence of operation for a multi/single block read from the SD card is as follows:

- The processor shall configure the Block Count Register [15:0] (Address= 0x06) with the number of blocks to be fetched. The maximum block count can be 16(x"0000010") for an 8Kbytes Read Write buffer. The register is configured using the single word write transaction.
- The process shall also program the Block Size Register[15:0](Address= 0x04) with a 1 for a 1024Byte block configuration, and a 0 for 512 Byte block size configuration. By default, the register is configured to 512 byte mode.
- The processor shall also program the address from which of the SD Host Controller shall read the blocks of data into the Argument0 Register [31:0] (Address = 0x08) with a 32 bit address value. The SD host controller shall post multi block or single block read commands with the address argument being the value of the register Argument0.
- The processor can now read the entire blocks of data that it configured for using the Multi Block Read transaction.

- The processor can abort the read transaction in before it reads out the entire block length of data by de-asserting the chip select.

**Figure 5. Multiblock Read Transaction**



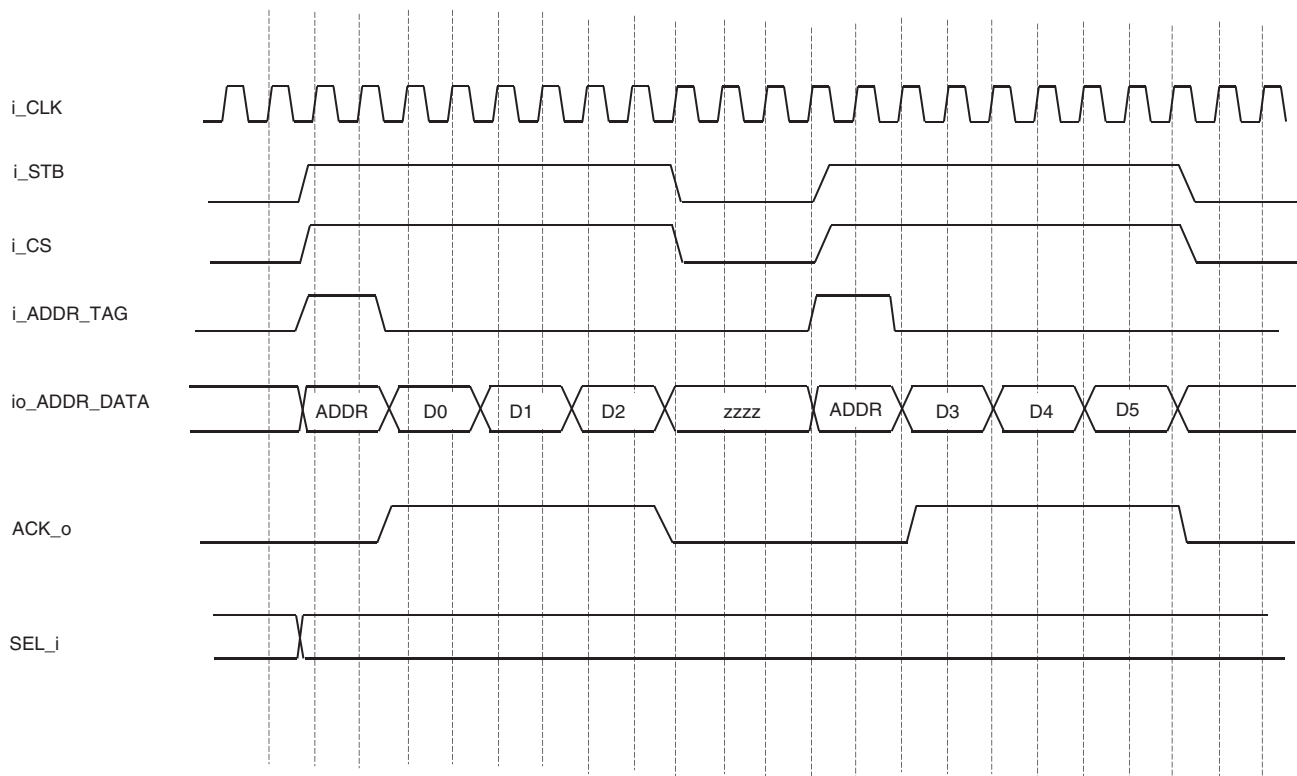
## Multiblock Write Transaction

The Processor can transfer multiple blocks of data to the SD card via the Host Controller using this transaction. The processor shall write the Block count register before performing this transaction. The host Controller shall transfer the number of blocks configured in the Block Count Register, from the Read Write buffer to the SD card. The sequence of operation for a multi/single block write transaction to the SD card is as follows:

- The processor shall configure the Block Count Register [15:0](Address= 0x06) with the number of blocks to be transferred. The maximum block count can be 16(x"0000010") for an 8Kbytes Read Write buffer. The register is configured using the single word write transaction.
- The process shall also program the Block Size Register [15:0](Address= 0x04) with a 1 for a 1024Byte block configuration, and a 0 for 512 Byte block size configuration. By default, the register is configured to 512 byte mode.
- The processor shall also program the address from which of the SD Host Controller shall read the blocks of data into the Argument0 Register [31:0] (Address = 0x08) with a 32 bit address value. The SD host controller shall post multi block or single block write commands with the address argument being the value of the register Argument0.
- The processor can now write the entire blocks of data that it configured for, using the Multi Block Write transaction.
- The processor can abort a write transaction before the minimum block length of data is transferred from the processor (less than 512 bytes), by de-asserting the chip select on the processor interface.

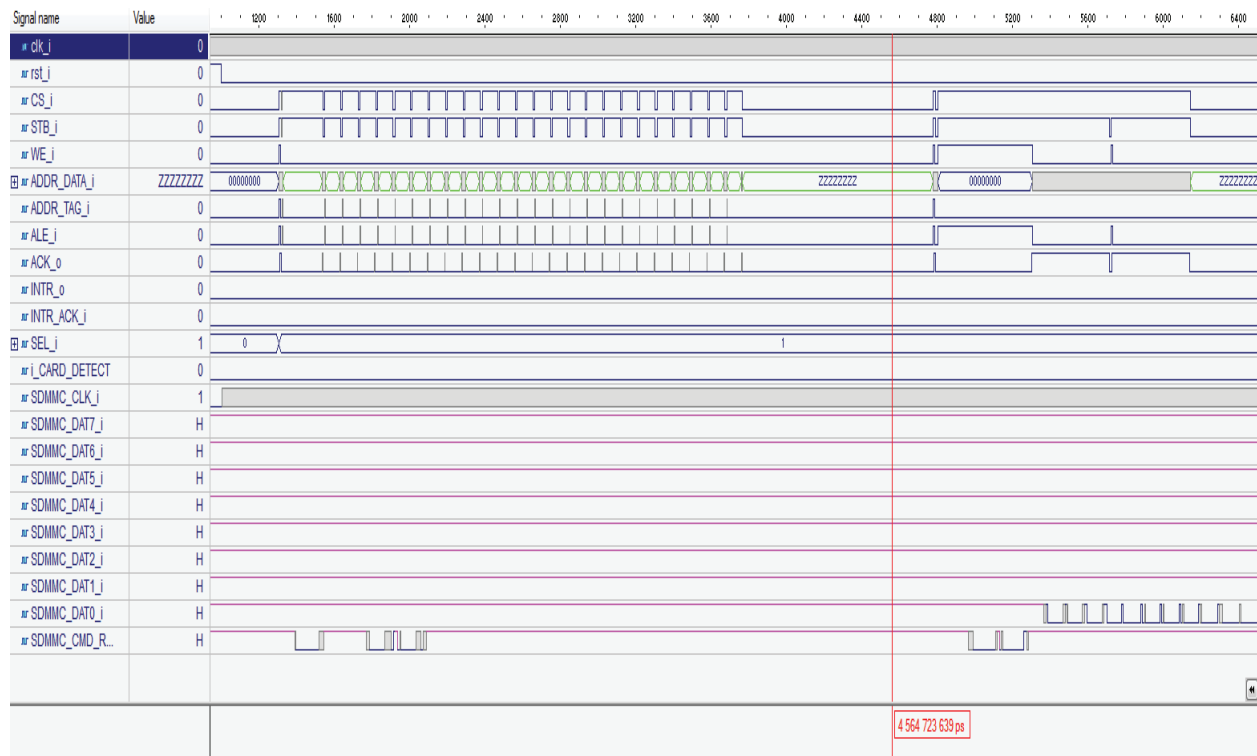
Figure 6 below shows a multiblock write transaction on the processor bus.

**Figure 6. Multiblock WriteTransaction**



## Simulation Waveforms

Figure 7. Simulation Waveforms



## Operation Sequence

1. The design is reset using the reset pin provided.
2. Initialization is initiated by the user. This is done by setting bit 0 of the iCE Design Specific Configuration Register to '1'.
3. The user next polls bit 0 of the register iCE Design Specific Status register. A '1' indicates that initialization has been completed successfully.

Please refer to the Timing Diagram section for detailed description on read and write operations.

## Implementation

This design is implemented in VHDL. When using this design in a different device, density, speed or grade, performance and utilization may vary.

Table 3. Performance and Resource Utilization

| Family             | Language       | Utilization (LUTs) | f <sub>MAX</sub> (MHz) | I/Os | Architectural Resources |
|--------------------|----------------|--------------------|------------------------|------|-------------------------|
| iCE40 <sup>1</sup> | VHDL & Verilog | 3058               | >50                    | 97   | (414/440)PLBs           |

1. Performance and utilization characteristics are generated using iCE40HX4K-TQ144 with iCEcube2 design software.

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## References

- [iCE40 Family Handbook](#)

## Technical Support Assistance

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Internet: [www.latticesemi.com](http://www.latticesemi.com)

## Revision History

| Date       | Version | Change Summary   |
|------------|---------|------------------|
| April 2013 | 01.0    | Initial release. |