MS Pro Interface

April 2013 Reference Design RD1163

Introduction

A Memory Stick (MS) is a removable flash memory card, which is used as storage media for portable devices such as digital cameras, digital music players, PDAs and cellular phones. This design example illustrates the implementation of a Memory Stick interface using Lattice iCE40™ product family of FPGAs.

The design is implemented in VHDL. The Lattice iCEcube2™ Place and Route tool integrated with the Synopsys Synplify Pro® synthesis tool is used for the implementation of the design. The design can be targeted to other iCE40™ FPGA product family devices.

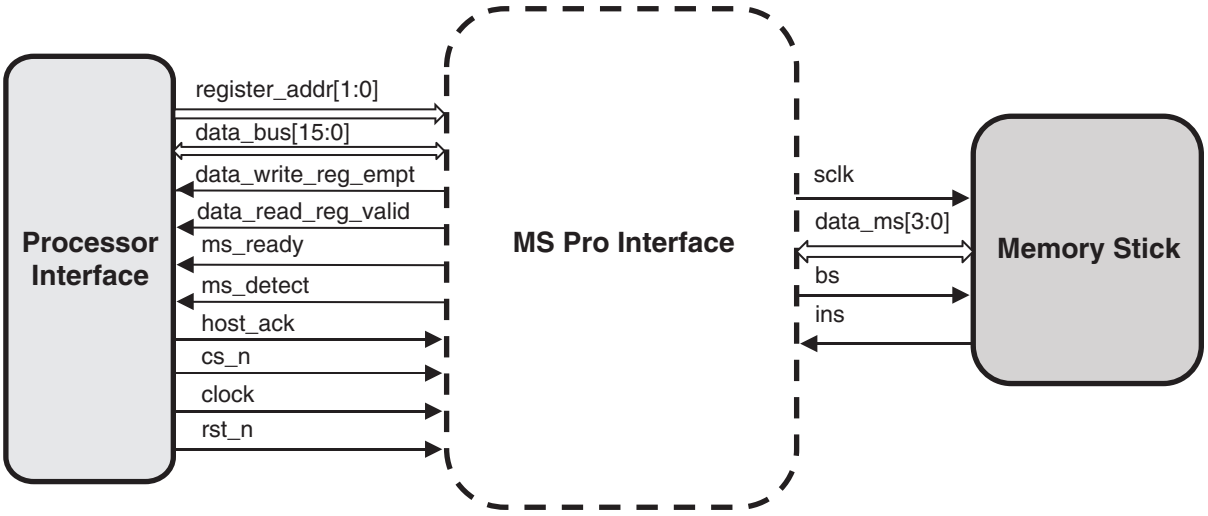
Figure 1 shows the System Block Diagram for the Memory Stick interface.

Features

- Parallel mode support
- Configurable clock frequency
- MS detect debounce logic
- Busy/Ready Interrupt generation
- Configurable data R/W size

System Block Diagram

Figure 1. System Block Diagram



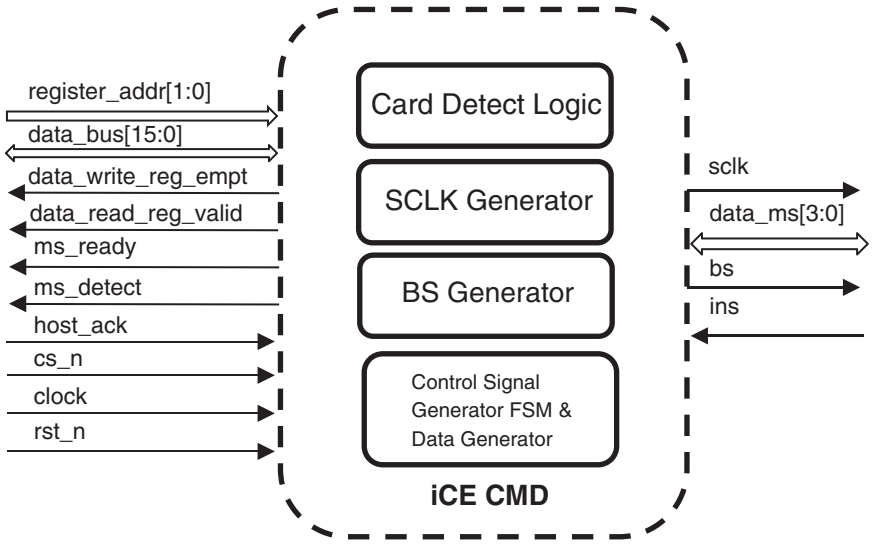
Signal Description

Table 1. Signal Description

Signal	Width	Type	Description
cs_n	1	Input	Chip select signal generated by the host
rst_n	1	Input	Asynchronous Active low system reset
clock	1	Input	System Clock
data_bus	16	Inout	Bidirectional Data bus from Host Processor
register_addr	2	Input	Select line for data or command register operation
data_read_reg_valid	1	Output	Goes high when data register is full[for read operations]
data_write_reg_valid	1	Output	Goes high when data register is empty[for write operations]
ms_detect	1	Output	Active high MS card detection to host processor
host_ack	1	Input	Host sends a high to the pin as soon as it acknowledges data_read_reg_valid or data_write_reg_valid empty signals.If not acknowledged,it suspends the communication by keeping sclk low
sclk	1	Output	Clock signal generated which is 1/4th the system clock
ins	1	Input	MS Pro insertion/removal detector.This pin goes low whenMS Pro is inserted into the socket
data_ms[3:0]	4	Inout	MS Data bus
bs	1	Output	Bus state signal.This signal operates in 4 modes. BS0:Idle state.BS is held low. BS1:TPC command write state.BS held high BS2:BS held low.If data read operation, then BUSY/RDY status available on Data lines.If Data write operation, then writes operation on Data lines. BS3:BS held high. If Data write operation, the BUSY/RDY status available on Data lines. If Data write operation, then data from MS Pro is available on Data lines.

Design Module Description

Figure 2. Functional Block Diagram



Card Detect Logic

Card Detect Logic tells the host processor if a card has been inserted or removed from the MS Pro slot. This primarily uses the signal ins to determine the status.

SCLK Generator

SCLK is the clock with which the MS pro card is synchronized. In this design, the SCLK is one fourth system clock frequency.

BS Generator

BS Generator is the bus state signal that operates in four modes:

- BS0 – Idle state. BS is held low.
- BS1 – TPC command Write state. BS held High.
- BS2 – BS held low. If data read operation, then BUSY/RDY status available on Data lines. If data write operation, then writes data on Data lines.
- BS3 – BS Held High. If data write operation, then BUSY/RDY status available on Data lines. If data read operation, then data from MS Pro is available on Data lines.

This is generated by the BS generator module as required.

Control Signal Generation FSM and Data Generator

The Control Signal Generation FSM and Data Generatorv generate the necessary control signals for the transaction with the MS Pro.

Register Mapping

There are two user accessible registers within this design. They are the command register and the data write register. These are write only registers.

When chip select “cs_n” asserted low, then command/data read/write operations are executed as follows:

- when "00" – No operation. MS Pro Stick deselected.
- when "01" – Command Write to MS IF TPC Register
- when "10" – Data Read from MS IF Data Register
- when "11" – Data Write to MS IF Data Register

Data is read/written in MSB byte first format.

Command Write Register

Command Write Register is used to configure the operation between the Host Processor and the MS Pro Stick. The register layout is as follows:

Table 2. Command Write Register

Bits[15:12]	Bits[11:10]	Bits[9:0]
TPC1	x	Number of bytes in transaction

This register can be accessed by pulling down the “cs_n” line with the register_addr line set to “01”.

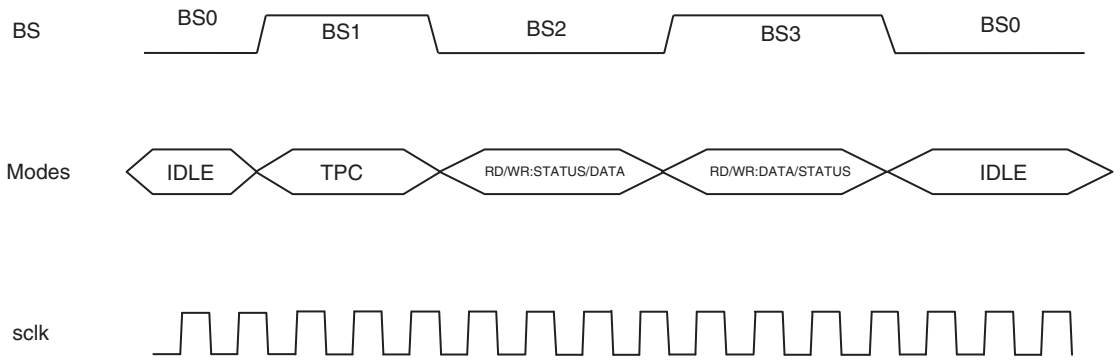
When the command register is written, the communication protocol with the MS Pro device starts. The data transfer direction with the Memory Stick is determined from TPC[3]. When TPC[3] = 0, the read protocol is performed, otherwise the write protocol is performed. When the protocol starts, ms_ready changes to ‘0’ to indicate that proto-

col execution is underway. ms_ready held 0 throughout the communication with the Memory Stick, and generates an interrupt at the end of communication by sending a High on ms_ready pin. TPC Register[15:12] is the command part and TPC[9:0] provides the Transmit/Receive Data Size information to the MS Pro IF.

data write register : This is a 16-bit data register which contains the data to be transferred during a write transaction. This register is accessed by pulling down the cs line and the register_addr line set to “11”.

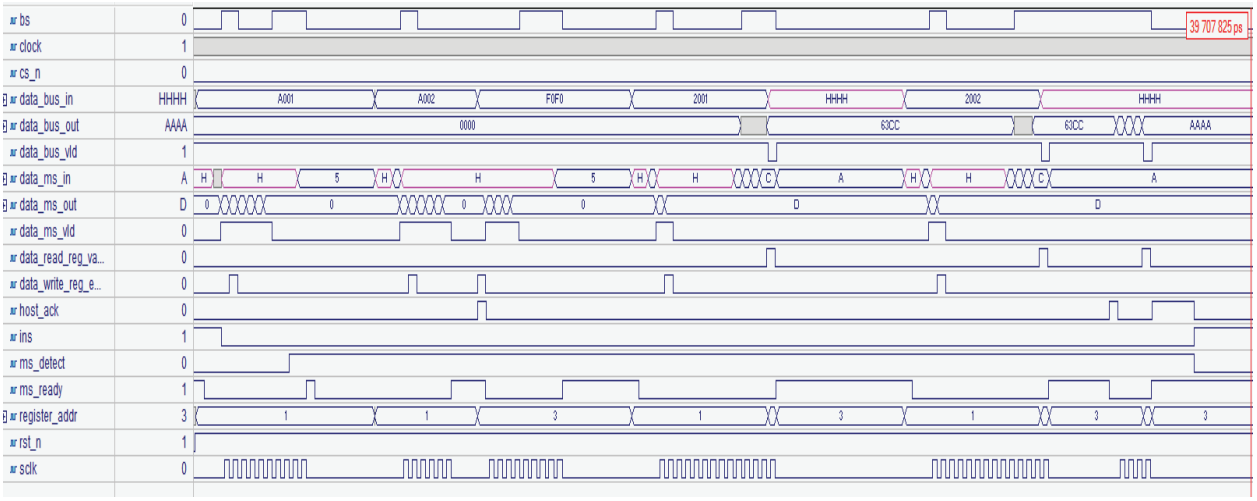
Timing Diagram

Figure 3. Timing Diagram



Simulation Waveforms

Figure 4. Simulation Waveforms



Implementation

This design is implemented in VHDL. When using this design in a different device, density, speed or grade, performance and utilization may vary.

Note: In the RTL, data_ms and data_bus signals have been taken as two separate input and output buses instead of inout bus.

Table 3. Performance and Resource Utilization

Family	Language	Utilization (LUTs)	f_{MAX} (MHz)	I/Os	Architectural Resources
iCE40[1]	VHDL	201	>50	53	(52/160)PLBs

1. Performance and utilization characteristics are generated using iCE40LP1K-CM121 with iCEcube2 design software.

References

- iCE40 Family Handbook

Technical Support Assistance

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Revision History

Date	Version	Change Summary
April 2013	01.0	Initial release.