Single Channel LVDS Tx

April 2013 Reference Design RD1162

Introduction

Low Voltage Differential Signaling (LVDS) is an electrical signaling system that can run at very high speeds over inexpensive twisted-pair copper cables. It delivers high data rates while consuming significantly less power than competing technologies. Since its introduction, it has become popular in very high speed networks and computer buses.

Source synchronous interfaces consisting of multiple data bits and clocks have become a common method for moving image data within electronic systems. A prevalent standard is the 7:1 LVDS interface (employed in Channel Link, Flat Link, and Camera Link), which has become a common standard in many electronic products including consumer devices, industrial control, medical, and automotive telematics. In many of these applications, the practice of using low-cost FPGAs for image processing has become quite common.

This document provides a brief description of an LVDS Transmitter and its implementation.

The design is implemented in VHDL. The Lattice iCEcube2™ Place and Route tool integrated with the Synopsys Synplify Pro® synthesis tool is used for the implementation of the design. The design can be targeted to other iCE40™ FPGA product family devices.

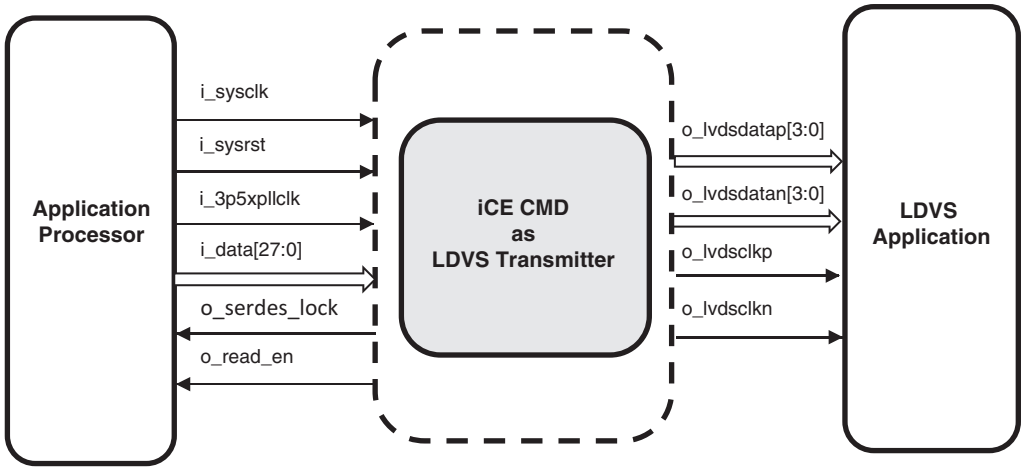
Figure 1 shows the System Block Diagram for the LVDS Transmitter.

Features

- LVDS Signaling on DDR Flip Flops
- Configurable LVDS data channels (1 to 4)
- Verilog RTL, testbench and ModelSim script for simulation

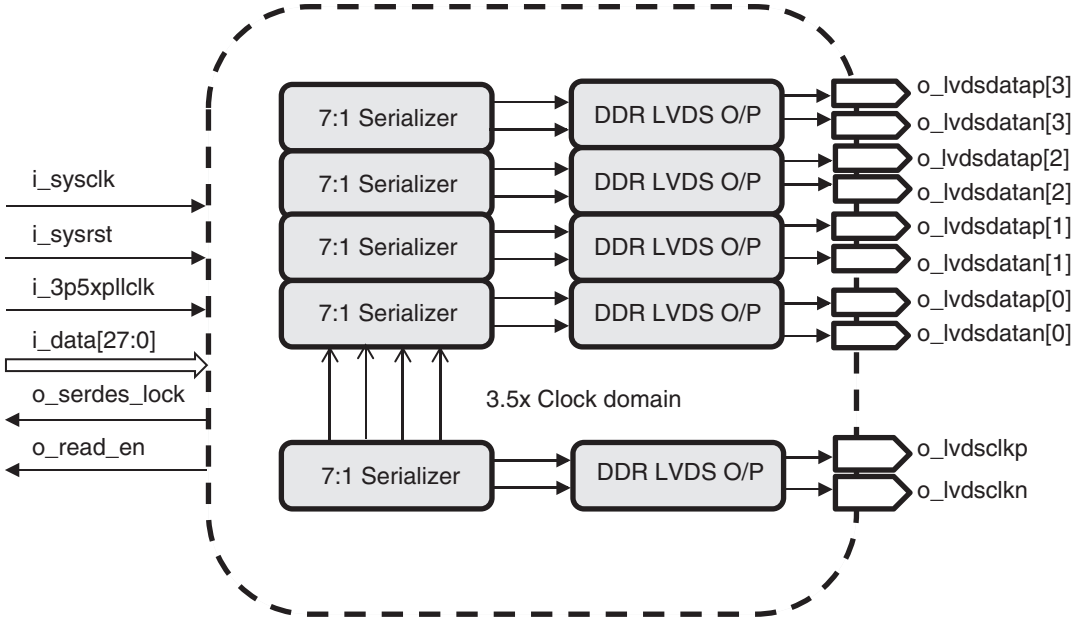
System Block Diagram

Figure 1. System Block Diagram



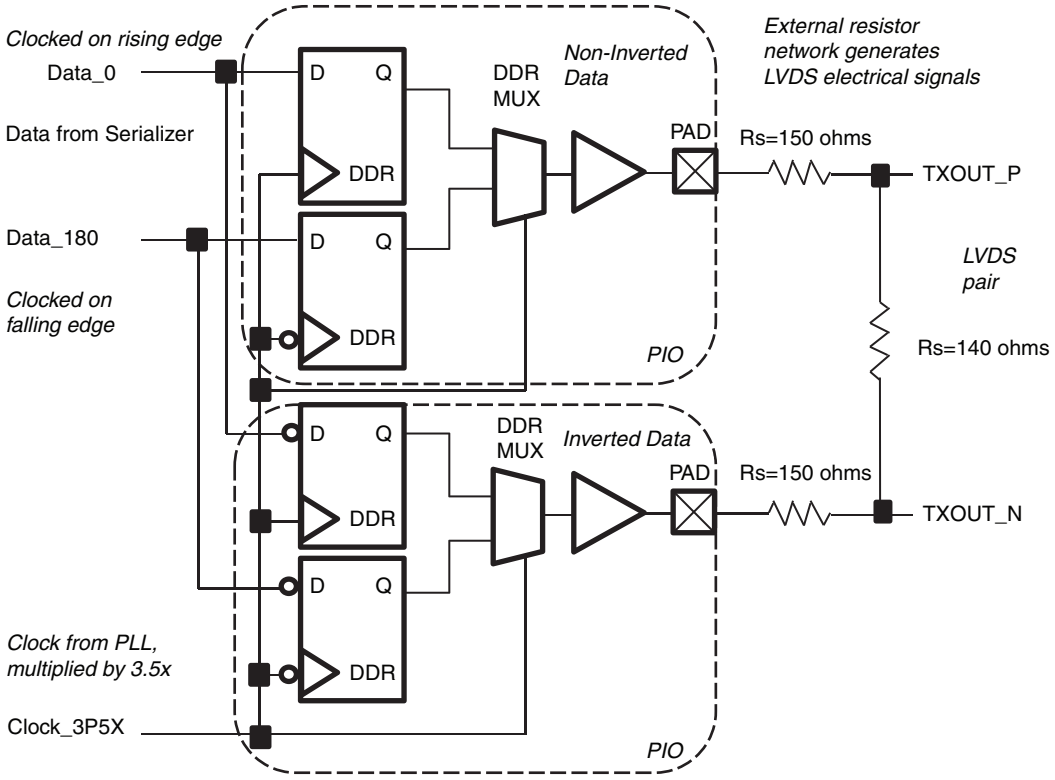
Functional Block Diagram

Figure 2. Functional Block Diagram



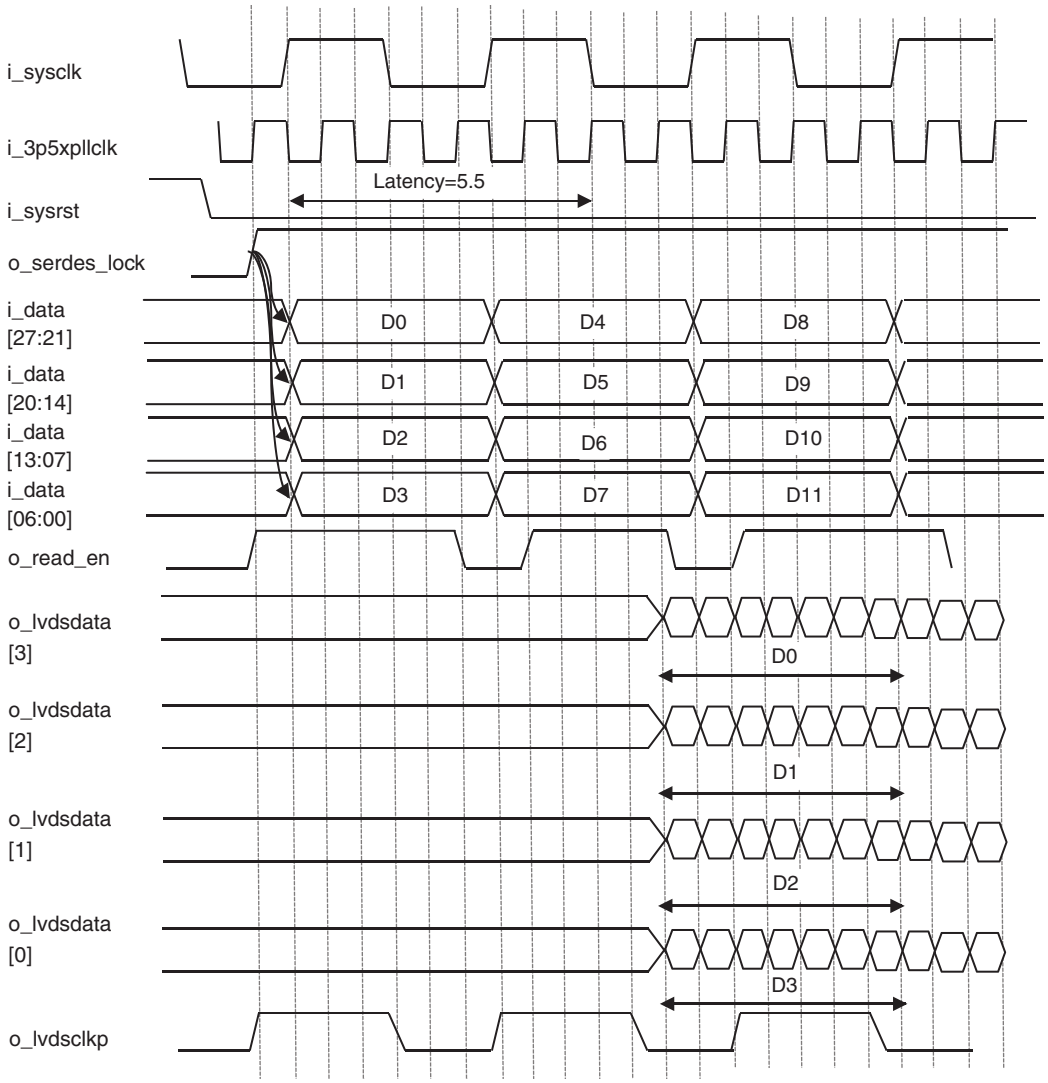
The FIFO output data (7-bit each for 4 channels) is fed to four instances of 7:1 serializers. The serializer module serializes the 7-bit parallel data to a single LVDS Data bit and transmits this single data channel along with the LVDS Clock. Usage of high speed DDR flops as shown in Figure 4, reduces the output clock rate by 50%, that is 3.5 times instead of 7 times the input clock rate. Each 7:1 serializer produces 2 outputs for the DDR LVDS output stage. Each DDR LVDS output on the iCE65 FPGA consists of 2 PIO pins and an external resistor compensation network to generate LVDS signals. One output from the serializer (DATA_0) is clocked out on the rising edge of the 3.5x clock while the other output (DATA_180) is clocked out on the falling edge. These 2 PIO pins form a complimentary LVDS pair, with one PIO pin (TXOUT_P) generating the non-inverting output while the other pin (TXOUT_N) generating the inverted output of the LVDS differential pair.

Figure 3. LVDS Differential Pair Using DDR F/Fs



Timing Diagram

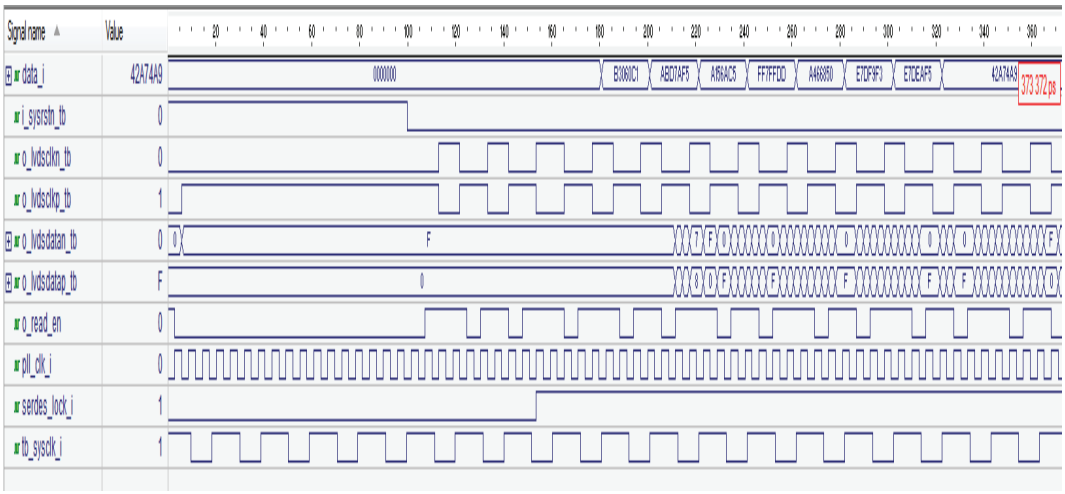
Figure 4. Timing Diagram



Data from the LVDS lines are MSB

Simulation Waveforms

Figure 5. Simulation Waveforms



Signal Description

Table 1. Signal Description

Signal	Width	Type	Description
i_sysclk	1	Input	Pixel clock for LVDS display
i_sysrst	1	Input	Active High System Reset
i_3p5pllclk	1	Input	3.5x of pixel clock for LVDS Display
i_data	28	Input	FIFO output data, with the read clock same as i_sysclk
o_serdes_lock	1	Output	SERDES lock signal. Only when this signal is high, the LVDS_Tx module is ready to accept input data
o_read_en	1	Output	Read enable signal to FIFO
o_lvdsdatap	4	Output	LVDS non-inverted data output
o_lvdsdatan	4	Output	LVDS inverted data output
o_lvdsclkp	1	Output	LVDS non-inverted clock output
o_lvdsclkn	1	Output	LVDS inverted clock output

Usage Example

Figure 6 shows the top level block diagram of an LVDS Display used with the LVDS Transmitter. Both the input pixel clock (i_sysclk) and 3.5x clock (i_3p5xpllclock) must be generated from the PLL in the Data generator.

Figure 6. Top Level Diagram of LVDS Display Used with the LVDS Transmitter

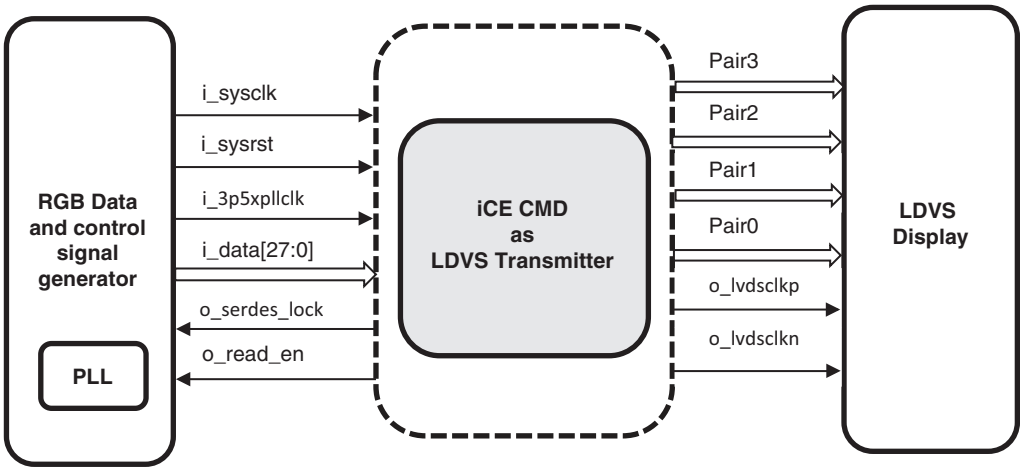
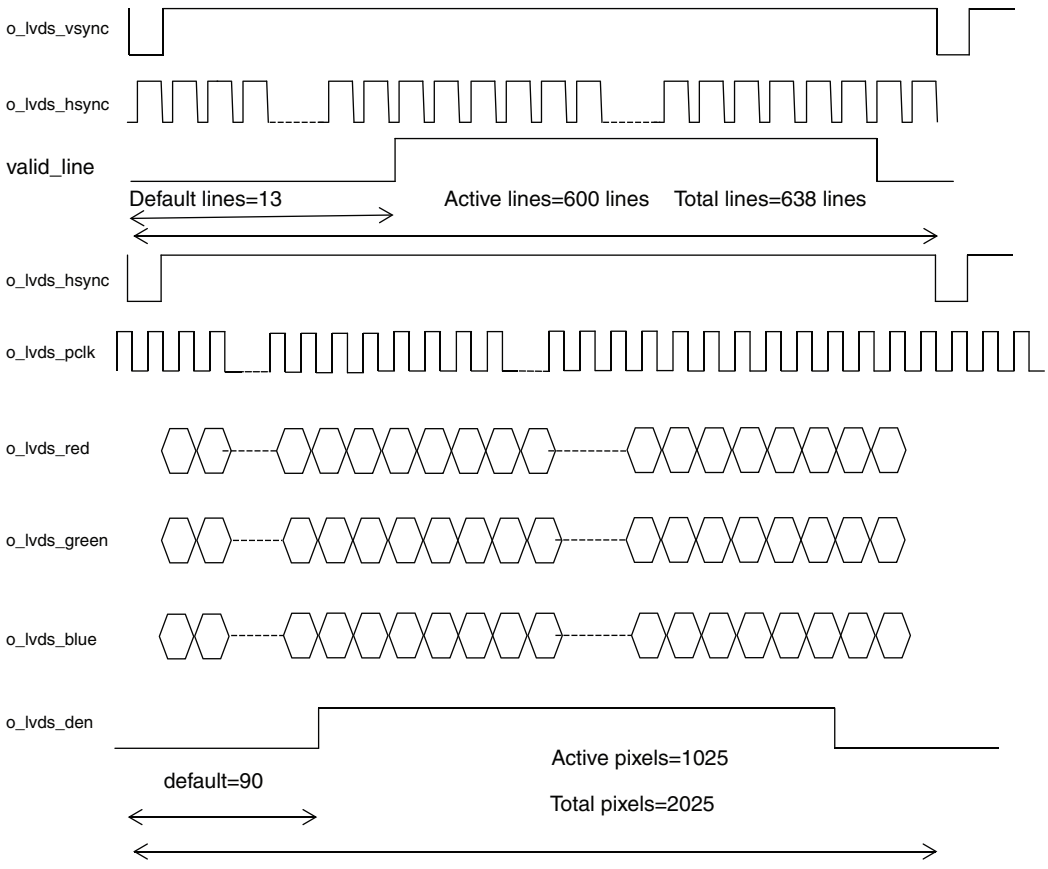


Figure 7 shows the generation of the control signals – HSYNC, VSYNC, DEN and 18-bit RGB data to the LVDS display. The display resolution in this case is 1024 x 600. The LCD control signals are generated based on the predetermined porch timing values of the display.

Figure 7. LVDS Display Timing Generation



Configurable parameters

NUM_CHANNELS : This parameter configures the number of LVDS data channels required. The values can range from 1 to 4

Initialization Condition

When 'i_sysrst' is HIGH, all the output LVDS signals will be low.

Operation Sequence

1. De-assert the ‘i_sysrst’ signal
2. Wait until the ‘o_serdes_lock’ signal goes high, indicating that the LVDS Tx is ready to accept the input data
3. o_read_en signal is used to read FIFO
4. Start writing the 28-bit RGB data and control signals as per the LVDS LCD specifications to the LVDS Tx on the positive edge of ‘i_sysclk’ to the DUT as shown in Figure 5.
5. There is a latency of 5.5 cycles of i_3p5xpllclk for the first serial data output, and there afterwards the serial data is available in pipelined fashion for the LVDS Display as shown in Figure 5.

Implementation

This design is implemented in VHDL. When using this design in a different device, density, speed or grade, performance and utilization may vary.

Table 2. Performance and Resource Utilization

Family	Language	Utilization (LUTs)	f_{MAX} (MHz)	I/Os	Architectural Resources
iCE40[1]	VHDL	123	>50	41	(21/160)PLBs

1. Performance and utilization characteristics are generated using iCE40LP1K-CM121 with iCEcube2 design software.

References

- iCE40 Family Handbook

Technical Support Assistance

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Revision History

Date	Version	Change Summary
April 2013	01.0	Initial release.