Graphics LCD Controller

Introduction

Liquid Crystal Display (LCD) is a flat display device used in many electronic products to view images and videos. These slim and thin packages, known for their low power characteristics, are an excellent choice for consumer applications. LCD devices are also found in demo boards and evaluation tools to provide debugging capabilities. Use of these devices has been simplified with on-board controllers, on-board drivers, and generic interfaces available on most LCD modules. This document provides a brief description of LCD Controller and its implementation.

The design is implemented in VHDL. The Lattice iCEcube2™ Place and Route tool integrated with the Synopsys Synplify Pro® synthesis tool is used for the implementation of the design. The design can be targeted to other iCE40™ FPGA product family devices.

Features

- Configurable image resolutions (maximum of 1280 x 800)
- Configurable Front and Back Porches for both VSYNC and HSYNC signals
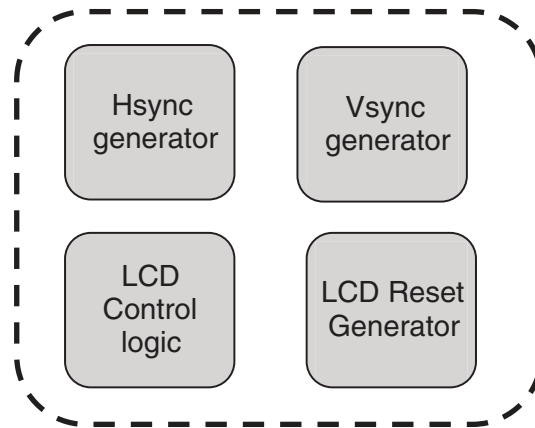- Configurable VSYNC and HSYNC Pulse widths and polarities

System Block Diagram

Figure 1. Block Diagram
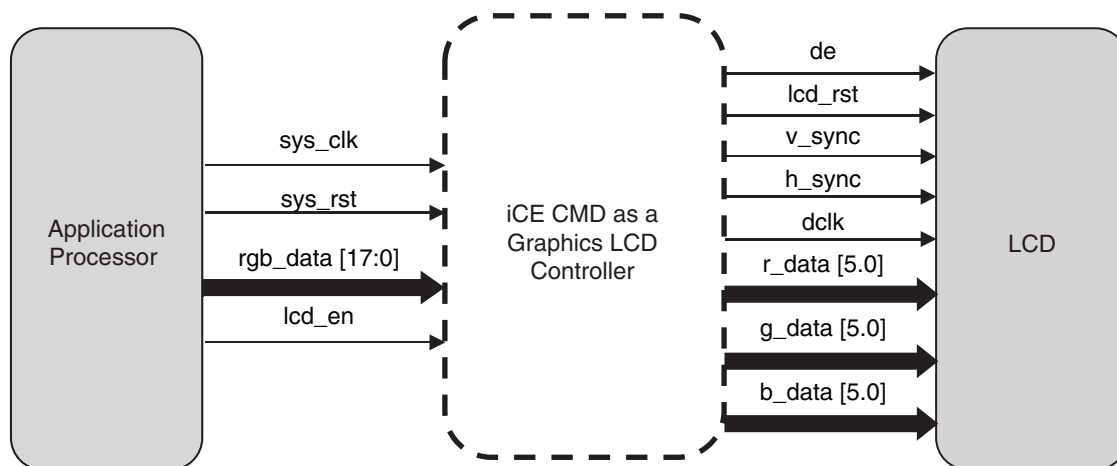
Functional Description

Figure 2. Functional Model

Design Module Description

HSYNC Generator

Generates the HSYNC signal to the LCD based on a 11-bit pixel counter, which keeps track of the active and dummy pixels per frame. It also depends on the HSYNC pulse width, HSYNC back and front porch and the image width.

VSYNC Generator

Generates the VSYNC signal to the LCD based on a 11-bit line counter, which keeps track of the active and dummy lines per frame. It also depends on the VSYNC pulse width, VSYNC back porch and the image height.

LCD Control Logic

Generates the DE signal as well as the RGB data to the LCD. The data coming out of the Graphics LCD Controller is valid only when DE is high.

LCD Reset Generator

Generates the LCD Reset signal. The polarity of the Reset signal can be configured in the package. The Reset signal is generated after 1 ms.

There is one module TIFF that transforms raw pixel data into a format compatible with the tag image file format, TIFF.The signals associated with this module are explained in the source code.

More information about these four modules and the top are present in their respective source codes.

Configurable Parameters

V_SYNC_BACK_PORCH

This is the distance between the top of the display to the upper most portion of the actual image. Its default value is 20. This can be modified as per the LCD used.

V_SYNC_FRONT_PORCH

This is the distance between the bottom of the display to the lower most portion of the actual image. Its default value is 28. This can be modified as per the LCD used.

V_SYNC_ACTIVE

The height of the actual image. Its default value is 1280.

V_SYNC_PULSE_WIDTH

This is used to signify the beginning of a new frame. Its default value is 2. This can be modified as per the LCD used.

V_SYNC_POL

This is the polarity of the VSYNC signal. It can be active high (1) or active low (0). This can be modified as per the LCD used.

H_SYNC_BACK_PORCH

This is the distance between the left part of the display to the left most portion of the actual image. Its default value is 40. This can be modified as per the LCD used.

H_SYNC_FRONT_PORCH

This is the distance between the right part of the display to the right most portion of the actual image. Its default value is 24. This can be modified as per the LCD used.

H_SYNC_ACTIVE

The width of the actual image. Its default value is 800.

H_SYNC_PULSE_WIDTH

This is used to signify the beginning of a new line in the frame. Its default value is 6. This can be modified as per the LCD used.

H_SYNC_POL

This is the polarity of the HSYNC signal. It can be active high (1) or active low (0). This can be modified as per the LCD used.

Signal Description

Table 1. Signal Description

| Signal name	Pin Type	Signal Description
sys_clk	Input	System clock
sys_rst	Input	Asynchronous Active Low System Reset
lcd_en	Input	Enable signal to the LCD controller
rgb_data[17:0]	Input	RGB Data
v_sync	Output	VSYNC signal to the LCD
h_sync	Output	HSYNC signal to the LCD
de	Output	DE signal to the LCD
dclk	Output	DCLK signal to the LCD
lcd_rst	Output	RESET signal to the LCD
r_data	Output	Red Component to the LCD
g_data	Output	Green Component to the LCD
b_data	Output	Blue Component to the LCD

Timing Diagram

Figure 3. Timing Diagram
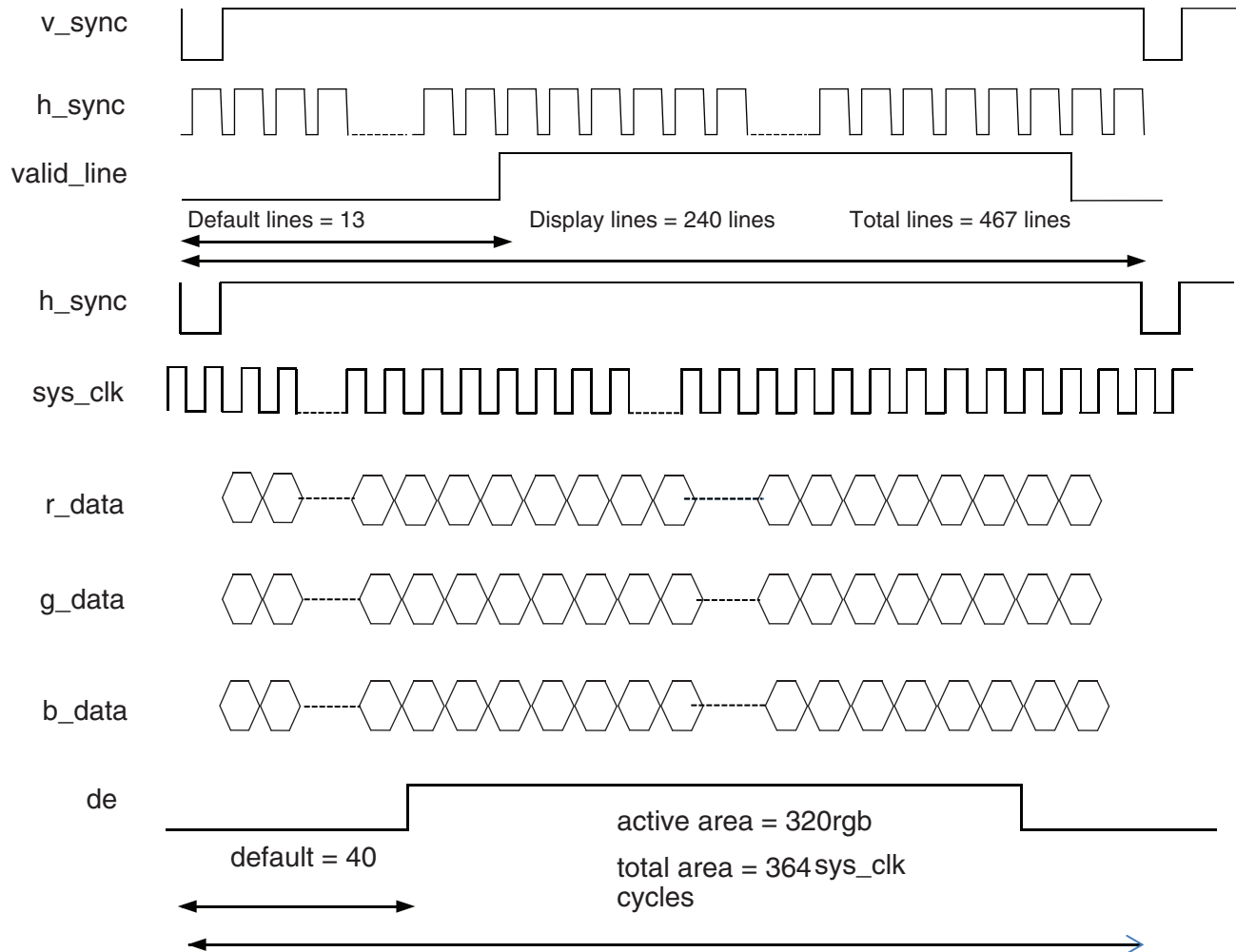
Simulation Waveforms

Figure 4. Simulation Waveforms
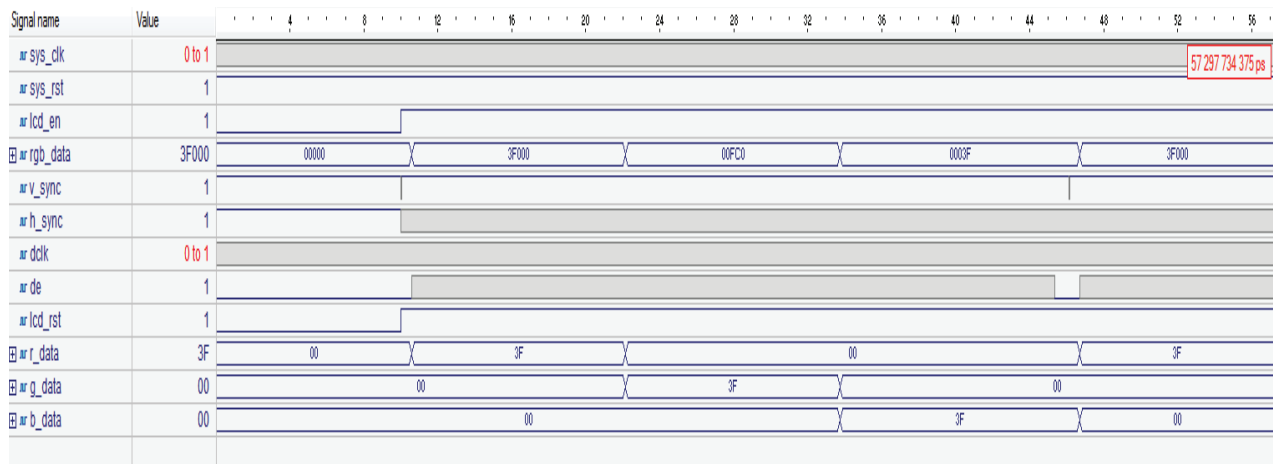
Implementation

This design is implemented in VHDL. When using this design in a different device, density, speed or grade, performance and utilization may vary.

Performance and Resource Utilization

Table 2. Performance and Resource Utilization

Family	Language	Utilization (LUTs)	f_{MAX} (MHz)	I/Os	Architecture Resources
iCE40[1]	VHDL	205	>50	46	(52/160) PLBs

1. Performance and utilization characteristics are generated using iCE40-LP1K-CM121 with iCEcube2 design software.

References

- iCE40 Family Handbook

Technical Support Assistance

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Revision History

Date	Version	Change Summary
April 2013	01.0	Initial release.