Panasonic Image Sensor Bridge with WDR Preprocessor

October 2012 Reference Design RD1133

Introduction

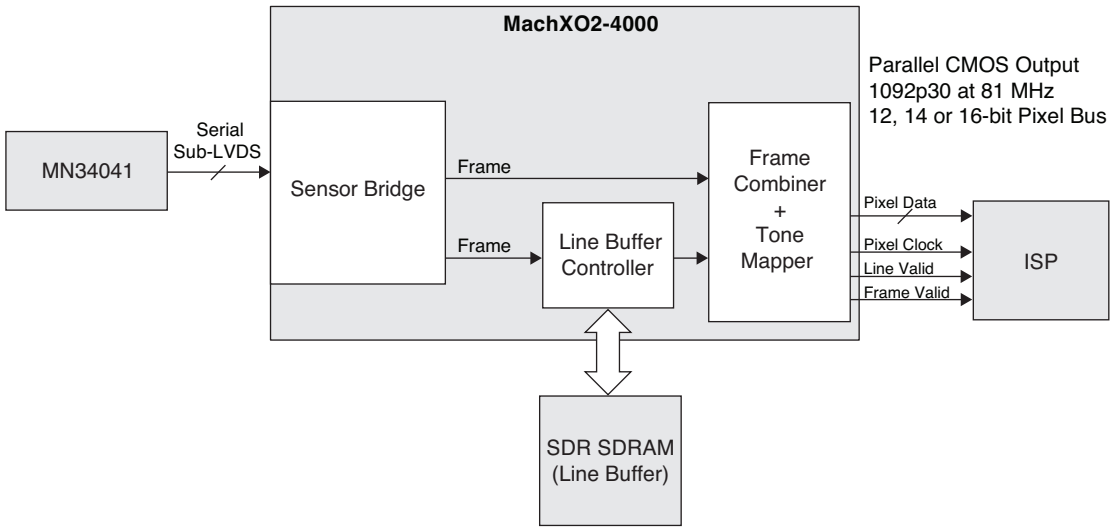
The dynamic range of the human eye is approximately 80-160dB depending on lighting conditions. Typical image sensors have a dynamic range between 48-72dB, which results in saturation of the brightest and darkest portions of the image. Wide Dynamic Range, also referred to as High Dynamic Range, is a method for achieving a greater amount of dynamic range through image processing techniques. Currently, the most common technique for increasing dynamic range with image sensors is to take two different exposures of the same image at virtually the same time. The images are then combined and compressed to utilize the same bandwidth as the standard dynamic range image. The result is an image with much higher dynamic range.

The Panasonic MN34041 image sensor is WDR capable at 1092x1944p30. The sensor captures a long and short exposure at virtually the same moment in time. The long and short exposures are packaged in separate frames and delivered over a serial sub-LVDS bus with separate unique synchronization codes.

The Lattice Panasonic Image Sensor Bridge with WDR Preprocessor reference design accomplishes two main tasks:

1. Converts the serial sub-LVDS bus from the image sensor into a standard parallel CMOS bus that most ISPs can interface to. We refer to this as the sensor bridge function.
2. Offloads the ISP from needing to handle and post-process long and short exposure frames. By using buffers and logic, both frames are combined and operated on before sending out to an ISP.

Figure 1. Functional Hardware System Block Diagram



The Lattice MachXO2™ device is configured to take in four sub-LVDS data and two sub-LVDS clock lanes from the Panasonic MN34041. The sensor bridge module deserializes the data lanes, aligns the deserialized lanes to each other and extracts the long and short exposures. The long and short exposures each have a 12-bit pixel width and are parsed separately based on their own unique synchronization codes. See the Panasonic data sheet and appendices for details.

There is a significant time difference between when the long exposure and short exposure frames start. Horizontal time differences are static, while vertical time differences are dependent on the exposure accumulation time.

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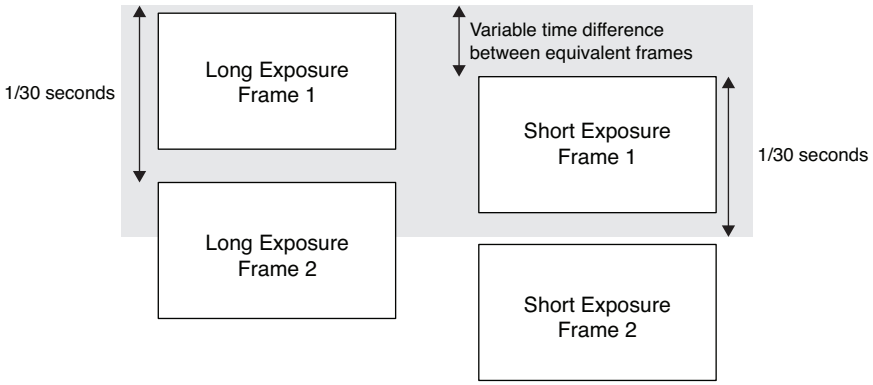
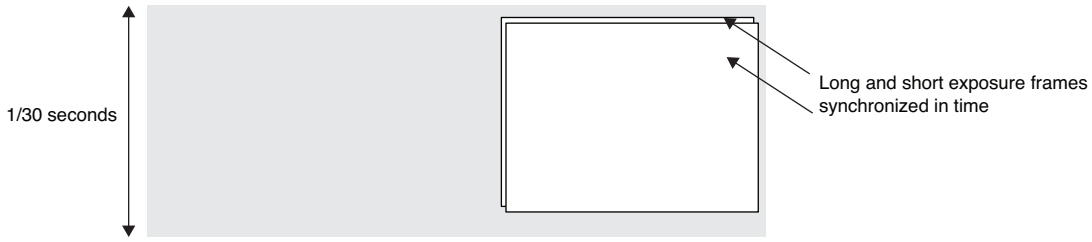
Figure 2. Visualization of Frame Offset in Time



Both frames need to be synchronized horizontally and vertically in time. For this reason an external LP single data rate SDRAM is used to line buffer the long exposure frame and synchronize both frames in time. The long exposure frame is output from the line buffer when the beginning of the short exposure frame starts to read from the MN34041.

Figure 3. Visualization of Post-Vertical Fame Alignment in Time



Once both frames are synchronized, the clock speed of each frame is reduced in half by taking advantage of the extra blanking space after horizontal and vertical synchronization. For the Panasonic MN34041 image sensor, the combined output frame rate will be 1092p30.

Figure 4. Visualization of Frame Down-Conversion in Time

The frame combining logic aggregates the two individual frames to a single image. Techniques are used to reduce image ghosting effects and color differences at the transition points with each RGB component. 12-bit and 16-bit output formats are supported. The 12-bit output is produced using a proprietary local tone mapping algorithm which compresses the combined 16-bit linearized image with virtually no data loss.

Design Demonstration

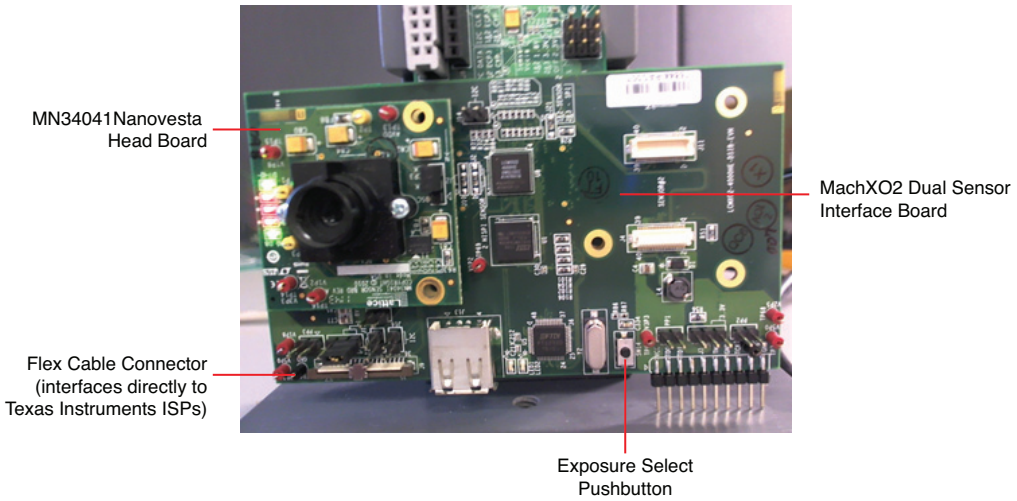
This reference design can easily be evaluated by utilizing the Lattice MN34041 Nanovesta Head Board, the Lattice MachXO2 Dual Sensor Interface Board (only one sensor port used for this application) and an image signal processor that utilizes a parallel CMOS input bus. One option is the Lattice HDR-60 Base Board with the LatticeECP3™ device. This can be used as an ISP and can display the WDR processing results on a HDMI monitor. Another option is to use the 36-pin connector with a flex cable to connect to an ISP. Custom designs can easily

interface to the Lattice Dual Sensor Interface Board using the schematic available in EB69, MachXO2 Dual Sensor Interface Board User's Guide.

Demonstration bitstreams are provided for using the MN34041 NanoVesta, the MachXO2 Dual Sensor Interface Board, and the Lattice HDR-60 Development Kit. When using this demonstration setup, the sensor is automatically programmed via I^2C. A frame doubler converts the video stream to 1080p60 so it can be viewed on a capable monitor or TV. Jumper settings off of the Aptina Header on the HDR-60 evaluation board allow the user to adjust the exposure gain over the 12 bits or enable a simple autoexposure feature.

A reference design bitstream is also provided for the MachXO2 Dual Sensor Interface Board. This bitstream's pinout matches Table 3 and should be used when connecting to an ISP other than the HDR-60 evaluation board. The sensor will need to be programmed via SPI with the configuration file contained in the *\docs folder of the reference design.

Figure 5. WDR Demonstration Platform Setup



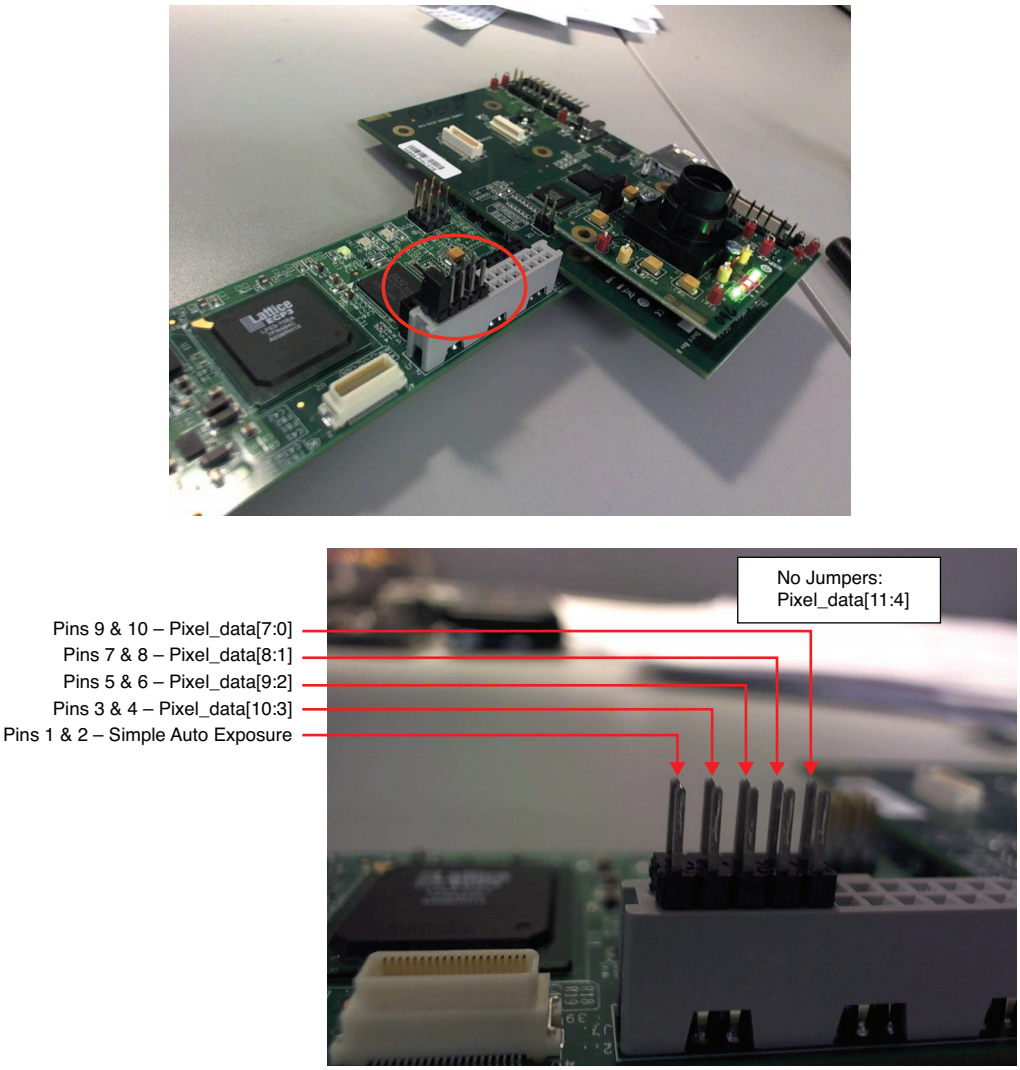
Demonstration Bitstreams

- Panasonic_WDR_12bit_RefDes_12bit_*.jed – 12-bit WDR output with pinout matching Table 3
- Panasonic_WDR_12bit_Demo_*.jed – Split non-WDR/WDR Demo to be used with HDR-60
- HDR-60_framedoubler_Demo_AE_*.bit – 1080p60 output, to be used with Panasonic_WDR_12bit_Demo_*.jed

Jumper configuration for the demonstration bitstreams and the reference design are quite simple if utilizing the HDR-60 as an ISP. No jumpers should be populated on the HDR-60 Base Board or MachXO2 Dual Sensor Interface Board. The Panasonic MN34041 Nanovesta should have a jumper on J2 on pins 2 and 3. This routes the 27 MHz oscillator from the MachXO2 Dual Sensor Interface Board to the MN34041 Nanovesta Head Board. For applications using a different ISP, regulators on the MachXO2 Dual Sensor Interface Board are fully configurable to 1.8V, 2.5V or 3.3V. Consult EB69, MachXO2 Dual Sensor Interface Board User's Guide for details.

The HDR-60 demonstration bitstream contains an 8-bit debayer. By default, the debayer will utilize pixel_data[12:4] of the incoming image data. Jumpers can be added to the Aptina header on the HDR-60 Evaluation Board to control pixel data used by the debayer as seen in Figure 6 if desired.

Figure 6. HDR-60 Demonstration Bitstream Exposure Control Jumpers



When utilizing the reference design bitstream, the sensor can be configured using the pinout below. These signals provide SPI port access to the sensor via passthrough signals in the FPGA design.

Table 1. SPI Pin Descriptions

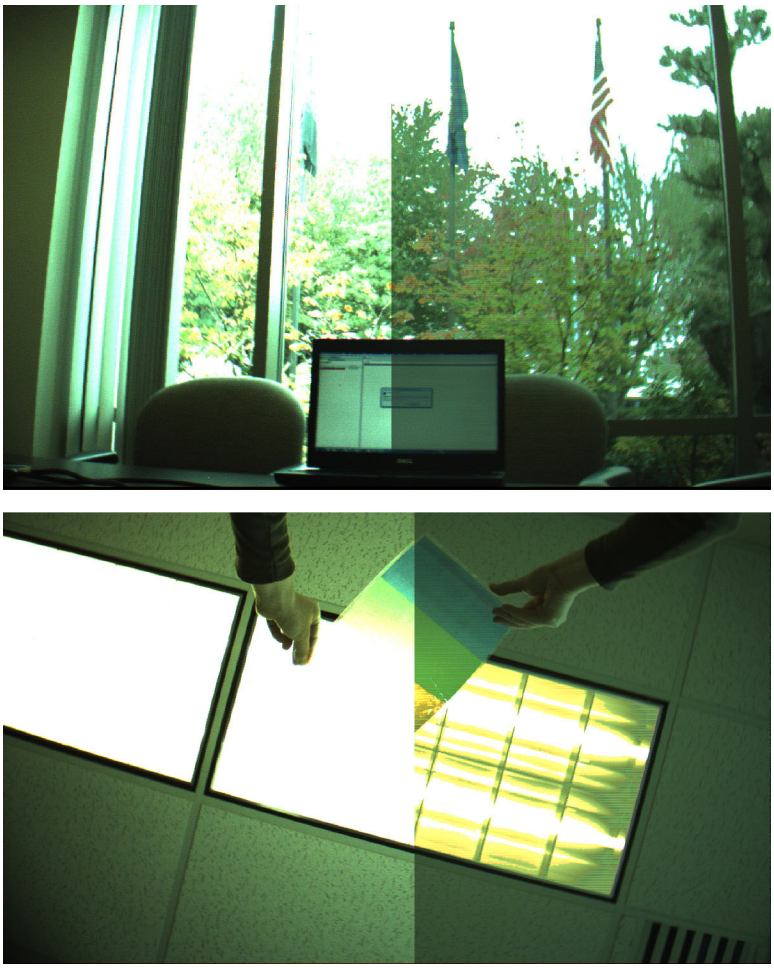
SPI Signal	ISP Direction	DSIB Schematic Signal Name	J9 Flex Connector Pin
SCS	Output	SADDR_2	34
SCK	Output	SCLK_2	32
MOSI	Output	SDATA_2	31
MISO	Input	ECP3_PRL_SDATA	30

Design Demonstration Results

The demonstration bitstream provides a split screen image through the HDMI port on the HDR-60 Evaluation Board. The left side contains the non-WDR image. The image on the right side shows the WDR output. The exposure of the non-WDR and WDR images are equivalent to each other around the midrange.

The images in Figure 7 show the performance of the WDR preprocessor in bright lighting conditions. You can see on the left hand side the images show areas of heavy saturation. On the other hand, the WDR image on the right side retains all the detail lost in the saturation areas. Note that both images appear to look the same in the mid-range of the image. As the image gets brighter, the WDR image gets brighter at a slower rate than the non-WDR image.

Figure 7. Performance of the WDR Preprocessor in Bright Lighting Conditions



The images in Figure 8 show improvements in performance under dark lighting conditions. Note that both images appear to look the same in the midrange of the image. As the image gets darker, the WDR image gets darker at a much slower rate than the non-WDR image. One would expect this to be the case in order to retain as much information from both images, without unrealistic changes in contrast and luminance.

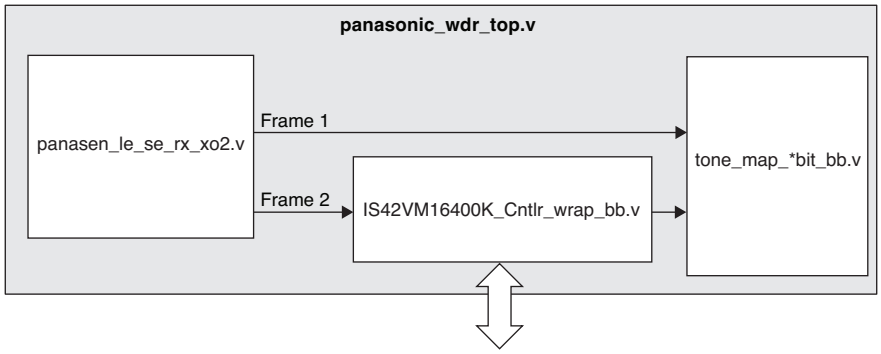
Figure 8. Improvements in Performance Under Dark Lighting Conditions

Reference Design

A complete reference design targets the MachXO2-4000HE in a 132-ball csBGA package. The reference design consists of three main modules:

- panasen_le_se_rx_xo2.v – Sensor bridge with long/short exposure outputs
- is42vm16400sdr_wrap_bb.v – SDR SDRAM line buffer controller
- tone_map_12bit_bb.v – Frame combiner and tone mapper

Figure 9. Reference Design Top Level Block Diagram



The design is configured for 12-bit compressed output by default, but can easily be changed to 16-bit linearized by changing the bus_width_out parameter on line 33 of panasonic_wdr_top.v.

Figure 10. Parameter for Output Bus Width

```
29  module panasonic_wdr_top #(
30    parameter pmi_family     = "XO2"  ,       //"ECP3" or "XP2" or "XO2"
31    parameter c_148_5_CONV   = "false",       //  true will convert the 162Mhz parallel output to 148.5Mhz (to be used with 27Mhz input clock)
32    parameter spi_ctrl       = "ext"  ,       // int = internal SPI controller, ext = external SPI controller
33    parameter bus_width_out  = 12             // 12, 14 or 16 bit
34    )(
```

All other parameters in panasonic_wdr_top.v are reserved and should be left in the their original state.

Table 2. panasonic_wdr_top.v Parameters

Parameter	Default	Setting Options	Description
pmi_family	“XO2”	Reserved	Reserved
spi_ctrl	“ext”	Reserved	Reserved
demo	“off”	“on”, “off”	Turns non-WDR/WDR screen on/off
bus_width_out	12	12, 16	Output Bus Width

Design NGO Files

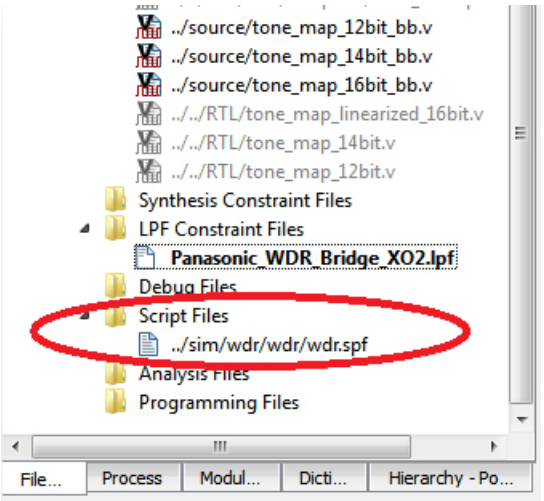
Multiple NGO files instantiate key elements of the design. These elements are:

- tone_map_*12bit.ngo – Frame Combiner and Tone Mapping Algorithm
- sdr_wrap.ngo – Line Buffer Memory Controller
- panasen_bridge_le_se.ngo – Panasonic Sensor Bridge with Long and Short Exposure Outputs

Simulation

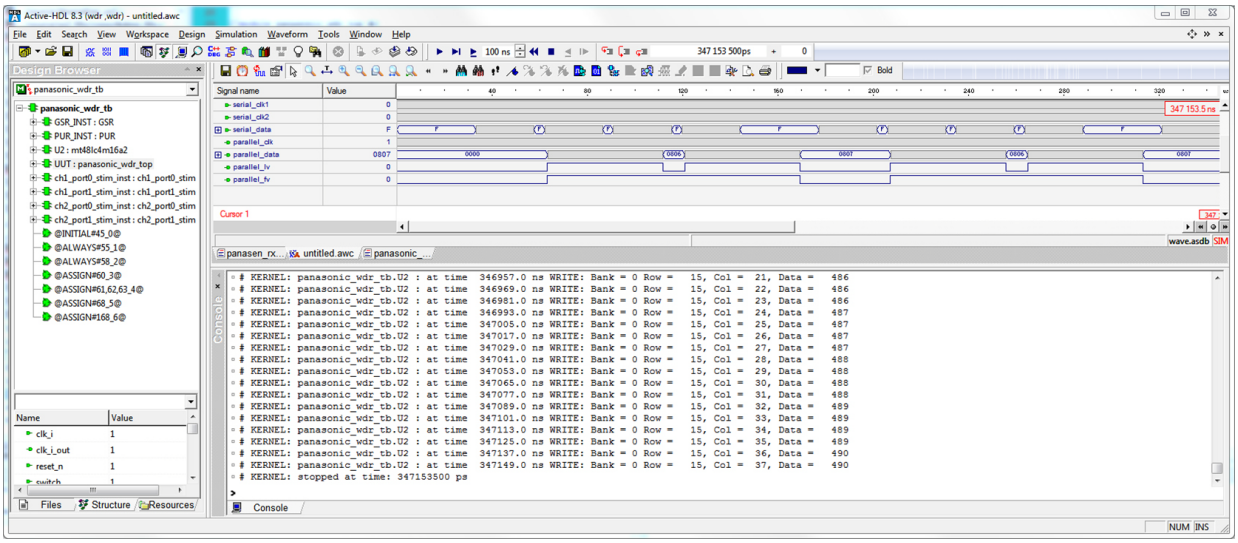
The complete functional design was simulated using Aldec Active-HDL. Design simulation can be accessed through the Lattice Diamond® design software by double-clicking the **wdr.spf** script file.

Figure 11. Simulation Script File Location in Lattice Diamond Software



Click **Finish** in the Simulation Wizard. This will open the Aldec Active-HDL simulator with the simulation project automatically. In Aldec Active-HDL, compile the design by going to **Design > Compile All**. Then start the simulation by going to **Simulation > Initialize Simulation**. A waveform viewer is available by clicking **File > New > Waveform**. Signals of interest can then be dragged into the waveform viewer.

Figure 12. Simulation Input and Output Results



Attached Register File

The WDR register file used to program the Panasonic MN34041 is included in the zipped reference design. It is called spi_WDR_x16.txt. This is intended to assist ISP firmware engineers with a known working sensor setting for WDR.

Table 3. Design Pinout

Signal Name	MachXO2-4000 132-Ball csBGA Ball Number	Reference Design Signal Name	Description
CLK_27MHz	C8	clk_i	27 MHz clock input
EXTCLK_FPGA	C2	clk_i_out	27 MHz clock output
SDOCAP	N6	serial_clk1	Clock A from image sensor
SDOCAN	P6		Clock A from image sensor
SDOCBP	M7	serial_clk2	Clock B from image sensor
SDOCBN	N8		Clock B from image sensor
SDODAP_0	M11	serial_data[0]	Data bus A from image sensor
SDODAN_0	P12		Data bus A from image sensor
SDODAP_1	P8	serial_data[1]	Data bus A from image sensor
SDODAN_1	M8		Data bus A from image sensor
SDODBP_0	M9	serial_data[2]	Data bus B from image sensor
SDODBN_0	N10		Data bus B from image sensor
SDODBP_1	N3	serial_data[3]	Data bus B from image sensor
SDODBN_1	P4		Data bus B from image sensor
RESET_TO_SENSOR	F2	sensor_rstn	Reset for Panasonic image sensor
PSV	C3	sensor_psv	Power save for image sensor
MSSEL	D1	mssel	Select pin on image sensor
RESET_BAR	C1	reset_n	Reset for MachXO2
PIXCLK	A11	parallel_clk	Pixel clock to ISP
FRAME_VALID	B7	parallel_fv	Frame Valid to ISP
LINE_VALID	C4	parallel_lv	Line Valid to ISP

Table 3. Design Pinout (Continued)

Signal Name	MachXO2-4000 132-Ball csBGA Ball Number	Reference Design Signal Name	Description
DOUT0	C6	parallel_data[11:0]	Data bus to ISP
DOUT1	B3	parallel_data[11:0]	Data bus to ISP
DOUT2	C11	parallel_data[11:0]	Data bus to ISP
DOUT3	A12	parallel_data[11:0]	Data bus to ISP
DOUT4	A7	parallel_data[11:0]	Data bus to ISP
DOUT5	B5	parallel_data[11:0]	Data bus to ISP
DOUT6	A9	parallel_data[11:0]	Data bus to ISP
DOUT7	A10	parallel_data[11:0]	Data bus to ISP
DOUT8	A2	parallel_data[11:0]	Data bus to ISP
DOUT9	B12	parallel_data[11:0]	Data bus to ISP
DOUT10	C12	parallel_data[11:0]	Data bus to ISP
DOUT11	B13	parallel_data[11:0]	Data bus to ISP
DOUT12 (Optional)	B9	parallel_data[12]	Optional data bit to ISP
DOUT13 (Optional)	A13	parallel_data[13]	Optional data bit to ISP
DOUT14 (Optional)	A3	parallel_data[14]	Optional data bit to ISP
DOUT15 (Optional)	C9	parallel_data[15]	Optional data bit to ISP
USB_TCK_2P5	B6	N/A	JTAG programming for MachXO2
USB_TDI_2P5	B4		
USB_TDO_2P5	A4		
USB_TMS_2P5	A6		
SDRAM_BA0	B14	sdr_BA[0]	LPSDRAM control
SDRAM_BA1	C13	sdr_BA[1]	
SDRAM_DQ0	C14	sdr_DQ[15:0]	LPSDRAM data bus
SDRAM_DQ1	D12		
SDRAM_DQ2	E12		
SDRAM_DQ3	E14		
SDRAM_DQ4	E13		
SDRAM_DQ5	F12		
SDRAM_DQ6	F13		
SDRAM_DQ7	F14		
SDRAM_DQ8	J13		
SDRAM_DQ9	K12		
SDRAM_DQ10	K13		
SDRAM_DQ11	K14		
SDRAM_DQ12	L14		
SDRAM_DQ13	M13		
SDRAM_DQ14	M12		
SDRAM_DQ15	M14		
SDRAM_WE_N	N13	sdr_WEn	LPSDRAM write enable
SDRAM_CS_N	N14	sdr_CSn	LPSDRAM chip select
SDRAM_CAS_N	G12	sdr_CASn	LPSDRAM CAS
SDRAM_RAS_N	G14	sdr_RASn	LPSDRAM RAS

Table 3. Design Pinout (Continued)

Signal Name	MachXO2-4000 132-Ball csBGA Ball Number	Reference Design Signal Name	Description
SDRAM_LDQM	G13	sdr_DQM[0]	LPSDRAM lower byte
SDRAM_UDQM	H12	sdr_DQM[1]	LPSDRAM upper byte
SDRAM_A0	J3	sdr_A[11:0]	LPSDRAM address bus
SDRAM_A1	K2		
SDRAM_A2	K1		
SDRAM_A3	K3		
SDRAM_A4	L3		
SDRAM_A5	M1		
SDRAM_A6	M2		
SDRAM_A7	F1		
SDRAM_A8	F3		
SDRAM_A9	H2		
SDRAM_A10	H1		
SDRAM_A11	H3		
SDRAM_CLK	J1	sdr_clk	LPSDRAM CLK
SDRAM_CKE	J2	sdr_CKE	LPSDRAM CLK enable

Note: LPSDRAM used is 4M x 16 bit, IS42VM16400K-6BLI.

Table 4. Resource Utilization

Device Family	Registers	LUTs	EBRs	PLLs
MachXO2	1729	2084	5	2

Table 5. I/O Timing Analysis of Sub-LVDS Serial Input Bus

Device Family	Setup	Hold	Units
MachXO2 (-6 Speed Grade)	243	158	ps

Table 6. Design Performance for MachXO2 (Speed Grade -6)

Clock Signal Name	Operating Frequency	Maximum Frequency	Units
serial_clk1	241.5	332.005	MHz
serial_clk2	241.5	332.005	MHz
clk_div2	121.5	162.417	MHz
pixel_clk	162	168.976	MHz
parallel_clk	81	130.174	MHz

Tested Designs

The Panasonic Image Sensor Bridge with WDR Preprocessor has been tested on the following hardware setups with components available for purchase through all major distributors:

- Complete Lattice Demonstration Platform
  - MN34041 Nanovesta Head Board – Part number: LF-PNV-ENV
  - MachXO2 Dual Sensor Interface Board – Part number: CLMXO2-4000HE-DSIB-EVN
  - HDR-60 Base Board – Part number: LFE3-70EAHDR60-DKN

References

- Target specifications – Area Sensor MN34041PL, Panasonic Corporation

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Revision History

Date	Version	Change Summary
October 2012	01.0	Initial release.