Capacitive Touch Sense Controller

October 2012 **Reference Design RD1136**

Introduction

Capacitive sensing is a technology based on capacitive coupling which takes human body capacitance as input. Capacitive touch sensors are used in many devices such as laptop trackpads, digital audio players, computer displays, mobile phones, mobile devices, tablets and more. Capacitive sensors are preferred for their versatility, reliability and robustness, unique human-device interface and cost reduction over mechanical switches.

The Capacitive Touch Sense Controller reference design demonstrates touch sensing and control using the iCE40™ FPGA. This design implements four touch sense buttons with outputs to LEDs.

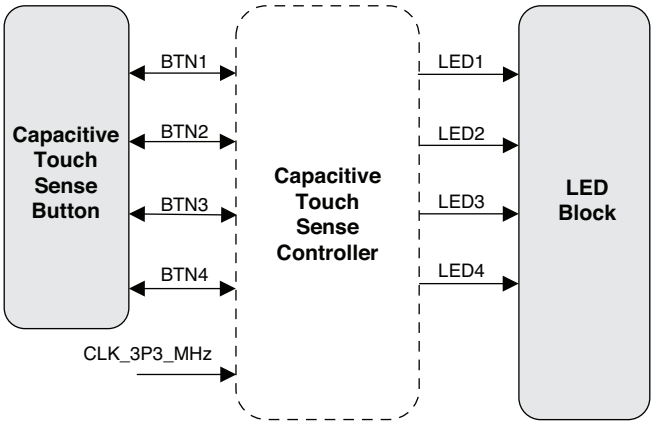
This reference design is implemented in Verilog. The Lattice iCEcube2™ Place and Route tool integrated with the Synplify Pro synthesis tool is used for implementation of the design. The design can also be targeted to other iCE40 family members.

Features

- Four capacitive touch sensitive user buttons
- Up to four LED toggle control outputs
- 3.3 MHz frequency operation
- Touch sensitive resolution up to 300ns

Functional Description

Figure 1. Block Diagram



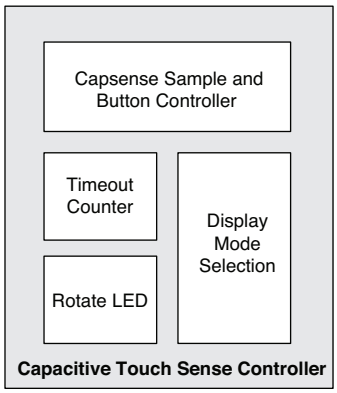
Signal Descriptions

Table 1. Signal Descriptions

Signal	Type	Description
BTN1	Bi-directional	Capacitive Touch Sense input
BTN2	Bi-directional	Capacitive Touch Sense input
BTN3	Bi-directional	Capacitive Touch Sense input
BTN4	Bi-directional	Capacitive Touch Sense input
LED1	Output	LED output
LED2	Output	LED output
LED3	Output	LED output
LED4	Output	LED output
CLK_3P3_MHZ	Input	Clock Input

Design Module

Figure 2. Design Module Block Diagram



The design module consists of the blocks shown in Figure 2 and described below.

Timeout Counter

When enabled, this block begins counting until the timeout interval period is reached. Once the timeout period is reached, it helps to trigger the scroll mode. If a touch occurs before the timeout, the counter is reset.

Display Mode Selection

This block sets the LED output display mode of operation depending on the timeout or a touch occurrence. When a timeout signal is asserted, the block selects the LED scroll mode. Otherwise, if buttons are pressed, toggle mode is selected.

Capsense Sample and Button Controller

This block constantly checks for a touch occurrence at any of the capacitive buttons. It controls the buttons by constantly sampling the button data to detect a touch input at any of the four buttons. This block drives the buttons to go to the high impedance state during the charging time for the Capsense capacitor. When a touch is sensed, the block sends signals to mode selection to toggle the respective LED.

Rotate LED

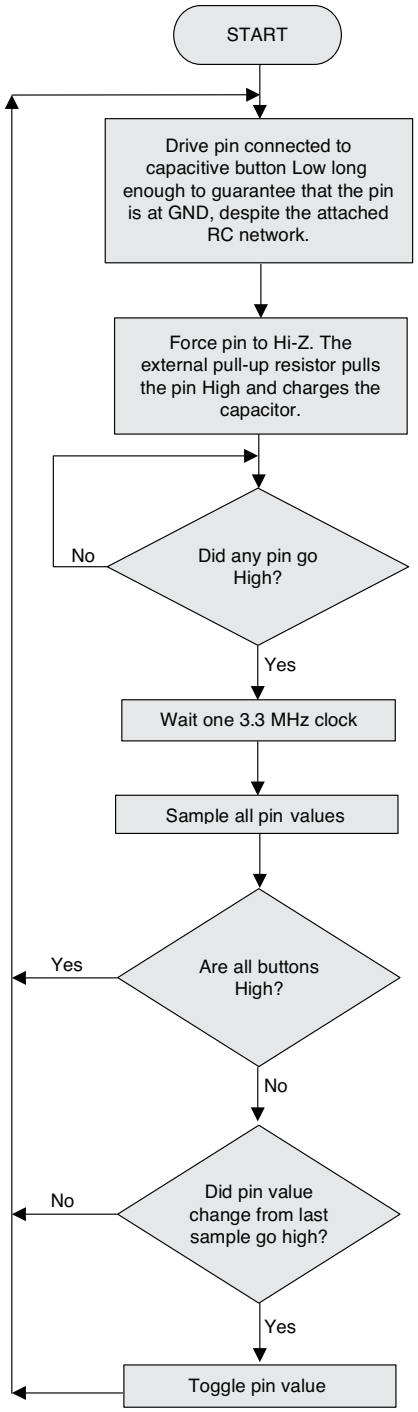
Once instantiated, this block rotates the LED blinking in scroll mode.

Operation

The design includes a set of four touch sensitive buttons that drive the signals to the FPGA input when a touch occurs. By default, the controller keeps the LED signals toggling in scroll-up mode until the touch interrupt occurs. The sample block constantly monitors for the occurrence of a touch at any button. Depending on the touch sequence and timing, the output LED control signal is toggled. The status block stores data on previous touch occurrences.

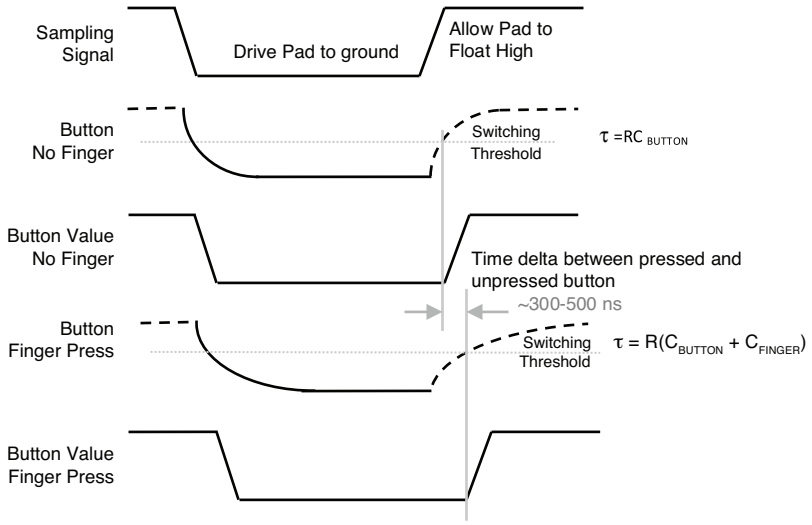
Figure 3 describes the capacitive touch button flow.

Figure 3. Capacitive Touch Button Flow Diagram



The sampling signal drives the voltage on the capacitive touch button to ground to bleed any residual charge. After a period of time, depending on the button sample frequency, the button is allowed to float High. Once the FPGA output goes to Hi-Z (high-impedance, floating, tri-state), the pull-up resistor charges the capacitor of the touch button. After about an RC time constant (tau), the voltage on the pad exceeds the input switching threshold of the FPGA. A finger pressed against the capacitive touch button adds about another 5 pF of capacitance, increasing the RC constant and delaying the Low-to-High transition for a pressed button.

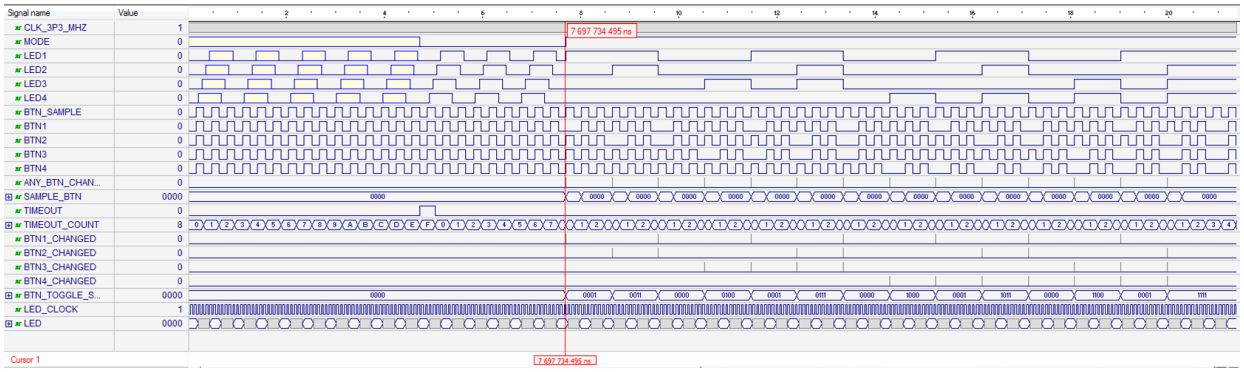
Figure 4. Capacitive Touch Timing Example



The switching time difference between an unpressed and one or more pressed buttons is roughly 300 to 500ns. Using the 3.33 MHz input, this amounts to a one clock delay difference between an unpressed and pressed buttons. The design detects simultaneous button presses on up to three of the capacitive touch buttons. Pressing all four buttons is the same as pressing no buttons.

Simulation Waveforms

Figure 5. Simulation Waveforms



Implementation

This design is implemented in Verilog. When using this design in a different device, density, speed or grade, performance and utilization may vary.

Table 2. Performance and Resource Utilization

Device Family	Language	Utilization (LUTs)	f_{MAX} (MHz)	I/Os	Architectual Resources
iCE40[1]	Verilog	83	>170	9	N/A

1. Performance utilization characteristics are generated using iCE-40LP1K-CM121 with iCEcube2 design software.

References

- iCE40 Family Handbook

Technical Support Assistance

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Revision History

Date	Version	Change Summary
October 2012	01.0	Initial release.