SPI-to-UART Expander

September 2012 Reference Design RD1143

Introduction

SPI and UART are among the most commonly-used protocols in today's embedded applications. Often, there is a requirement to expand a single SPI master to several UART interfaces or to have a bridge between SPI and UART interfaces due to peripheral limitations in processors interacting with each other. The SPI-to-UART Expander provides a cost-effective solution for communicating from a host processor's SPI bus to multiple UART devices. This reference design acts as a SPI port expander, multiplexing and demultiplexing read/write data through the SPI slave to multiple UARTs using iCE40™ FPGAs.

Functional Description

The SPI-to-UART Expander interfaces the host processor/microcontroller's SPI master to a number of UARTs through a SPI slave. This interface consists of two modules:

- SPI slave which interfaces with the SPI master in the host processor and acts as a port expander
- Multiplexer/Demultiplexer to write/read data from UARTs. This interface module selects the appropriate UART device based on address and mode bits on the MOSI frame and performs the following operations
  - Writes the configuration register and configures baud rate, data length, enables/disables parity and parity type (even/odd)
  - Writes data to the UART write register/FIFO
  - Reads data from the UART status register
  - Reads data from the UART's read FIFO. This data is communicated to host processor through the MISO line. The SPI slave operates in CPOL = 0 and CPHA = 0 mode, MSB first read/write and is configured for a 16-bit SPI data frame.

Figure 1. SPI-UART Interface

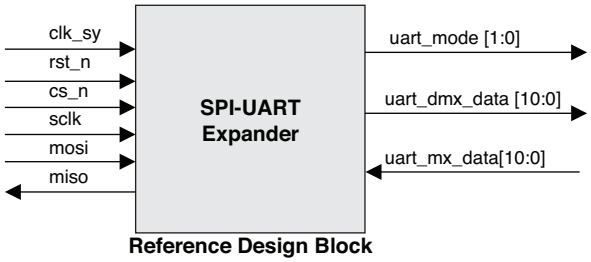


Figure 2. Block Diagram (UART_nums-1)

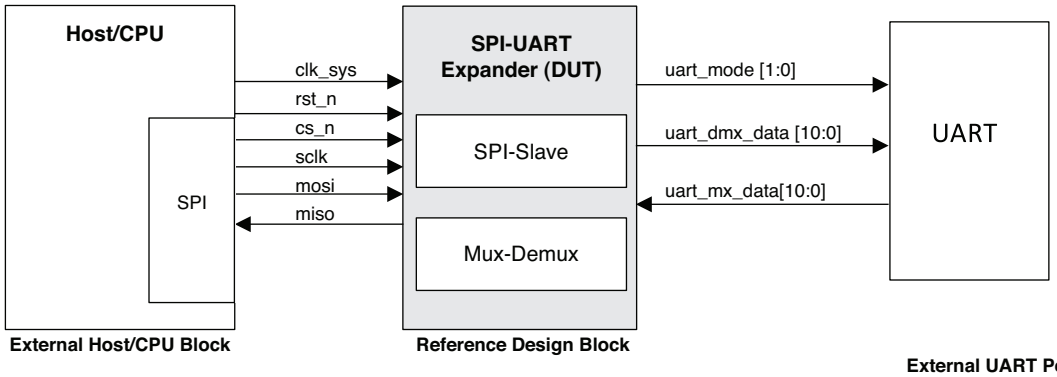
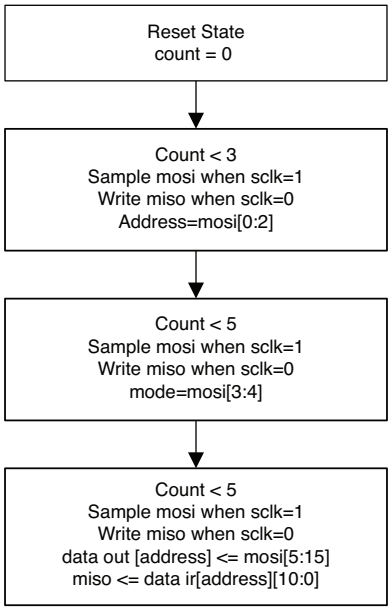


Figure 3. Simplified State Machine Flow Diagram



Figures 1 and 2 show the simplified block diagram of the SPI-to-UART Expander and simplified state diagram. SPI-to-UART expansion and interface is achieved in the iCE40 FPGA by decoding the appropriate bits in the SPI's MOSI data frame to obtain the address of the UART port the slave has to expand to. Once this address is decoded in the slave, the serial data that the master sends to the slave on its MOSI line detects the mode of operation of the UART, such as read data, read status, write data and write configuration. At the same time, the serial input data that the slave received on a selected input UART is routed on to the MISO line based on the bit address in the SPI master's MOSI data frame. This port expander is designed for a 16-bit SPI frame, with the MSB being sent first. The first three bits of the 16-bit MOSI frame signify the address of the UART to be expanded into. The next two bits signify the mode of the UART as follows:

- When '00' and cs_n = '0' then reads the UART status register
- When '01' and cs_n = '0' then reads the UART data register/FIFO
- When '10' and cs_n = '0' then writes the UART data register/FIFO
- When '11' and cs_n = '0' then writes the UART configuration register

The remaining eight bits in the MOSI frame contain the data byte to be written to the slave's output UART device. The first five bits on the MISO data frame are insignificant and are ignored. The following 11 bits contain the input data byte that the slave received on a selected UART port. The data format of the SPI's 16-bit word and the significance of its bit positions are indicated in Figure 3.

Table 1. I/O Interface Description

Pin	Direction	I/O Bank	Voltage (V)	Description
clk_sys	Input	0/1/2/3	1.8/2.5/3.3	System clock
rst_n	Input	0/1/2/3	1.8/2.5/3.3	Active low system reset
cs_n	Input	0/1/2/3	1.8/2.5/3.3	Active low chip select
sclk	Input	0/1/2/3	1.8/2.5/3.3	SPI serial clock
mosi	Input	0/1/2/3	1.8/2.5/3.3	Master Out Slave In, data line from SPI master
miso	Output	0/1/2/3	1.8/2.5/3.3	Master In Slave Out, data line from SPI slave (this interface)
uart_mode[1:0]	Output	0/1/2/3	1.8/2.5/3.3	Mode selection signals per UART
uart_dmx_data [10:0]	Output	0/1/2/3	1.8/2.5/3.3	Read data/status lines per UART
uart_mx_ data[10:0]	Input	0/1/2/3	1.8/2.5/3.3	Write configuration/data lines per UART

Figure 4. Data Format of a SPI 16-Bit Word

MOSI Frame – Config Write (M1M0:11)

DIN 15	DIN 14	DIN 13	DIN 12	DIN 11	DIN 10	DIN 9	DIN 8	DIN 7	DIN 6	DIN 5	DIN 4	DIN 3	DIN 2	DIN 1	DIN 0
A2	A1	A0	M1	M0	X	X	X	X	PT	PE	L1	L0	B2	B1	B0

MOSI Frame – Data Write (M1M0:10)

DIN 15	DIN 14	DIN 13	DIN 12	DIN 11	DIN 10	DIN 9	DIN 8	DIN 7	DIN 6	DIN 5	DIN 4	DIN 3	DIN 2	DIN 1	DIN 0
A2	A1	A0	M1	M0	X	X	X	D7	D6	D5	D4	D3	D2	D1	D0

MISO Frame – Data Read (M1M0:00)

DO 15	DO 14	DO 13	DO 12	DO 11	DO 10	DO9	DO8	DO7	DO6	DO5	DO4	DO3	DO2	DO1	DO0
X	X	X	X	X	X	PER	BER	D7	D6	D5	D4	D3	D2	D1	D0

MISO Frame – Status Read (M1M0:01)

DO 15	DO 14	DO 13	DO 12	DO 11	DO 10	DO9	DO8	DO7	D O6	DO5	DO4	DO3	DO2	DO1	DO0
X	X	X	X	X	CTS	RTS	RXBSY	TXBSY	PER	BER	WFULL	RFULL	PE	L1	L0

Testbench Description

Figure 5. Testbench Architecture(UART_nums-7)

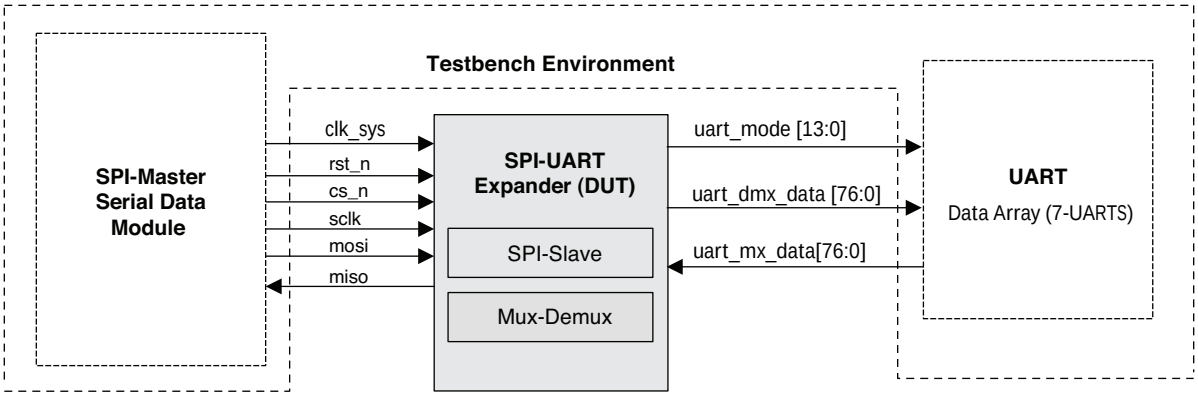


Figure 6. Simulation Timing Waveforms Showing Read (MISO-uart_dmx_data) and Write (MOSI-uart_mx_data) Operations

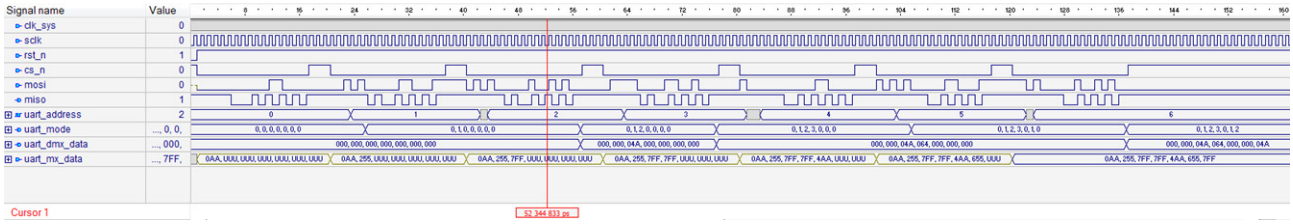


Figure 7. Simulation Timing Waveforms Showing UART Address Bits "uart_address [2:0]" Read with Active Low "cs_n"

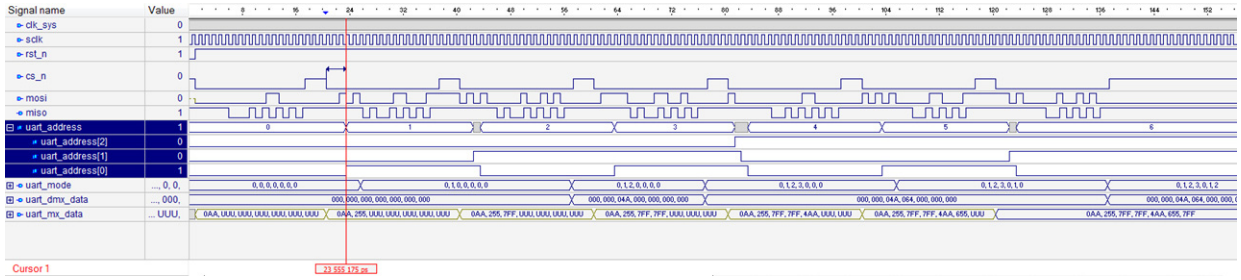


Figure 8. Simulation Timing Waveforms Showing UART Mode Bits "uart_mode [4:3]" After the uart_address Bits for the "UART Device" Corresponding to the Address uart_address [2:0]

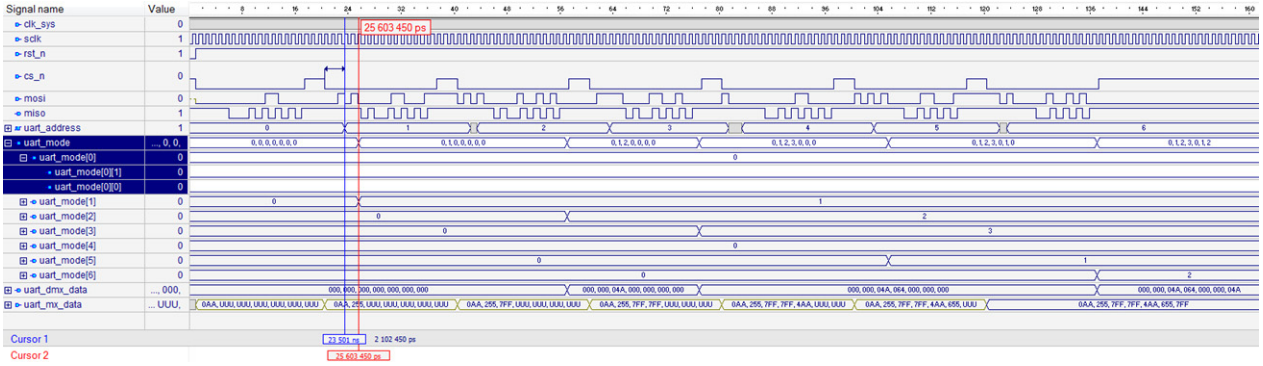


Figure 9. Simulation Timing Waveforms Showing UART-MOSI Mode-10 Data Write Operation with "uart_dmx_data" for the UART Device that Corresponds to the Address uart_address [2:0]

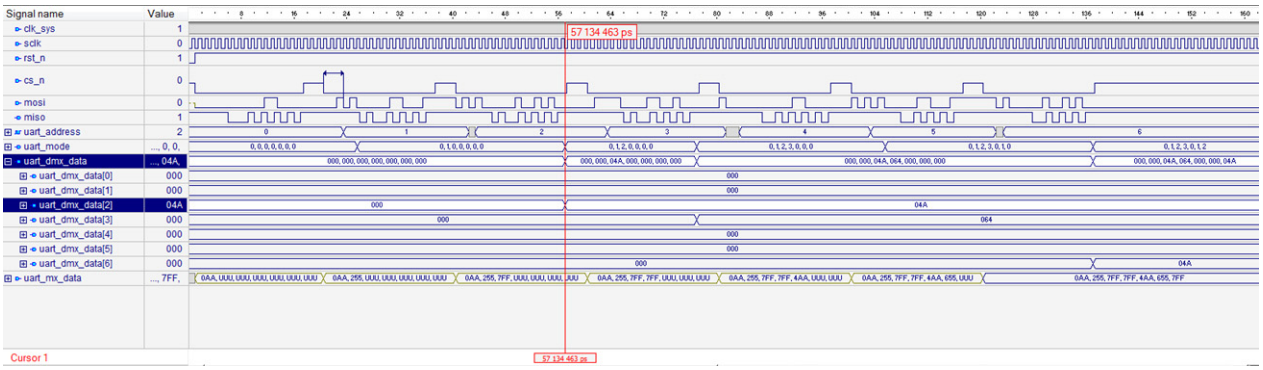
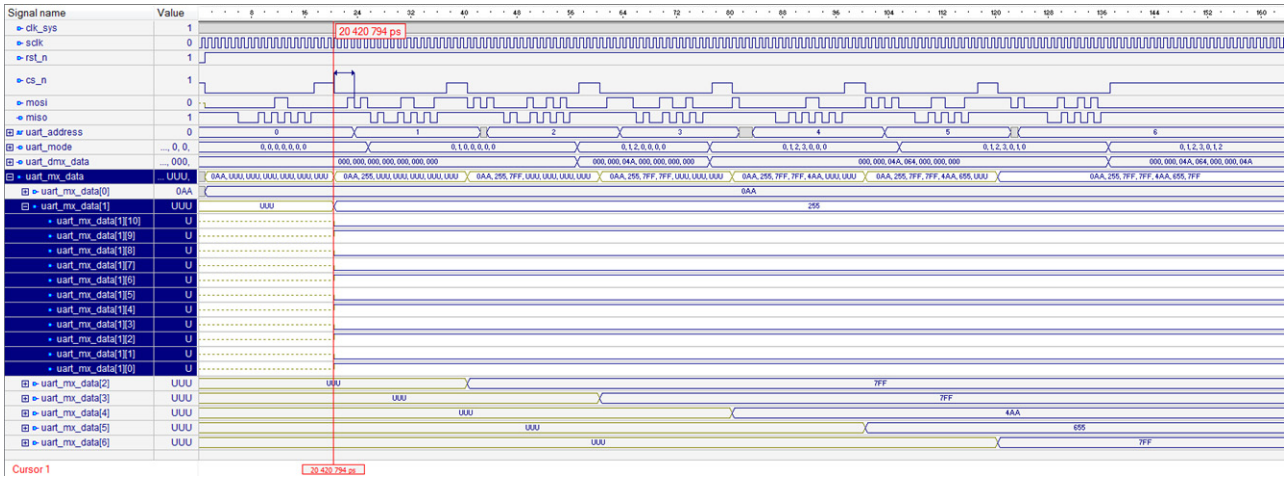


Figure 10. Simulation Timing Waveforms Showing UART-MISO Mode-00 Data Read Operation with "uart_mx_data" for the UART Device that Corresponds to the Address uart_address [2:0]



Implementation

This design is implemented in VHDL. When using the design in a different device, density, speed, or grade, performance and utilization may vary. Default settings are used during the fitting of the design.

Table 2. Performance and Resource Utilization

Family	Language	Utilization	f_{MAX} (MHz)	I/Os	Architecture Resources
iCE40	VHDL	245 LUTs	755.28	172	PLB

1. Performance and utilization characteristics are generated using iCE40HX8K-CT256 with iCEcube2™ design software.

Technical Support Assistance

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Revision History

Date	Version	Change Summary
September 2012	01.0	Initial release.