SPI Slave Controller

October 2012 Reference Design RD1142

Introduction

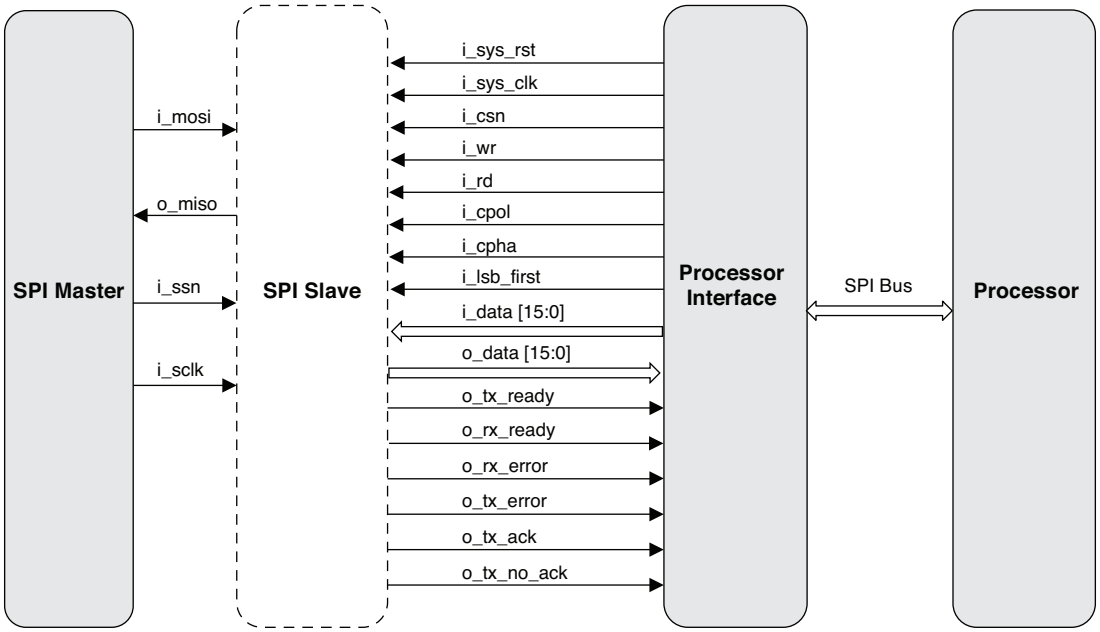
The Serial Peripheral Interface (SPI) is used primarily for synchronous serial communication between a host processor and its peripherals. The SPI bus is often selected because of its low pin count and full-duplex mode that can achieve data throughput in the tens of Mbps range. The SPI bus uses a 4-wire interface with two unidirectional data lines to communicate between the master and the selected slave. It supports one master with multiple slaves on one bus and allows protocol flexibility for the bit transferred.

This reference design implements a SPI slave device interface that provides full-duplex, synchronous, serial communication with the SPI master. The data size of the SPI bus can be configured to either 16 or 8 bits. The SPI Slave Controller reference design supports all modes of CPOL and CPHA – 00, 01, 10 and 11.

This design uses three pins (clock, data in and data out) plus one select for each slave device. A SPI is a good choice for communicating with low-speed devices that are accessed intermittently and transfer data streams rather than reading and writing to specific addresses. A SPI is an especially good choice if we can take advantage of its full-duplex capability for sending and receiving data at the same time.

This design is implemented in VHDL. The Lattice iCECube2™ Place and Route tool integrated with Synplify Pro synthesis tool is used for the implementation of the design. The design uses an iCE40™ ultra low density FPGA and can be targeted to other iCE40 family members.

Figure 1. Block Diagram

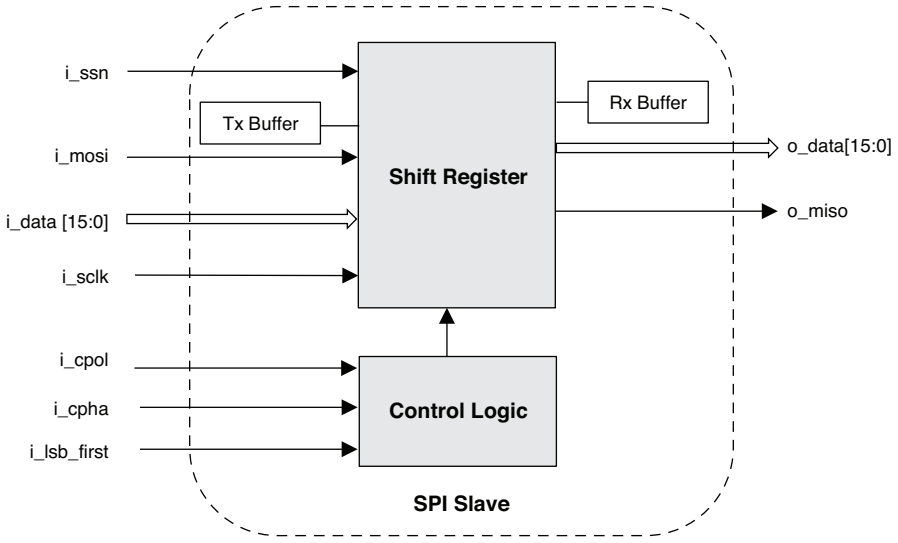


Features

- Supports all four modes of CPOL and CPHA operation (00/01/10/11)
- Supports variable data widths (8 and 16 bits)
- Provision for easy integration of any processor interface
- IP-XACT version 1.2 compliant

Functional Description

Figure 2. Functional Block Diagram



SPI Slave Receiver

MOSI sampling – SPI slave receives the data on the MOSI line based on CPOL and CPHA modes as follows:

Sample at positive edge of SCLK for:

- i_cpol = ‘0’ and i_cpha = ‘0’
- i_cpol = ‘1’ and i_cpha = ‘1’

Sample at negative edge of SCLK for:

- i_cpol = ‘1’ and i_cpha = ‘0’
- i_cpol = ‘0’ and i_cpha = ‘1’

After the data is received, rx_ready goes high and valid received data is available on the bus. If new data has arrived and the last data received has not yet been read, then the rx_error signal goes high to indicate a receive error.

SPI Slave Transmitter

Sending data on the MISO line – The SPI slave transmits the data on the MISO line from a shift register based on CPOL and CPHA as follows:

- CPOL = 0 and CPHA = 0: Data is placed before the rising edge of sclk
- CPOL = 1 and CPHA = 0: Data is placed before the falling edge of sclk
- CPOL = 0 and CPHA = 1: Data is placed at the rising edge of sclk
- CPOL = 1 and CPHA = 1: Data is placed at the falling edge of sclk

At the end of data transmission, the tx_ready signal goes high. When the transmitter is busy transmitting a data stream, the tx_error signal goes high if the transmit buffer data is over-written by the processor interface.

Clock Requirements

For proper operation of the SPI slave, the system frequency should be twice that of the SCL frequency at a minimum.

Signal Descriptions

Table 1. Signal Descriptions

Signal	Width	Type	Description
i_csn	1	Input	Active low chip select
i_data	16	Input	Input data from the processor interface
i_wr	1	Input	Active low write enable
i_rd	1	Input	Active high read enable
o_data	16	Output	Output data to processor interface.
o_tx_ready	1	Output	Transmitter ready status – High indicates the transmitter is ready to send additional data
o_rx_ready	1	Output	Receiver ready – High indicates the receiver is ready to receive additional data
o_tx_error	1	Output	Indicates error in transmission of data
o_rx_error	1	Output	Indicates error in reception of data
i_cpol	1	Input	Polarity of the clock
i_cpha	1	Input	Phase of the clock
i_lsb_first	1	Input	LSB sent first when ‘1’. MSB goes first when ‘0’.
o_miso	1	Output	Slave output to master
i_mosi	1	Input	Slave input from master
i_ssn	1	Input	Slave select from master
i_sclk	1	Input	Serial clock from master
i_sys_rst	1	Input	Asynchronous active low reset
i_sys_clk	1	Input	System clock
o_tx_ack	1	Output	Transmission acknowledged from slave
o_tx_no_ack	1	Output	Transmission not acknowledged from slave

Initialization Conditions

An asynchronous active low reset signal assertion is necessary to initialize the SPI slave to the proper operating state. Receive and transmit buffers are initialized to zero during the reset condition.

Configurable Parameters

DATA_SIZE – This parameter configures the data width of the SPI transaction. It can take either of two values: 16 (the default value) or 8.

Operation Sequence

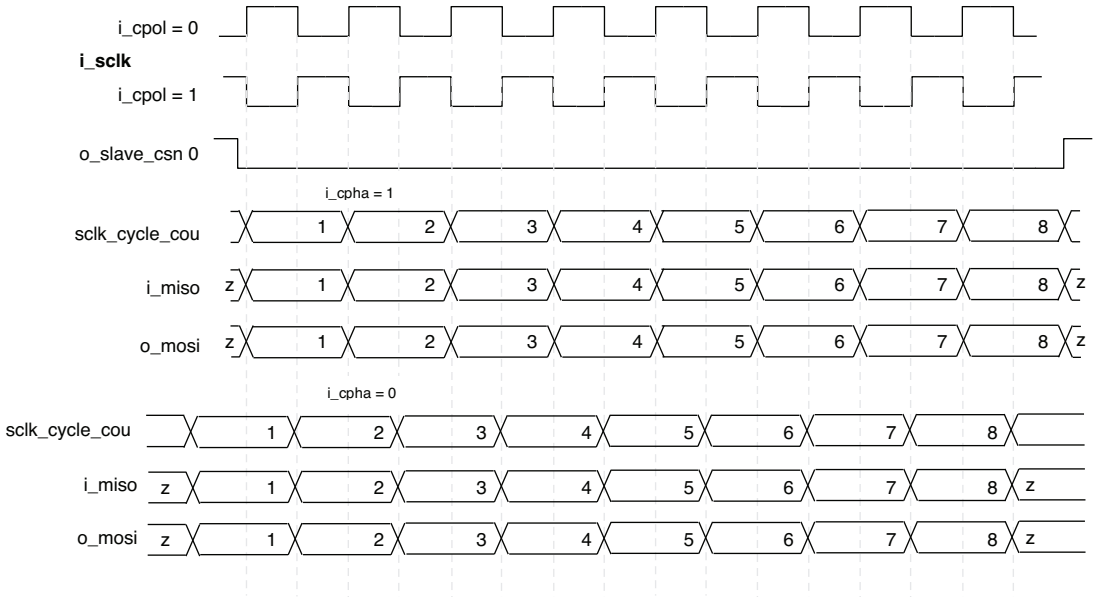
1. Write a data slave, set up CPOL, CPHA and LSB/MSB first mode.
2. Enable the SPI slave by making i_ssn = 0.
3. Generate the SCL depending upon CPOL and CPHA.
4. Receive the data from the i_data line to the MOSI line depending upon CPOL, CPHA and LSB/MSB.
5. Similarly, drive the MISO line depending upon CPOL, CPHA and LSB/MSB.
6. Repeat steps 1, 2, 3, 4 and 5 for four different sets of CPOL, CPHA and LSB/MSB first modes and input the data pattern to the slave.

Timing Diagram

Signal definitions:

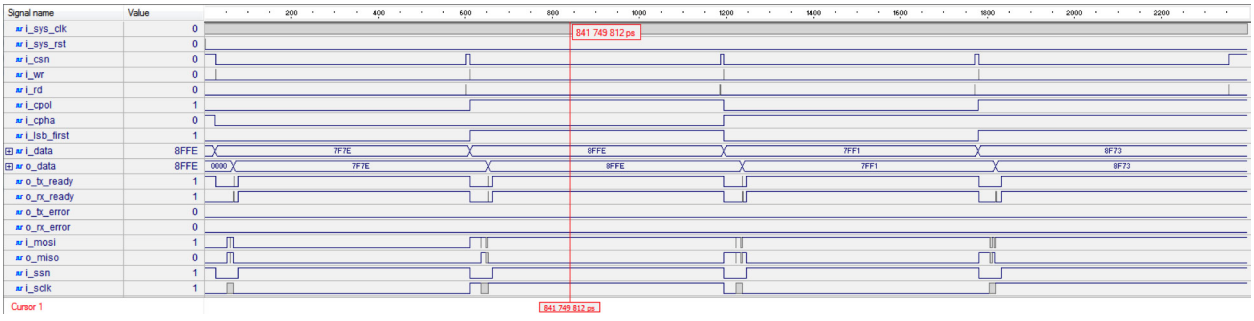
- i_sclk – Serial clock line (Generated by master)
- i_cpol – Clock polarity
- i_cpha – Clock phase
- i_ssn – Slave select
- o_miso – Output from the SPI slave
- i_mosi – Input to the SPI slave

Figure 3. Timing Diagram



Simulation Waveforms

Figure 4. Simulation Waveforms



Implementation

This design is implemented in VHDL. When using this design in a different device, density, speed or grade, performance and utilization may vary.

Table 2. Performance and Resource Utilization

Family	Language	Utilization (LUTs)	f_{MAX} (MHz)	I/Os	Architecture Resources
iCE40[1]	VHDL	217	254	48	N/A

1. Performance and utilization characteristics are generated using iCE-40LP1K-CM121 with iCEcube2 design software.

References

- iCE40 Family Handbook

Technical Support Assistance

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Revision History

Date	Version	Change Summary
October 2012	01.0	Initial release.