Touch Screen Controller

September 2012 **Reference Design RD1137**

Introduction

A touch screen is a display that can detect the location of touches within the display area. This reference design demonstrates the use of the iCE40™ ultra low density FPGA as a Touch Screen Controller for use with low power handheld devices. The design includes an asynchronous processor interface, and is implemented in VHDL. The Lattice iCEcube2™ Place and Route tool integrated with the Synplify Pro synthesis tool is used for implementation of the design. The design can also be targeted to other iCE40 family members.

Features

- Compatible with digitizer chip (TSC2046)
- Touch de-bounce logic
- 16x32 touch screen resolution
- Interrupt generation logic

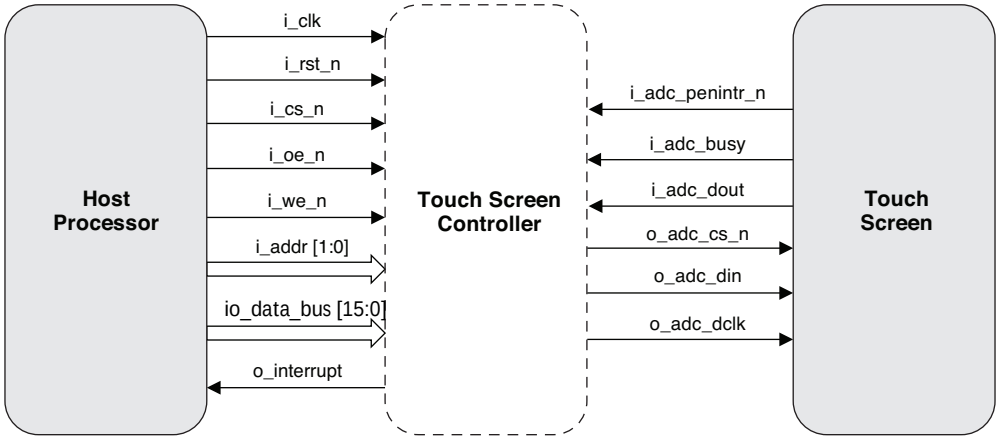
Features not supported:

- Power save mode support
- Configurable resolution
- Configurable for digitizer chips with SPI or I^2C interfaces

Functional Description

Figure 1 shows the system interface of the Touch Screen Controller reference design.

Figure 1. System Block Diagram



Signal Descriptions

Table 1. Signal Descriptions

Signal	Width	Type	Description
i_clk	1	Input	System clock operating at 32 MHz
i_rst_n	1	Input	Active low asynchronous reset
i_adc_penintr_n	1	Input	Touch screen pen interrupt
i_adc_busy	1	Input	Touch screen busy
o_adc_cs_n	1	Output	Touch screen chip select
o_adc_dclk	1	Output	Touch screen dot clock
i_adc_dout	1	Input	Touch screen serial data out
o_adc_din	1	Output	Touch screen serial data in
o_interrupt	1	Output	Interrupt signal to host processor
io_data_bus[15:0]	16	Inout	Bidirectional processor data bus
i_cs_n	1	Input	Chip select
i_oe_n	1	Input	Output enable
i_we_n	1	Input	Write enable
i_addr[1:0]	2	Input	Address lines to access internal registers

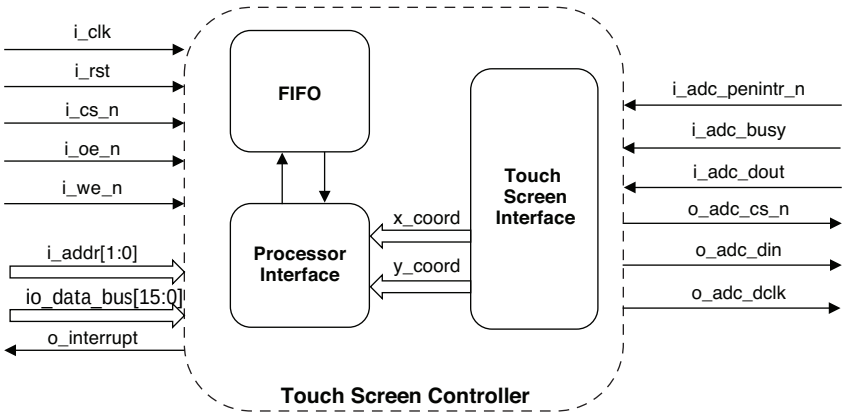
Table 2. Internal Register Set

Name	Address	Width	Access
Valid Data Register	0x01	16	R
FIFO Status Register	0x02	16	R

Design Module Description

Figure 2 shows the functional block diagram of this design. The design has three main modules as shown in Figure 2.

Figure 2. Functional Block Diagram



Touch Screen Interface

The Touch Screen Controller waits on the input signal, i_adc_penintr_n, to go low which indicates that a touch has taken place. The interface logic then waits for the de-bounce time and starts to sample the x-coordinate and y-coordinate data. This data is passed on to the processor interface for storage.

Processor Interface

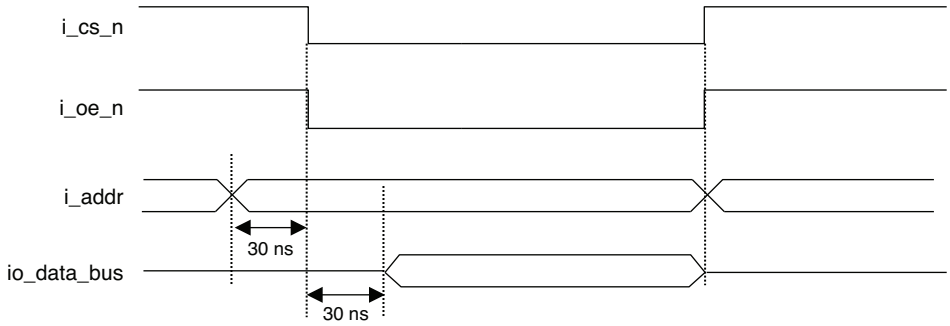
The following signals are used for transactions between the host processor and the touch screen interface: i_cs_n, i_oe_n, i_we_n, i_addr and io_data_bus. For all transactions to be valid, the i_cs must be held low. Since the internal registers of this interface are read only, only the i_oe_n signal is used and the i_we_n is provided for future enhancements. The control signal for the read operation is the output enable signal i_oe_n. The host processor can use this signal with the chip select line i_cs_n to read either the touch data within the RAM or the status of the FIFO. As long as valid touch data is available within the RAM an interrupt is generated by the Touch Screen Interface Module. The interrupt is de-asserted once all the valid data had been read from the RAM. The touch data received by the processor interface block from the Touch Screen Interface Block is stored in the FIFO.

FIFO

The FIFO is provided to store the processed touch data. The depth of this FIFO is 128 words and can store 16 bit of data at each word.

Timing Diagram

Figure 3. Timing Diagram for the Register Read Operation



HDL Simulation

Figure 4. Simulation Timing Diagram

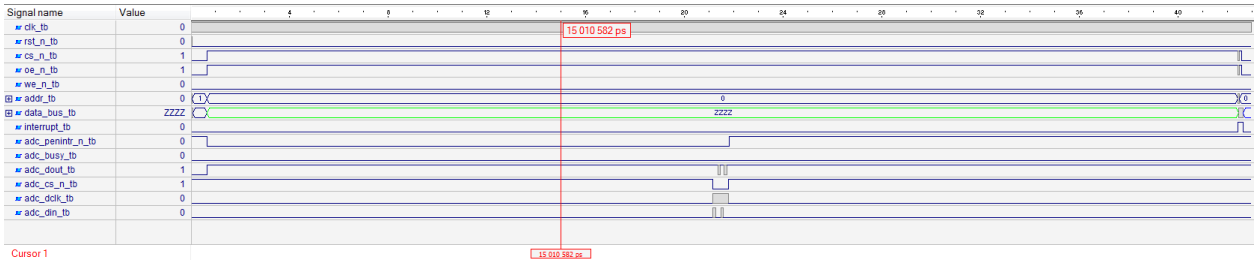
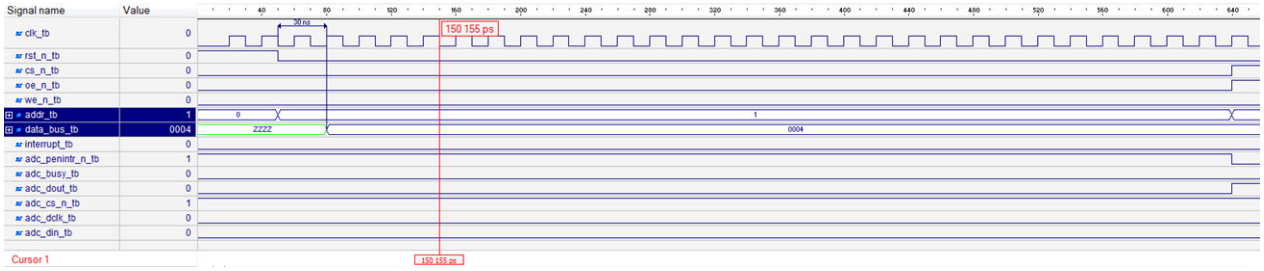


Figure 5. Simulation Diagram Showing the Register Read Operation from the Specified Address



Implementation

This design is implemented in VHDL. When using this design in a different device, density, speed or grade, performance and utilization may vary.

Table 3. Performance and Resource Utilization

Family	Language	Utilization (LUTs)	f_{MAX} (MHz)	I/Os	Architecture Resources
iCE40[1]	VHDL	170	120	28	N/A

1. Performance and utilization characteristics are generated using iCE40LP1K-CM121 with iCEcube2 design software.

References

- iCE40 Family Handbook

Technical Support Assistance

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Revision History

Date	Version	Change Summary
September 2012	01.0	Initial release.