IrDA Fast Receiver

October 2012 Reference Design RD1134

Introduction

The Infrared Data Association (IrDA) maintains an interoperable, low cost, low power, half-duplex serial data interconnection standard that supports a walk-up, point-to-point user model that is adaptable to a wide range of appliances and devices. Infrared (IR) technologies are best suited for short distance, low-to-medium data throughput and wireless communication channels.

This document provides a brief description of an IrDA Fast Receiver and its implementation.

This reference design is implemented in VHDL. The Lattice iCEcube2™ Place and Route tool integrated with the Synplify Pro synthesis tool is used for implementation of the design. The design uses an iCE40™ ultra low density FPGA and can be targeted to other iCE40 family members.

Features

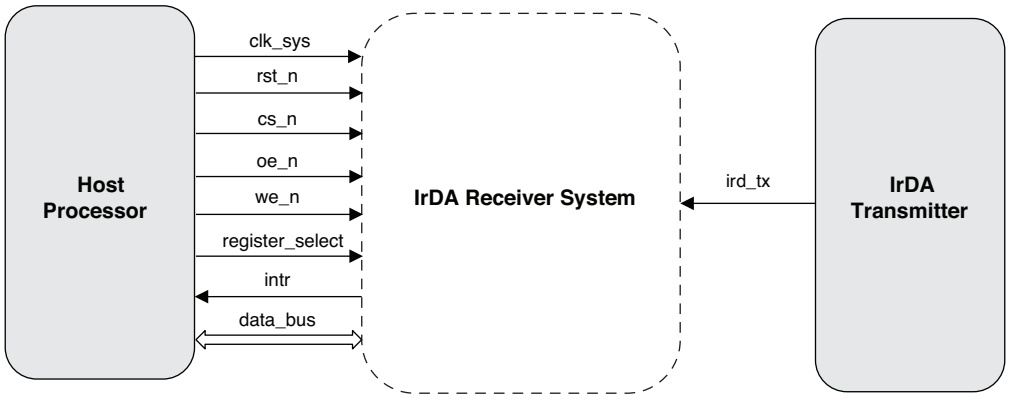
- 4 Mbps baud rate
- Complete 4PPM packet support – Preamble, STA, Data, STO fields
- Synchronous parallel processor interface
- 32x32-bit read and write data FIFOs
- Interrupt on completion of data receipt
- IEEE 802 32-bit Cyclic Redundancy Check (CRC-32) generation and detection

Features not supported:

- Configurable baud rate
- Host UART interface
- Not hardware tested

Functional Description

Figure 1. Block Diagram



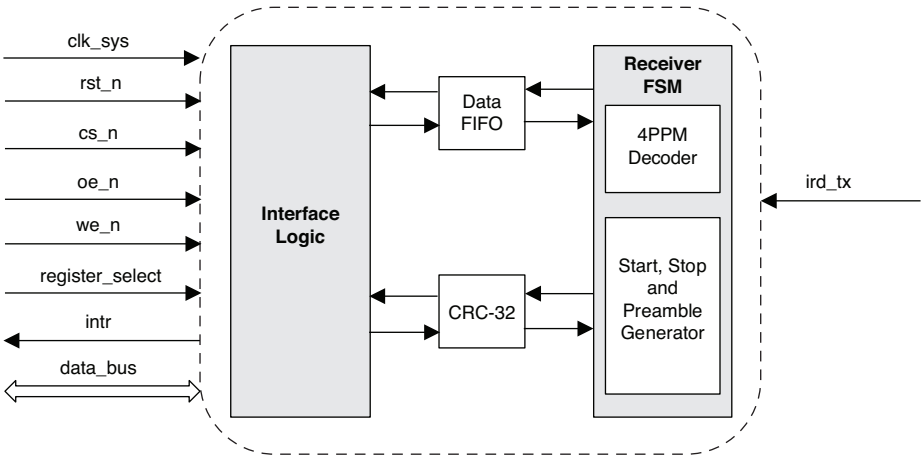
Signal Descriptions

Table 1. Signal Description

Signal	Width	Direction	Description
cs_n	1	Input	Active low chip select
oe_n	1	Input	Active low output enable
we_n	1	Input	Active low write enable
register_select	2	Input	Register selection bus to select registers from – control register, status register
intr	1	Output	IrDA Receiver interrupt
data_bus	32	Input	Processor data bus (bi-directional)
irda_tx	1	Input	IR device data input
rst_n	1	Input	Asynchronous active low reset – This signal is used to initialize the internal state machine to a known state
clk_sys	1	Input	System clock

Module Descriptions

Figure 2. Functional Block Diagram



The IrDA defines a set of specifications, or protocol stack, that provides for the establishment and maintenance of a link so that error-free communication is possible.

The IrDA standards include three mandatory specifications: the Physical Layer, Link Access Protocol (IrLAP), and Link Management Protocol (IrLMP). Beginning with version 1.1 of the IrDA Physical Layer specification, a 4 Mbps data rate is supported.

The Fast Infrared (FIR, 4 Mbps) scheme uses the four pulse position modulation (4PPM) scheme, where one complete symbol is represented by four equal-time slices called “chips”. In FIR, every chip has 125 ns duration, and every symbol represents two bits of data. Because there are four unique chip positions within each symbol in 4PPM, four independent symbols exist in which only one chip is a logic ‘1’ while all other chips are a logic ‘0’. These four unique symbols are the only legal data symbols (DD) allowed in 4PPM. Each DD represents two bits of payload data, or a single data bit pair (DBP), so that a byte of payload data can be represented by four DDs in sequence.

In IrDA FIR mode, a special packet format is used for data transfer. The packet format is divided into four blocks as shown in Table 2.

Table 2. IrDA Data Format

PA	STA	DD along with CRC-32	STO

- **PA** – Preamble consists of exactly 16 repeated transmissions of the following symbols: 1000 0000 1010 1000.
- **STA** – Start sequence. Occurs only once and includes the following symbols: 0000 0011 0000 0011 0110 0000 0110 0000. After the preamble, the receiver looks for the STA sequence for synchronization.
- **DD** – Actual data encoded in the 4 PPM scheme along with CRC-32 bit. After the start sequence, the transmitter transmits the data in encoded form along with CRC-32 to facilitate error detection at the receiver end. CRC(x) = $x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$. The data is decoded only after the STA flag is raised.
- **STO** – The stop sequence occurs only once and includes the sequence 0000 0011 0000 0011 0000 0110 0000 0110, indicating the end of a data frame.

The IrDA Fast Receiver uses two-bit address select signals for programming control registers, reading/writing data and reading the status register. Table 2 lists the address mapping of the receiver. These register addresses, along with the active low output enable (oe_n) and write enable (we_n), configure the read/write mode for the register addressed.

Figure 3. FIR (4 PPM) Modulation/Demodulation Schemes

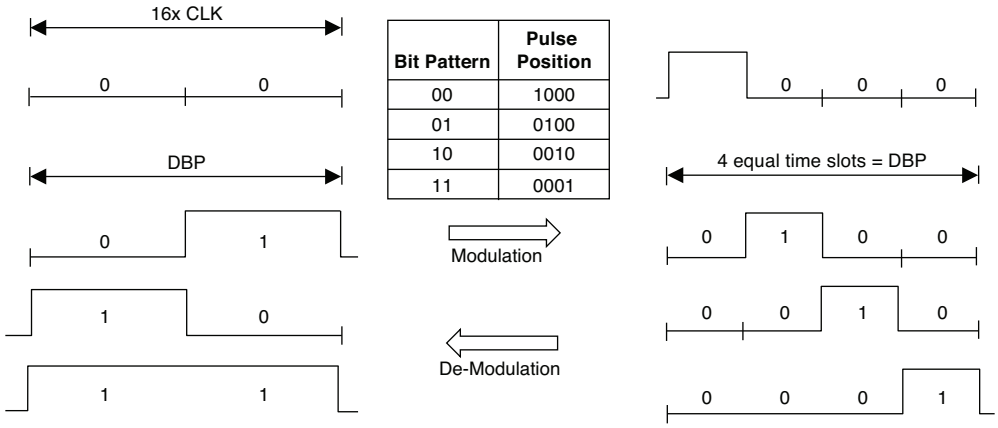


Table 3. Internal Register List

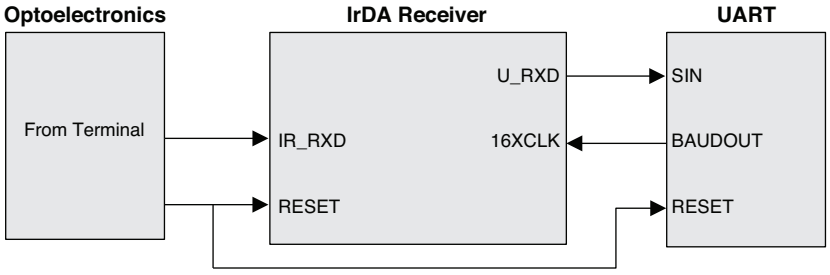
Register	Address	Width (Bits)	Access
Configuration register	0x01	32	R/W
Read (Rx) data FIFO register	0x02	32	R
Status register	0x03	32	R

Table 4. Internal Register Bit Descriptions

Internal Register	Bit #	Access	Description
Configuration Register (0x01)	31:12	RW	Unimplemented
	11	RW	Clears the interrupts
	10	RW	Enables the interrupts
	9	RW	Clears the read/write FIFO
	8:5	RW	Unimplemented
	4:0	RW	Block length of the data transaction
Read (Rx) Data FIFO Register (0x02)	31:0	R	Receiver FIFO read data
Status Register (0x03)	32:8	R	Unimplemented
	7	R	Preamble Error
	6	R	Start Error
	5	R	Stop Error
	4	R	CRC Error
	3	R	'1' indicates read FIFO full
	2	R	'1' indicates read FIFO half full
	1	R	'1' indicates read FIFO empty
	0	R	'1' indicates receiver is busy

Operation Sequence

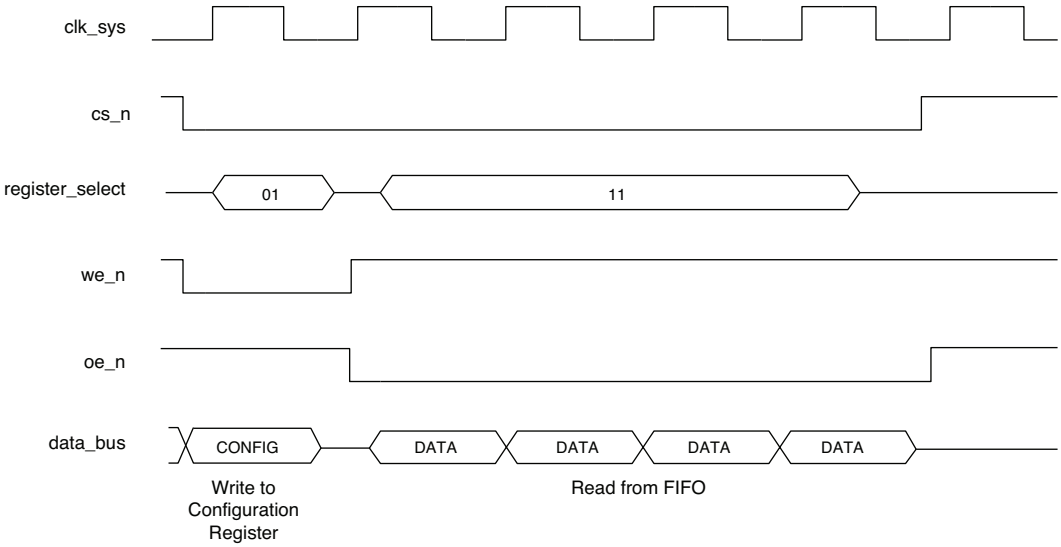
Figure 4. Operational Blocks



1. The receiver is operational when reset = '1'.
2. Write to the receiver configuration register by selecting address = '01'. Make the 10th bit = '1' to enable the interrupt. In this case, the block length is 16 data words.
   Sample input: "00000000000000000000010000010000" is given at data_bus
3. Write the data to be transmitted to the irda_tx line bit by bit. Give X"78000000", X"78787800" …. (16 data words) to the ird_tx line bit by bit.

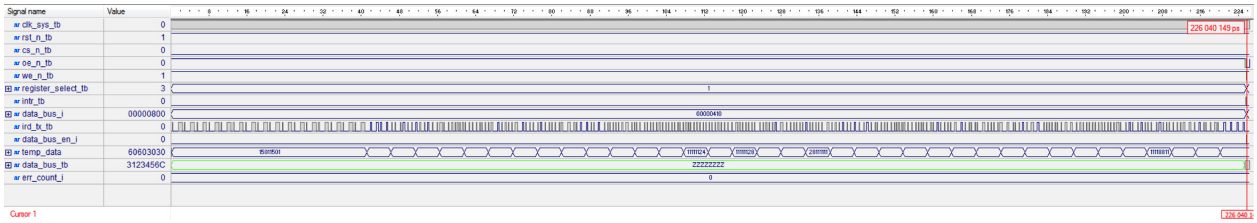
Timing Diagram

Figure 5. IrDA Receiver Write/Read Data/Configuration Register Timing Diagram



Simulation Waveform

Figure 6. Simulation Waveforms



Implementation

This design is implemented in VHDL. When using this design in a different device, density, speed or grade, performance and utilization may vary.

Table 5. Performance and Resource Utilization

Family	Language	Utilization (LUTs)	f_{MAX} (MHz)	I/Os	Architectural Resources
iCE40[1]	VHDL	643	83	40	N/A

1. Performance and resource utilization characteristics are generated using iCE-40LP1K-CM121 with iCEcube2 design software.

References

- iCE40 Family Handbook

Technical Support Assistance

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Revision History

Date	Version	Change Summary
October 2012	01.0	Initial release.