MachXO2 Hardened SPI Master/Slave Demo

User's Guide

May 2012
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Introduction

The Serial Peripheral Interface (SPI) bus is a synchronous serial data link standard developed by Motorola. The SPI bus is a 4-wire bus that operates in full duplex mode. SPI devices communicate using a master/slave relationship in which the master initiates the data frame. SPI interfaces are available on popular processors and microcontrollers.

The MachXO2™ Embedded Function Block (EFB) contains a hard SPI IP core that can be configured as a SPI master or slave. In Master mode, the SPI core has eight available Master Chip Select (MCSN) ports, allowing the control of up to eight external devices with the slave SPI interface. In Slave mode (user mode, after the device is configured), the SPI core has one slave chip select (SCSN) pin, allowing the SPI core to be selected by an external device with a master SPI interface. The SPI port can also be used for programming the device. Asserting the SN pin from an external controller will cause the SPI port to enter the configuration mode. In that condition, the SPI port acts as a Slave SPI interface and is used to access the configuration logic of the device.

This design demonstrates the use of the hardened SPI core as both master and slave on two MachXO2 Pico Evaluation Boards. One board is configured as SPI master and the other as SPI slave. For user interaction with the demo, a SPI-based digital clock has been designed. This includes capsense button controllers and LCD display logic. The SPI master board communicates with the SPI slave board based on user inputs through the capsense buttons.

Demo design hardware requirements:

- Two MachXO2 Pico Evaluation Boards
- Windows PC for implementing the demo project and downloading the bitstream
- USB download cable
- Connecting wires to make a connection between the SPI signals of the two boards

Demo design software requirements:

- Lattice Diamond® design software version 1.4 (or later)

Demonstration Design

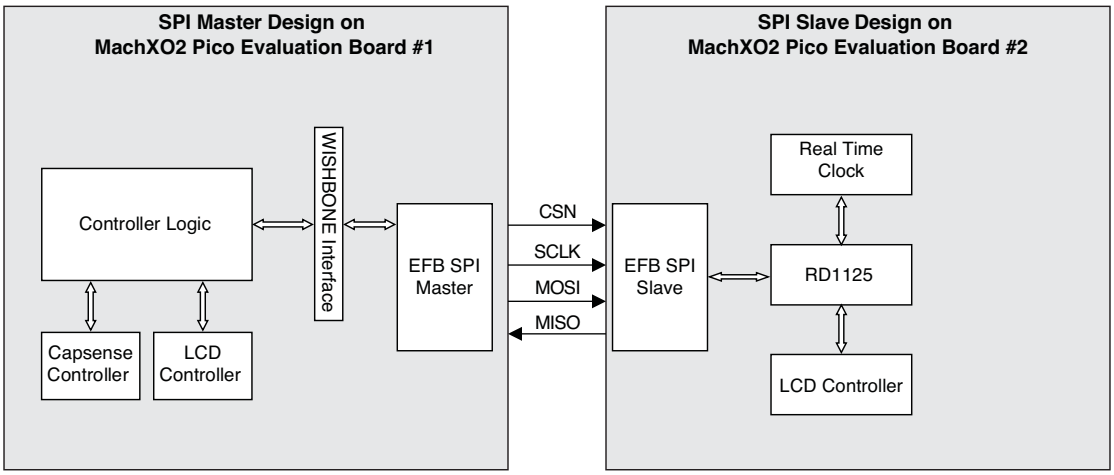
The MachXO2 Hardened SPI Master/Slave Demo consists of two designs:

- SPI Master demo design
- SPI Slave demo design

This demo showcases the use of the EFB SPI port in controlling a real time digital clock. Users can set the time in Hours (HH), minutes (MM) and Seconds (SS) using the capsense buttons. The SPI Master demo design responds to the user inputs by writing data to or reading data from the SPI Slave demo design using the hardened SPI primary IP core. The SPI Master demo design also has LCD controller logic which displays the real time clock.

The SPI Slave demo design incorporates RD1125, SPI Slave Peripheral Implementation using Lattice Embedded Function Block. The the GPIO output ports of RD1125 are connected to LCD controller logic. Figure 1 shows the block diagram of this demo design.

Figure 1. MachXO2 Hardened SPI Master/Slave Demo Block Diagram



MachXO2 Hardened SPI Master Design

Controller Logic

The controller logic controls the different modules of the SPI Master design. Users can interact with the controller logic through the capsense buttons. The controller logic generates the necessary WISHBONE signals to interact with the hardened SPI master module based on input from the user.

EFB SPI Master

The MachXO2 EFB hardened IP is configured to use the SPI IP as the SPI master in default mode (CPOL, CPHA, LSB set to 0) and operates at a data transfer speed of 10 MHz. The SPI IP interacts with the controller logic through the WISHBONE interface.

Capsense Buttons

The user can interact to the real time clock through the on-board capsense buttons on the SPI master board. There are four capsene buttons on the board and their functionality is described below:

- **Button 1**: Selects the mode of the clock, either Set or Run
- **Button 2**: Selects the hour of the clock
- **Button 3**: Selects the minutes of the clock
- **Button 4**: Selects the display option between Hours : Minutes (HH:MM) or Seconds (:SS)

MachXO2 Hardened SPI Slave Design

EFB SPI Slave

The MachXO2 EFB hardened IP is configured to use the SPI IP as a SPI slave. The SPI IP interacts with the controller logic through the WISHBONE interface.

RD1125

This design provides eight bytes of I/O port and memory interface, which is controlled through the SPI slave interface. There are four single-byte input ports and four single-byte output ports. This design interfaces with an embedded memory block. The memory read and write operations are controlled by the SPI commands. One of the GPIO output ports is connected to the LCD controller logic. Based on the commands received from the SPI master, data from the SPI master is displayed on the LCD.

RD1125 Commands Used for this Demo

Table 1 shows the commands used in this demo by the SPI Master design in order to access RD1125. For more information on the command structures and sequencing, please refer to the RD1125 documentation.

Table 1. RD1125 Commands

Operation	Command	Address Byte	Dummy Byte	Data Bytes
Enable	0x06	—	—	—
Disable	0x04	—	—	—
Write GPO	0x01	1	—	1
Latch GPI	0x03	—	—	1
Read GPI	0x05	1	1	1
Write Memory	0x02	1	—	1+
Read Memory	0x0B	1	1	1+

Port Descriptions and Pin Assignments

SPI Master Design

Table 2. SPI Master Design Pinout

Port	I/O	Description	MachXO2 Pin
rst_n	Input	Active low reset signal	N3
spi_csn	Output	SPI slave select	B2
spi_miso	Input	SPI master in slave output	N4
spi_clk	Output	SPI serial clock	M4
Spi_mosi	Output	SPI master output slave input	P13
intq	Input	SPI interrupt	B1
LCD_COM0	Output	LCD COM signal	B14
LCD_COM1	Output	LCD COM signal	C13
LCD_COM2	Output	LCD COM signal	C14
LCD_COM3	Output	LCD COM signal	D12
LCD_5	Output	LCD segment signal	J12
LCD_6	Output	LCD segment signal	J14
LCD_7	Output	LCD segment signal	J13
LCD_8	Output	LCD segment signal	K12
LCD_9	Output	LCD segment signal	K13
LCD_10	Output	LCD segment signal	K14
LCD_11	Output	LCD segment signal	L14
LCD_12	Output	LCD segment signal	M13
cap_btn1	Inout	Capsense button 1	M10
cap_btn2	Inout	Capsense button 2	P11
cap_btn3	Inout	Capsense button 3	M11
cap_btn4	Inout	Capsense button 4	P12
EnAMP	Output	Pico OpAmp power enable signal	P2
EnI2CSPI	Output	Pico I^2C/SPI power enable signal	N2

SPI Slave Design

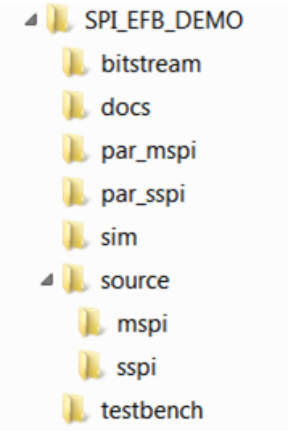
Table 3. SPI Slave Design Pinout

Port	I/O	Description	MachXO2 Pin
rst_n	Input	Active low reset signal	N3
spi_csn	Input	SPI slave select	B2
spi_miso	Output	SPI master in slave output	N4
spi_clk	Input	SPI serial clock	M4
Spi_mosi	Input	SPI master output slave input	P13
intq	Output	SPI interrupt	B1
LCD_COM0	Output	LCD COM signal	B14
LCD_COM1	Output	LCD COM signal	C13
LCD_COM2	Output	LCD COM signal	C14
LCD_COM3	Output	LCD COM signal	D12
LCD_5	Output	LCD segment signal	J12
LCD_6	Output	LCD segment signal	J14
LCD_7	Output	LCD segment signal	J13
LCD_8	Output	LCD segment signal	K12
LCD_9	Output	LCD segment signal	K13
LCD_10	Output	LCD segment signal	K14
LCD_11	Output	LCD segment signal	L14
LCD_12	Output	LCD segment signal	M13
EnAMP	Output	Pico OpAmp power enable signal	P2
EnI2CSPI	Output	Pico I^2C/SPI power enable signal	N2

Demo Directory Structure

The directory structure of the MachXO2 Hardened SPI Master/Slave Demo is shown in Figure 2. The demo package includes four top-level folders, bitstreams, docs, par_mspi,par_sspi, sim, source and test bench folder.

Figure 2. MachXO2 Hardened SPI Master/Slave Demo Directory Structure



bitstream
This folder includes the bitstreams for the SPI Master and Slave designs.

docs
This folder includes the MachXO2 Hardened SPI Master/Slave Demo User's Guide and the read_me file which contains the details of the different files in the demo and steps to regenerate the bitstream for the demo.

par_mspi
This folder includes the implementation project files for the Diamond design software and file for the SPI Master design.

par_sspi
This folder includes the implementation project files for the Diamond design software and file for the SPI Slave design.

sim
This folder includes the .do file to invoke the simulation for SPI Master/Slave demo.

Source
This folder includes the following subfolders,

- mspi – This folder includes all RTL source files used for the SPI Master design.
- sspi – This folder includes all RTL source files used for the SPI Slave design.

Apart from these subfolders, this folder also contains the common files which will be used in both the SPI Slave and SPI Master designs.

Setting up the Board

Connecting the MachXO2 Pico Evaluation Boards

1. The following pins of the header U3 on the two MachXO2 Pico Evaluation Boards must be connected to each other, as shown in Figure 3 (U3/Silkscreen/XO2).

   SPI_INTQ – Connect pin (19/B1/B1) of the two boards to each other

   SPI_CSN – Connect pin (21/B2/B2) of the two boards to each other

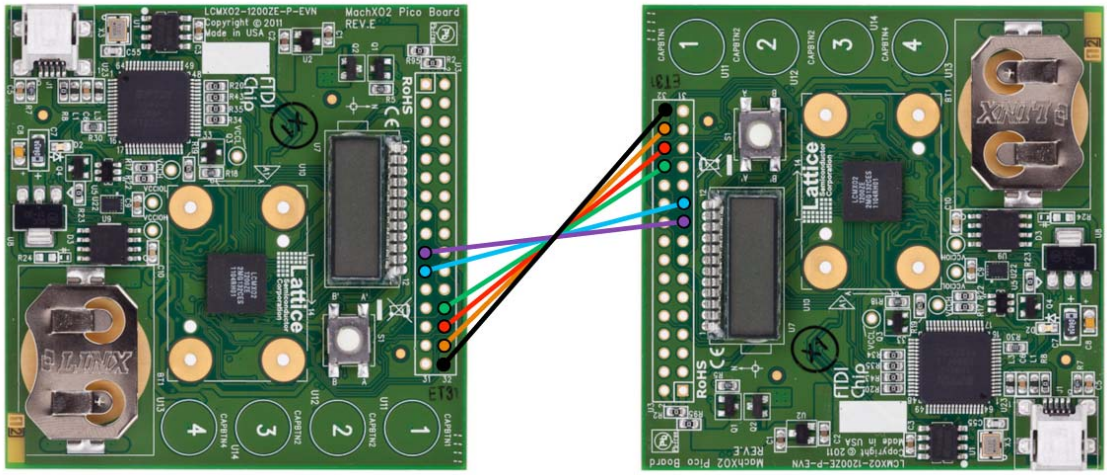
   SPI_CLK – Connect pin (26/SCK/M4) of the two boards to each other

   SPI_MOSI – Connect pin (28/SI/P13) of the two boards to each other

   SPI_MISO – Connect pin (30/SO/N4) of the two boards to each other

   Ground – Connect pin (32/GND/-) of the two boards to each other

Figure 3. Evaluation Board Connections



2. Press capsense button 1 on SPI master board to set the clock value
3. Press capsense button 2 on SPI master board to set the hour (HH) of the clock
4. Press capsense button 3 on SPI master board to set the minutes (MM) of the clock
5. Press capsense button 1 on SPI master board to start the clock
6. Press capsense button 4 to check the seconds values (:SS)
7. The SPI Master board will echo what is displayed on the SPI master board

Programming the Boards

Using ispVM™ System software, users can scan and perform JTAG operations, including programming the MachXO2 device. Program the two boards one at a time using the bitstreams in the following locations:

1. Program one of the MachXO2 Pico Evaluation Boards with the jed file in the following location:
   .\ XO2_EFB_SPI_Demo\bitsreams\mspi_top_mspi_top.jed
2. Program the second board with the jed file in the following location:
   \ XO2_EFB_SPI_Demo\bitsreams\sspi_top_sspi_top.jed

Once both the boards are programmed, power-up the SPI slave board first and then the SPI master board.

Running the Demo

After successfully setting up the two MachXO2 Pico Evaluation Boards, various demo operations can be performed by using the capsense buttons of the SPI master board.

Technical Support Assistance

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Revision History

Date	Version	Change Summary
April 2012	01.0	Initial release.
May 2012	01.1	Updated Evaluation Board Connections diagram and Design Pinout Tables 2 and 3.