

Enabling Low-Cost Displays for Digital Still Cameras

Image Rotation Using the iCE40 Ultra-Low Density FPGA

Market Dynamics

Smartphone demand is growing. In 2010, worldwide smartphone shipments reached 235 million units with a year-over-year growth rate of 29%.1 The International Data Corporation's research forecasts that smartphone vendors will ship more than 450 million smartphones in 2011 compared to the 303.4 million units shipped in 2010.

It is commonly known that volume drives price - higher volume means lower price. Smartphone display prices have dropped tremendously. Most popular smartphone display sizes range from 3.0" to 3.8".

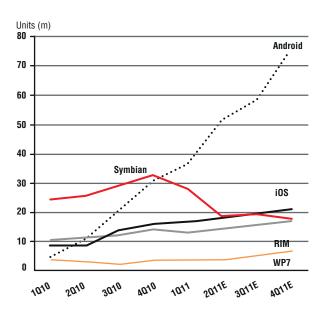


Figure 1: Smartphone shipment data by OS. From Gartner Group.

The price point is now ideal for many other applications where similar size displays are required. However, many applications cannot directly benefit due to the following issues:

- Interface incompatibility
- · Incompatible display output formats

Smartphone displays often support RGB and/or the MIPI interface. If an application does not support the RGB/MIPI interface then an interface conversion chip is needed. This can easily be solved by using an ASSP (Application Specific Standard Product) or an FPGA. The larger problem is incompatible display output formats. This can be addressed by using an iCE40 $^{\rm TM}$ FPGA.

Designer's Challenge

Most camera DSPs can only work with displays that are in landscape mode. The typical display output format from the camera DSP is shown in Figure 2. The longer line on top of the figure "HS" is the Horizontal Sync and the shorter one on the left side "VS" is the Vertical Sync.

However, mobile displays are in portrait mode (see Figure 3). In this case, "HS" and "VS" are different and therefore the image data writing sequence is also different.

To overcome this, designers must implement an image rotation function inside the camera DSP or use an external device to do the image rotation function. To perform this function, a minimum of two full frames of storage space is necessary.

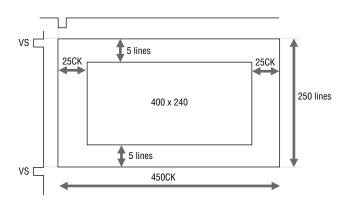


Figure 2: An example of landscape display data format.

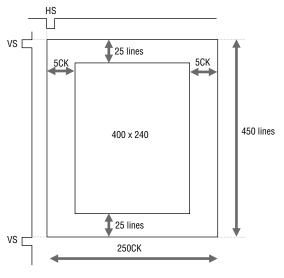


Figure 3: An example of portrait display data format.



Lattice Image Rotation Solution

The image rotation solution allows the receiving landscape scan images to be rotated and displayed on portrait type displays. To do this rotation, a minimum of two full-frame buffers of storage are required: one for reading and one for writing in alternation. To do this, an external storage device is required. Lattice uses a mobile SDRAM (see Figure 4).

Upon video data transfer, the FPGA sends the parameter data pre-stored in the internal ROM to the LCD Driver IC to initialize and change the status of the LCD. The camera DSP sends the control commands to the FPGA through the SPI port and the FPGA controls the LCD driver according to the command.

In reality, the rotated data is sent to the LCD after buffering in the memory in the iCE40 FPGA. The incoming/outgoing frame rate is twice the substantial frame rate, meaning the camera DSP sends the same image two frames in a row. Therefore, the SDRAM write by the FPGA happens in every other frame even though data read from the SDRAM happens in every frame. Data from the iCE40 FPGA can be either 60 fps or can be sent from the frame data in every other frame period.

LCD driver control can be different from vendor to vendor. Using an iCE40 FPGA is ideal since one device can be used with multiple different LCD driver ICs.

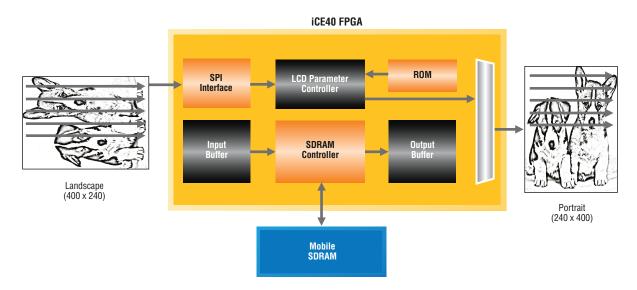


Figure 4: Image Rotation Block Diagram

Applications Support

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