Common Analog Functions Using an iCE40 FPGA

Integrate discrete analog devices into the iCE40 Ultra-Low Density FPGA

Analog Functions in an FPGA

FPGA designers are familiar with implementing digital designs by using FPGAs to glue together various processors, memories, and standard functions. In addition to these digital functions, FPGAs can also be used to implement some common analog functions. By using an LVDS input, a simple resistor capacitor (RC) circuit and some FPGA digital logic elements, designers can create a comparator, Analog-to-Digital Converter (ADC), Digital-to-Analog Converter (DAC), or simple temperature monitoring system.

Basic Comparator

The iCE40™ FPGA family offers 2 to 23 Low Voltage Differential Signal (LVDS) I/O pairs depending on density and package combinations. These differential I/O pairs are ideal for implementing common analog functions such as comparators, ADC and DAC. Figure 1 and Table 1 show the LVDS buffer and the comparator's common mode range. Input signals IN_P and IN_N are compared and the result is output to signal OUT as shown in Figure 2a. When the voltage of one of the inputs is out of the common mode range between VcmL and VcmH, then the other input must remain within the common mode range between VcmL and VcmH. Operating current adds 160 µA per comparator to ICCIO. An example application of the comparator is an infrared receiver is shown in Figure 2b. Reference voltage IN_N is compared with the voltage generated by photo diode current, IN_P. When infrared light is applied, OUT will switch from low to high.

Symbol	Description	VCCIO=1.8V	VCCIO=1.8V	Units
VcmH	Common mode voltage high	VCCIO/2 + 0.2	VCCIO/2+ 0.3	V
Vcm	Common mode voltage	VCCIO/2	VCCIO/2	V
VcmL	Common mode voltage Low	VCCIO/2 - 0.2	VCCIO/2-0.3	V
Icomp	ICCIO per comparator	160	160	µA

Table 1: Common mode operating ranges

Within the specified common mode range described in Table 1, input signals IN_P and IN_N are compared and the result is output to signal OUT. For high-speed operation, both inputs must remain within the common mode range between VcmL and VcmH. An example application of high-speed operation is in the camera serial interface in MIPI CSI-1. Common mode output levels from iCE40 bank 3 are set by 220Ω and 120Ω resistors at the transmitter. 100Ω resistors terminate the receiver side at the iCE40 bank 3 comparator inputs, setting the high voltage level at 3/5 * 1.8 = 1.08 V and the low voltage level at 2/5 * 1.8 = 0.72 V, within the specified common mode range.

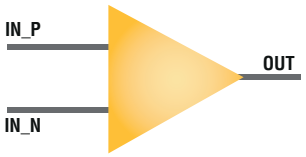

Figure 1: Comparator in iCE40

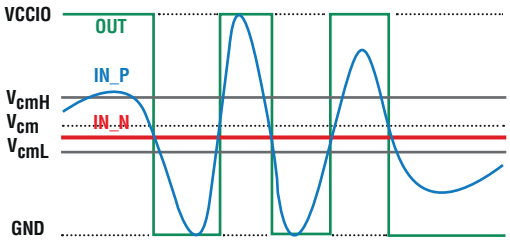

Figure 2a: Comparator waveform

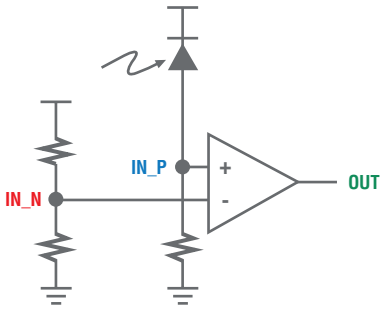

Figure 2b: Infrared receiver example

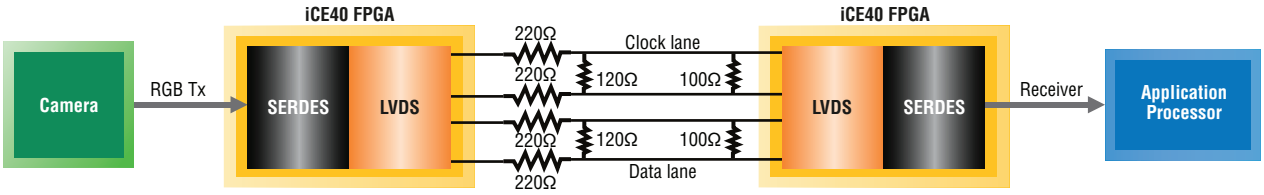

Figure 3: A comparator in the iCE40 MIPI CSI-1 application

Digital-to-Analog Converter (DAC)

A Delta-Sigma DAC can be implemented using an iCE40 FPGA. Figure 4 shows a block diagram implementing a digital-to-analog converter using the iCE40. A first, second or third order Delta-Sigma modulator can be implemented for desired performance. It offers 8 to 10-bit resolution with a 44 KHz sampling rate and is ideal for audio related applications.

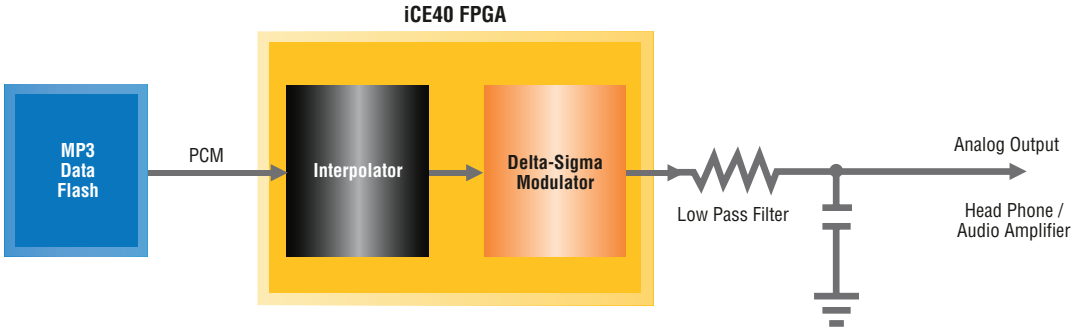

Figure 4: Implementing an Audio Decoder and Digital-to-Analog Converter with an iCE40 FPGA

Analog-to-Digital Converter (ADC)

Similar to a DAC, an analog-to-digital converter can be implemented using an iCE40 FPGA. A first order Delta-Sigma ADC with 8-bit resolution and a sampling frequency of 8KHz is implemented inside an iCE40 FPGA. This is ideal for sensor applications such as pressure, temperature, voltage and acceleration or motor control. Figure 5 provides a block diagram of an ADC in an iCE40 FPGA.

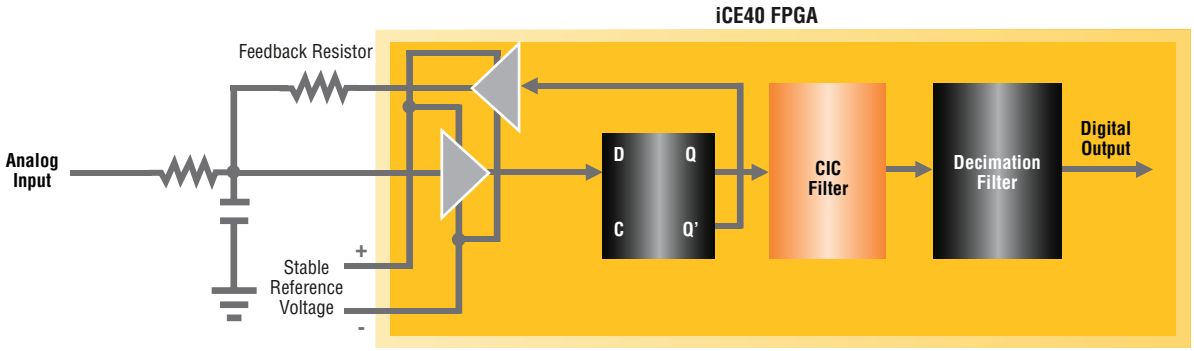

Figure 5: Implementing an Analog-to-Digital Converter with iCE40

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