Radio Expansion in Portable Navigation Devices

Enabling 3G Connectivity using the iCE40 Ultra-Low Density FPGA

Portable Navigation Market Dynamics

With smartphones and tablets seeing tremendous market growth, many Portable Navigation Device (PND) developers are adding 3G capability into the PND to make it a tablet-like device to attract more customers. PNDs come with a 7 to 10-inch display size, which is good enough for simple web browsing. However they lack wireless connectivity which prevents users from extensive web use. PNDs require either Wi-Fi connectivity or 3G connectivity. 3G is more practical since PNDs are primarily used on the road where a reliable Wi-Fi connection is often not available.

Design Challenges

So how would PND developers add 3G connectivity into their products? First of all, developers need to utilize their existing platform as much as possible. Fewer changes mean less work for developers and therefore less risk. This means absolutely no change to the main processor. So the question is, can existing PND processors connect to a 3G baseband processor? The ideal port to connect both would be a SDIO port, however both the 3G baseband processor and PND processor have SDIO host controllers making it impossible to connect (see Figure 2). This means an external device is needed to bridge the two processors. Since no Application-Specific-Standard-Product (ASSP) exists to support such a function, it must be done by using either an ASIC or an FPGA.

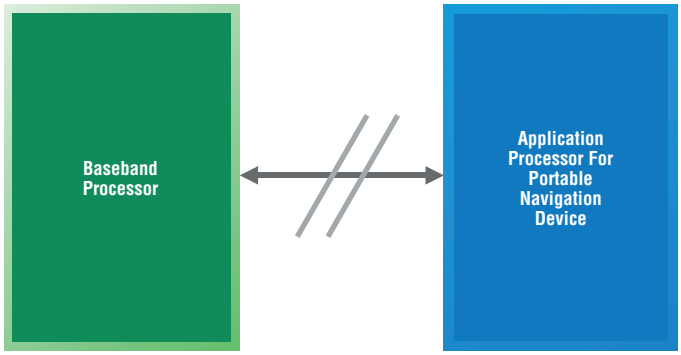

Figure 2: PND AP does not have a native port to connect to the baseband processor.

Figure 1: Portable Navigation Device with a 10-Inch Display

Lattice Solutions

SDIO is the ideal interface candidate for this application because it can run up to 200Mbps (SDIO Spec v2.0 @ 50MHz with 4-bit mode) offering more than enough bandwidth for existing 3G connectivity. With SDIO version 2.0 support, it can even support current 4G (LTE) bandwidth requirements. 4G (LTE) has a maximum bandwidth requirement of 100Mbps download and 50Mbps upload.

Lattice offers a quick way to add 3G capability to PND products by bridging to the SDIO ports of an existing PND Application Processor (AP). See Figure 3 for a detailed block diagram. Both PND AP and baseband processors offer only the SDIO host controllers preventing it from making the direct connection. Implementing an SDIO client controller to bridge the PND AP and high-speed parallel bus for the baseband processor is the ideal solution and offers the following advantages:

- As an SDIO client-based design, it can be added or removed easily to offer multiple product versions
- High-speed parallel bus allows easier driver implementation
- Designers can choose their preferred interface to hook up to the baseband processor

All of these benefits are offered in a low-cost, low-power, small form factor package, to satisfy a designer's needs.

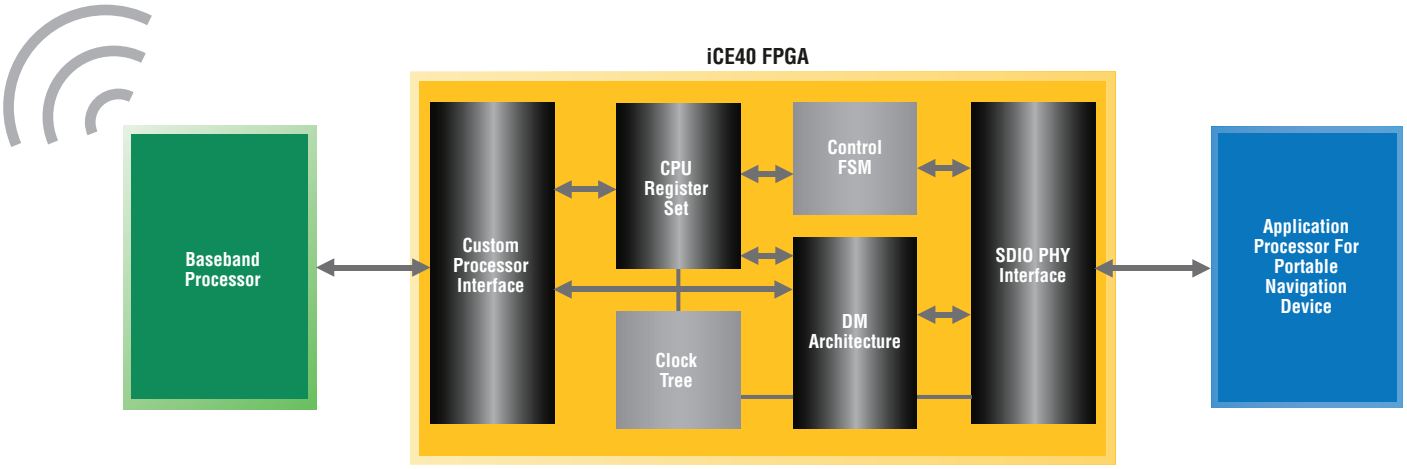

Figure 3: Enabling 3G connectivity through an SDIO client to the Navigation Application Processor

SDIO Client Controller

Users can easily instantiate the SDIO client controller in their design by using the Lattice iCEcube2™ software suite. SDIO client IP included in iCEcube2 software offers the following features:

- Complies with SDIO host specification, version 2.0
- Supports SDIO 1-bit and 4-bit modes
- Supports clock rates up to 50 MHz
- Supports automatic CRC16 generation and verification on DATA[3:0]
- Supports maximum byte count of 512 bytes

To learn more about the Lattice SDIO client controller, please download iCEcube2 software. Once installed, find the "IP" directory under the installation directory, then locate the documentation on the SDIO client controller IP. The documentation includes a simple block diagram, resource utilization, register settings and description of the IP.

Customization

There are multiple ways to connect to the baseband processor. One common way is to connect to the processor's high-speed parallel bus (memory bus). It can be customized to be address and data muxed/non-muxed, synchronous/asynchronous, and 8-/16-/32-bit architecture depending on the performance requirements. With the iCE40™ family of FPGAs, customization can be done at any phase of the development cycle allowing maximum flexibility to users.

Furthermore, designers can use the unused space left inside an iCE40 device to either replace other glue logic on the same printed circuit board or create new functions to increase product value. All of these can be done without adding a new device, lowering the overall bill of materials cost.

Applications Support
1-800-LATTICE (528-8423)
503-268-8001
techsupport@latticesemi.com

October 2012
Order #: SB005