Sensor Expansion for the Qualcomm MSM/QSD

EBI2 to Multiple I²C Masters Using the iCE40 Ultra-Low Density FPGA

Sensors in Smartphones

Sensors are changing the landscape of today's smartphones. According to IMS Research, "Sensors are poised to enable the next stage of mobile handset evolution. Various different sensor types are now showing the potential to alter user input methods, user interfaces, and to enable whole new genres of use cases for mobile handsets." Sensors not only enhance the user interface to smartphones but are also used to monitor environmental conditions such as battery life, temperature, and ambient light. In fact, today's high-end smartphones can contain anywhere from 10 to 20 different sensors.

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The I²C Bottleneck for Sensors

I²C is a common interface used to connect sensors to the Applications Processor (AP) of a smartphone. The issue smartphone designers face when adding additional sensors is that the I²C master controller found inside the AP can become performance-limited which in turn limits the number of sensors one can add (see Figure 1). In addition, the few and precious general purpose I/O (GPIO) for the AP often are not able to meet the performance requirements to emulate the I²C interface.

Using the I²C interface on the Qualcomm processor, a limited number of I²C sensor slaves can be implemented due to bandwidth and loading limitations on the bus.

EBI2 to Multiple I²C Masters

The EBI2 bus interface on a Qualcomm processor has greater bandwidth than the I²C interface. A Lattice iCE40™ ultra low density FPGA can be used to implement multiple I²C master controllers and interface to the Qualcomm processor via the EBI2 bus (see Figure 2). This allows the smartphone designer to implement additional I²C sensors and overcome the I²C bottleneck.

EBI2 to Triple I²C Master Reference Example

Lattice has created a reference example that implements an EBI2 to triple I²C master controller in an iCE40 FPGA. To further evaluate this reference example, please contact your local Lattice sales office.

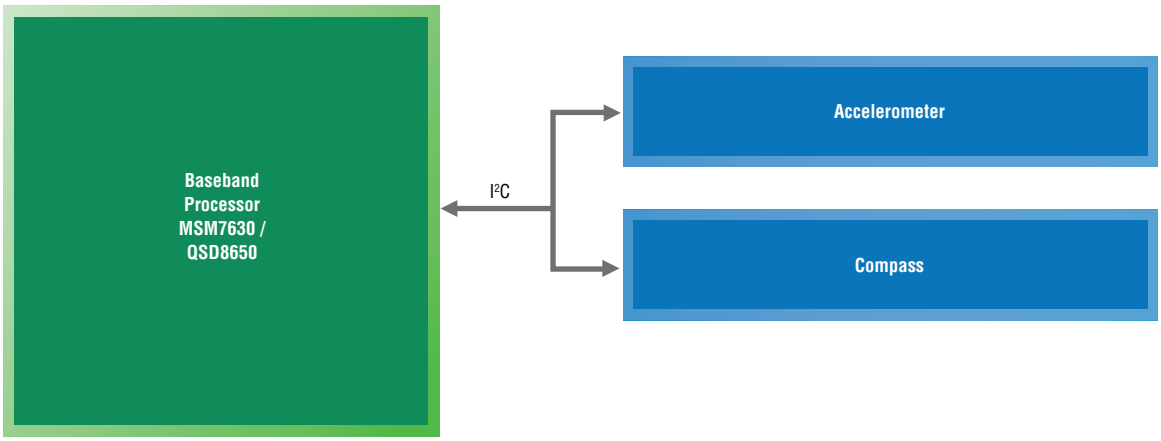

Figure 1

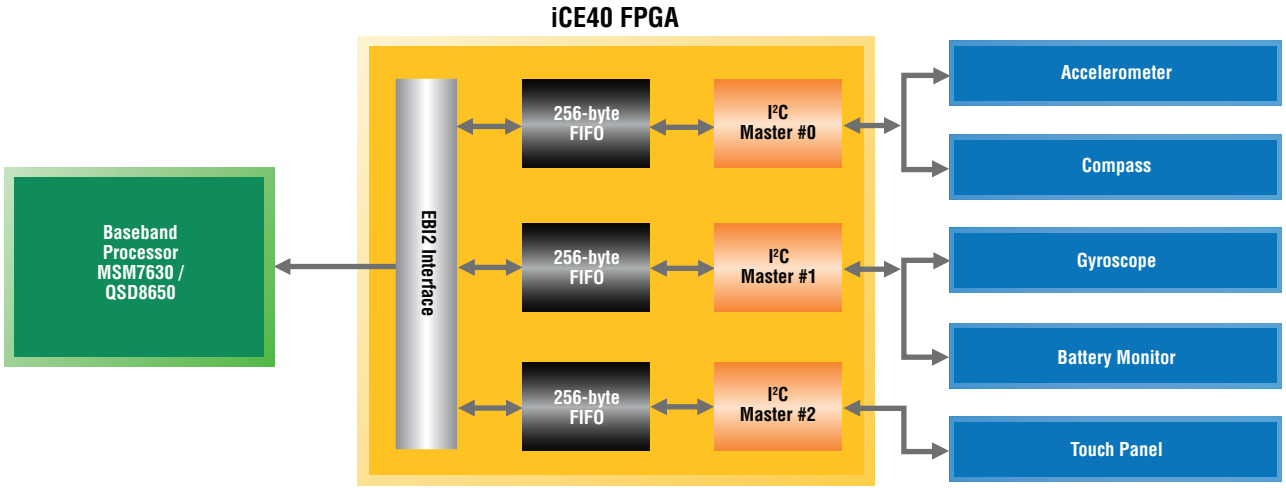

Figure 2

The iCE40 FPGA can serve as a bridge from the Qualcomm EBI2 bus interface to multiple I²C slave sensors, incorporating FIFOs and I²C master controllers. Figure 2 shows an EBI2 to triple I²C master controller example.

- **EBI2 to Triple I²C Reference Example Features**
  - EBI2 asynchronous interface with access time of <50 ns
  - Three I²C compliant masters support 100KHz (standard mode) and 400 KHz (fast mode)
  - Independent I²C master operation
  - I²C master clock stretching and repeated start operation
  - I²C master FIFOs (256 bytes deep)
  - Interrupt-driven or polling software interfaces
  - Implemented in a 4x4 mm ucBGA package
  - Standby current as low as 40µA

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