

Dual Sensor Bridge Reference Design

Dual Image Sensor Applications

When one thinks about an application with two image sensors, the first thought is likely to be a 3D camera. However, numerous designs can be improved by using the data from two image sensors; one example is Black Box Car Driver Recorders (CDRs), which typically are mounted near the rear view mirror and incorporate two cameras. Other applications include precision analytics in surveillance and pedestrian detection in automobiles. In these designs, the output of both cameras is used to create an algorithm that includes depth perception. With this data, a processor can very accurately "see" images and discern people from shadows or other objects.



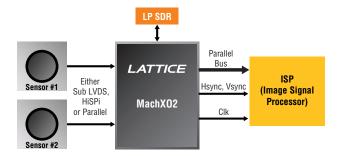


Camera Pointed at the Driver

Camera Pointed at the Front of the Vehicle

The Dual Image Sensor Bridge Design

Most Image Signal Processors (ISPs) can support the data throughput of two image sensors. However, most ISP devices have been designed to interface to only one sensor. Even ISPs that have two ports often cannot combine and process both images. and if they can, they tend to be expensive. The majority of ISP devices support traditional CMOS parallel sensor interfaces. They usually lack interfaces that support sub-LVDS and DDR I/Os. Therefore, a bridge device capable of synchronizing, merging and converting serial sensor interfaces to a CMOS parallel bus is required. The MachXO2™ non-volatile PLD provides an efficient and cost-effective solution for bridging two image sensors to a parallel ISP.



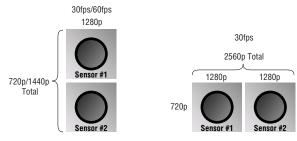
Applications Support

1-800-LATTICE (528-8423) 503-268-8001 techsupport@latticesemi.com

Key Features

- Complete Reference Design
- Designed to Emulate a Parallel Sensor Output
 - · Output bus width of 12 bits
- Accepts Two Aptina HiSPi 720P Interfaces
 - Aptina 9MT024 Sensor NanoVesta Headboard used for demonstration
- Synchronizes Both Sensors Completely
- Merges the Output into Either Left/Right or Top/Bottom Configuration
 - · Modes compliant with HDMI 3D specification version 1.4a
- Bridge Device Offered in Space-saving 8x8 mm 132-Ball csBGA. TQFP Packages Also Available.
- External LP SDRAM Used for Top/Bottom Configuration
- Parallel Interface can be Configured for 1.8V, 2.5V or 3.3V **LVCMOS** Levels

Output Format Examples



Top/Bottom Configuration

Left/Right Configuration

MachXO2 Dual Image Sensor Interface Board

The MachXO2 Dual Image Sensor Interface Board is available for demonstration and evaluation. Order the interface board (LCMXO2-4000HE-DSIB-EVN), the 9MT024 Sensor NanoVesta Headboard (LF-9MT024NV-EVN) and the HDR-60 Development Kit (LFE3-70EA-HDR60-DKN) to configure your own demo. Learn more about the Dual Sensor Bridge reference design at www.latticesemi.com/dualsensorbridge













Copyright © 2012 Lattice Semiconductor Corporation. Lattice Semiconductor, L (stylized) Lattice Semiconductor Corp., and Lattice (design) and MachXO2 are either registered trademarks or trademarks of Lattice Semiconductor Corporation in the United States and/or other countries. Other product names used in this publication are for identification purposes only and may be trademarks of their respective companies.

March 2012 Order #: I0226A