LATTICE
SEMICONDUCTOR™

SYNOPSYS®

iCEcube2 Development System
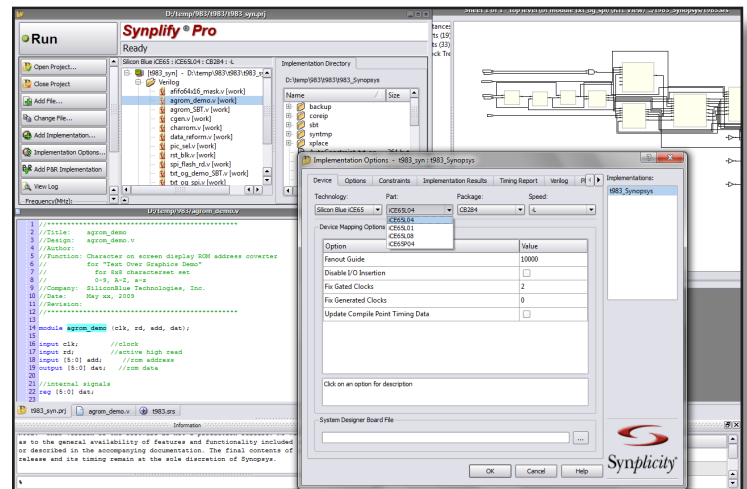*Powered by Synopsys' Synplify Pro Synthesis Tools*

Static Timing Analyzer

Project Navigator

Floor Planner

Package Viewer

Power Estimator
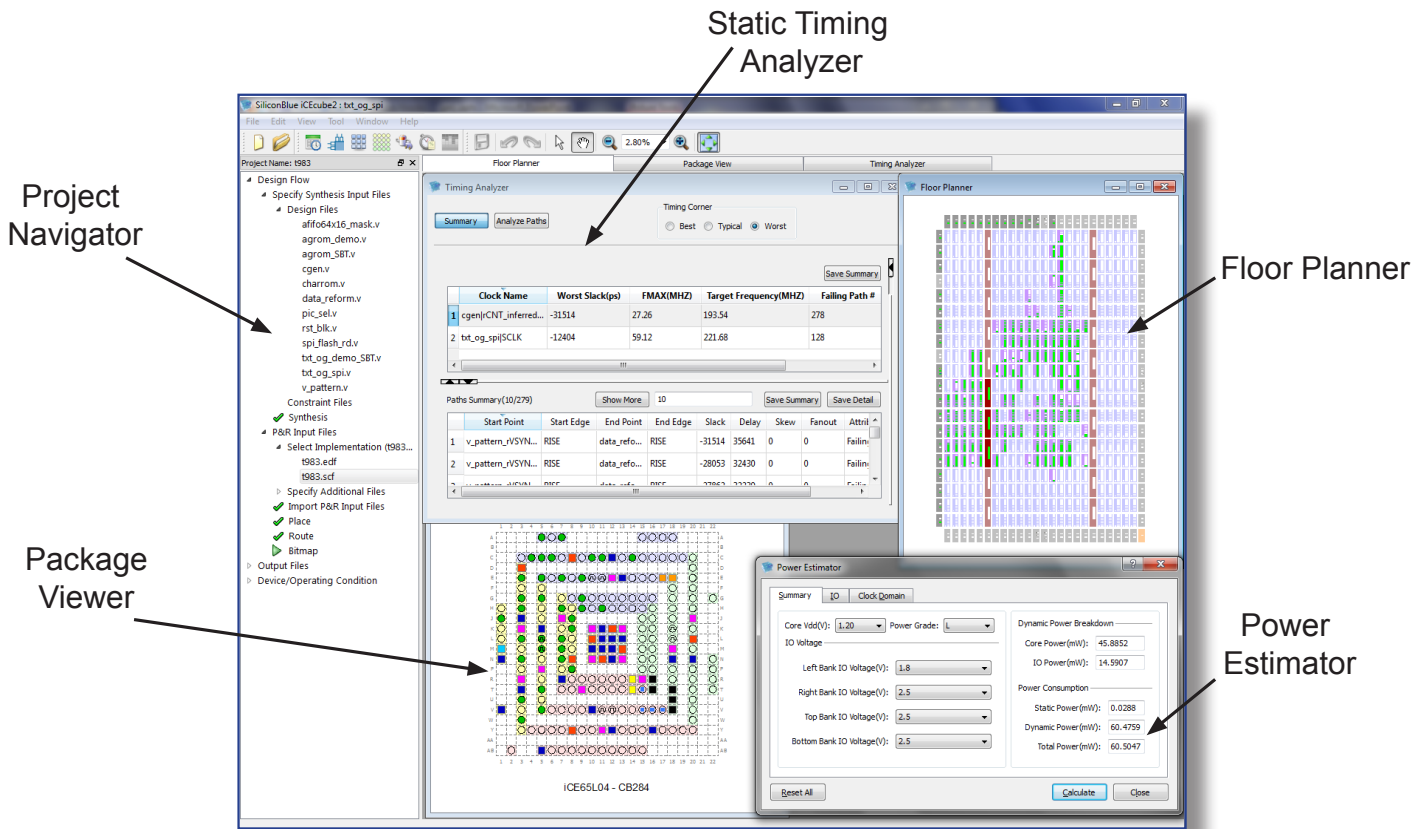
iCEcube2 Development System Design Environment

Mobile Design Efficiency

Design cycles for today's mobile applications are becoming shorter than ever before. Customer demand and stiff competition are forcing designers to bring products with new features to market constrained by tight development schedules. Design cycles that once took more than 2 years to complete have now shortened to 6 months or less. Thus, design efficiency is more important than ever before.

Lattice, a leader in ultra-low power, single-chip SRAM FPGAs has partnered with Synopsys, a leader in software and IP for semiconductor design to offer an integrated development system for the mobile designer. Lattice's iCEcube2™ development system is now fully integrated with Synopsys' Synplify Pro® synthesis tool to deliver world class synthesis and mapping technology to the mobile designer.

Synopsys' Synplify Pro synthesis tools are fully integrated with Lattice's iCE-cube2 Development System

Synplify Pro Features	Benefits
Timing-Driven Synthesis	Automatically optimizes for area once timing is met.
Proprietary BEST Algorithm	Globally optimized design acheives the best Quality of Results.
HDL Analyst	Generates an RTL block diagram from RTL for corss-probing with source code and identifies critical paths.
Comprehensive Language Support	Supports Verilog, VHDL, System Verilog, and mixed-language designs.
Automatic Retiming	Moves registers within combinatorial logic balancing delay and improving timing performance.
FSM Compiler and Explorer	Automatically extracts and optimizes Finite State Machines based on constraints.
Graphical State Machine Viewer	Automatic creation of bubble diagrams for debuggind and document FSMs.
Automatic RAM and DSP Inference	Extracts and optimizes memory and DSP functions from your RTL code.
Incremental Static Timing Analysis	Enables you to update timing exceptions and see results immediately, without re-synthesis.
Formal Verification Mode	Supports logical equivalency checking with popular logical equivalency checking tools.
ReadyIP™ Browser	Access to 3rd party IP for evaluation and download.
Incremental Design	Fast turnaround times with consistent results from one run to the next.
Contraints Checker and Advisor	Quickly configure RTL and constraints avoiding time-consuming pilot errors.

BEST Timing Results with the Lowest Area Utilization

Synopsys' Synplify Pro® product automatically achieves industry-leading quality of results by incorporating innovative optimization techniques including Synopsys' proprietary Behavior Extracting Synthesis Technology (BEST™). By extracting behavior such as Finite State Machines, DSP functions, and memories directly from the RTL code, the design can be optimized globally for performance. Automatic retiming, pipelining, or register balancing is also performed with the flip of a switch either locally or globally. This enables movement of registers inside combinatorial logic such that delay is balanced and clock speeds can be increased.

True timing driven synthesis technology allows designers to specify the timing performance required and not worry about the tool adding more logic than is necessary. Less logic reduces power consumption and often allows implementation in a smaller part since the extra logic can bump the FPGA device requirement to the next larger and more costly size.

Design Checking and Analysis

Included in the Synplify Pro software is the powerful HDL Analyst graphical analysis and debug tool. This provides designers with an instant understanding of what their Verilog or VHDL code produced by creating a high-level RTL graphical diagram that can be cross-probed with the

source code and a gate-level (post synthesis) schematic also produced by the HDL Analyst tool. Critical paths in a design are quickly highlighted and can be analyzed in an easy to read format. The Synplify Pro tool includes a design constraints checker to help correctly and completely configure design constraints so as to avoid pilot errors, properly meet design intent, and to attain improved performance.

IP Use and Evaluation

The Synplify Pro software allows IP providers a secure way of distributing their IP and enables designers an easy way to evaluate and integrate IP into their FPGA design. The Synplify Pro software also provides web-based access to download various IP-XACT compliant IP for evaluation.

Interface to Industry Leading Simulation Tools

iCEcube2™ generates design timing information in Standard Delay Format (SDF) for post-synthesis and post-layout simulation. The export of both VHDL and Verilog netlists are also supported.

Supported Platforms
- Windows XP and Vista
- Linux

Applications Support
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