DDR2 Demo for the LatticeECP3 Serial Protocol Board

User's Guide

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Introduction

This document provides technical information and instructions for using the LatticeECP3™ DDR2 demo design. This demo demonstrates the functionality of the Lattice DDR2 SDRAM Controller IP core at a speed of 200 MHz and 400 Mbps using the LatticeECP3 Serial Protocol Board. The document provides a circuit description of the demo logic as well as instructions for running the DDR2 demo.

The demo package includes the following:

- DDR2 SDRAM Controller IP core configuration files (.lpc, .ipx)
- Verilog source code for the demo logic design
- Lattice Diamond® implementation project files (.ldf) along with the preference files (.lpf) for the demo project
- Aldec® Active-HDL™ and Mentor Graphics® ModelSim® simulation scripts (.do) and Verilog test bench
- 32-bit DDR2 demo bitstream file (.bit)

Demo design hardware requirements:

- LatticeECP3 Serial Protocol Board Revision E with a LatticeECP3-95EA FPGA, 1156-ball fpBGA package
- 12V DC power supply for LatticeECP3 Serial Protocol Board
- Windows PC or Linux machine for implementing the demo project and downloading the bitstream
- JTAG download cable

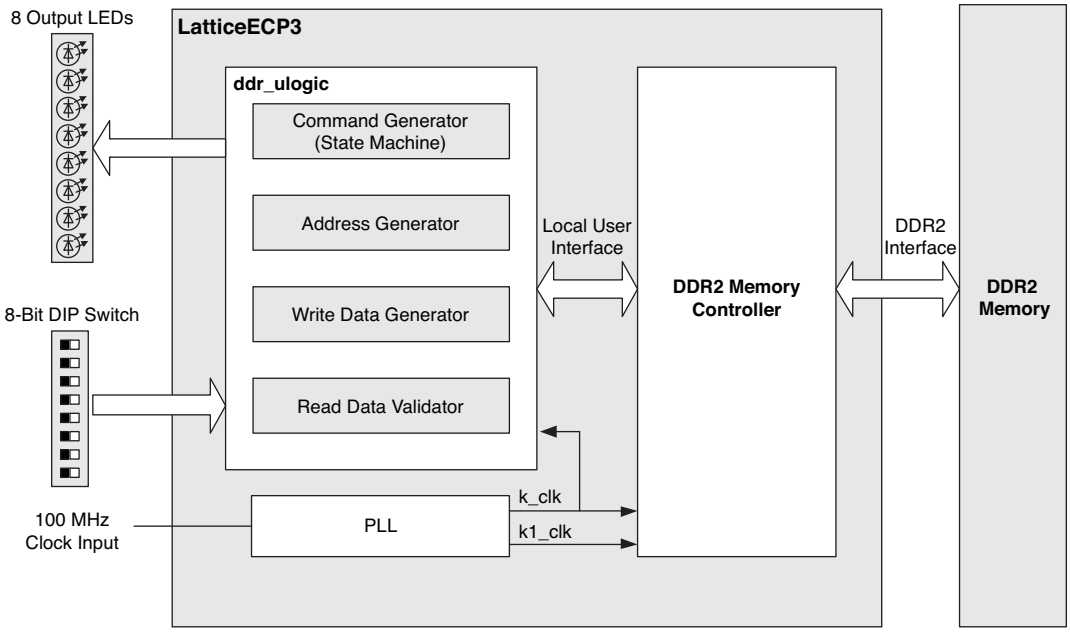
Demo design software requirements:

- Diamond design software version 1.3 (or later)

DDR2 Demo Design Overview

The DDR2 demo design consists of two major parts: a DDR2 SDRAM Controller IP core and the user logic block. The latter includes a function block that exercises and analyzes the DDR2 data stream. Figure 1 illustrates a block diagram of the demo design.

Figure 1. DDR2 Demo Design Block Diagram



DDR2 SDRAM Controller IP Core

The demo has been designed to support the parameterized DDR2 data bus widths (8-, 16-, 32-, and 64-bit configurations). The user logic is also parameterized by the core parameter file. Once a DDR2 core is generated with a supported data width, the whole demo design can be simulated and implemented without modifying the code. A DDR2 IP core configuration file for the 32-bit data width is provided in the demo package. If a different configuration is to be used, the following conditions need to be met:

- DDR2 data width is 8, 16, 32, or 64 bits
- One chip select only
- Select the default DDR2 memory device and keep the default DDR2 timing parameters (If a DDR2 memory device or module with a different specification is to be used, make the necessary updates in the DDR2 timing parameters to match them with the timing parameters of the memory to be used)
- Keep all other core options unchanged

User Logic

The user logic implemented in the DDR2 demo design provides the following functions:

- State machine programs the mode registers and controls DDR2 read and write operations
- Address generation
- Write data generation
- Read data validation
- Control and observation

Demo Control State Machine

The state machine controls the demo using the user control input through an 8-bit DIP switch. Once the LatticeECP3 device is programmed and a system reset is applied (the GSR (SW1) button is pressed), the state machine programs all DDR2 mode registers (MR/EMR) based on the user test configuration (DIP switch setting). Then, it generates a write command sequence. The write command can be repeated up to 32 times using either the command burst feature of the core or multiples of single write commands depending on the user setting. After the write command sequence, a read command sequence is initiated. The read command sequence can also be repeated up to 32 times in the same way as the write command sequence. The read command sequence that follows the write command sequence must include the same number of commands as the as the write command sequence. The state machine makes sure that both the write and the following read command sequences are always the same even when the user test configuration is changed at any time during the command sequences. This allows the DDR2 demo to be dynamically reconfigurable.

Address Generation

The address generation block provides the start address for the current user read/write command which is generated by the state machine. When the burst command mode is enabled, the address generation block automatically calculates the next address according to the demo control input.

Write Data Generation

The demo uses both PRBS and sequential data patterns. When PRBS is selected, a PRBS pattern generator is implemented to the local write data bus to generate up to a 64-bit DDR2 data pattern. For 32-bit DDR2 data, for example, an identical 64-bit PRBS pattern is allocated to both the upper and lower halves of the local data bus. For the sequential data pattern, the demo design uses only a 32-bit sequential data pattern generator to provide up to 64-bit DDR2 data. This 32-bit data pattern is allocated to each 32-bit wide local data bus slot. For example, a 64-bit DDR2 bus requires a 128-bit local data bus which has four identically sequenced 32-bit patterns allocated on four 32-bit slots. The write data generation is enabled and driven by the data_rdy signal assertions.

Read Data Validation

The read data checker validates the read data from the DDR2 memory module. To do this, it generates the expected data patterns using exactly the same data sequences as the Write Data Generator block. The expected data generation is enabled and driven by the read_data_valid signal assertions. The read data captured by read_data_valid is compared with the expected data generated from the Expected Data Generator block. As soon as both data patterns mismatch each other, the demo design will flag the error detection signal.

Control and Observation

The Control and Observation block includes the demo control input and result display functions. The demo control input uses an 8-bit DIP switch available on the LatticeECP3 Serial Protocol Board. The demo result is displayed through the eight LEDs on the board. See the following section for descriptions of the demo control input switches and the result display LEDs.

LatticeECP3 Serial Protocol Board Setup for Demo

This section describes the setup requirements for the DDR2 demo using the LatticeECP3 Serial Protocol Board.

DDR2 Memory

The LatticeECP3 Serial Protocol Board has two 16-bit DDR2 memory devices to support a 32-bit DDR2 interface. Therefore, you can implement an 8-, 16-, or 32-bit DDR2 interface on the LatticeECP3 Serial Protocol Board.

Programming Cable Connections

The LatticeECP3 device on the LatticeECP3 Serial Protocol Board can be programmed via the JTAG download port or through the SPI Flash interface. If the JTAG port is used, it can both program the device and use the Reveal™ logic analyzer when internal signal paths are to be traced. The J12 connector is used for the JTAG downloading. More details on programming the board are given in the LatticeECP3 Serial Protocol Board User's Guide (EB49).

Port Assignments and Descriptions

Table 1. DDR2 Bus Interface

Port Name	Active	Direction	Description
em_ddr_clk	N/A	Output	Memory clock generated by the controller.
em_ddr_cke	High	Output	Memory clock enable generated by the controller.
em_ddr_ras_n	Low	Output	Memory row address strobe.
em_ddr_cas_n	Low	Output	Memory column address strobe.
em_ddr_we_n	Low	Output	Memory write enable.
em_ddr_cs_n	Low	Output	Memory chip select.
em_ddr_odt	High	Output	Memory on-die termination control.
em_ddr_dm	High	Output	DDR2 memory write data mask.
em_ddr_ba	N/A	Output	Memory bank address.
em_ddr_addr	N/A	Output	Memory address bus, multiplexed row and column address for the memory.
em_ddr_data	N/A	In/Out	Memory bi-directional data bus.
em_ddr_dqs	N/A	In/Out	Memory bi-directional data strobe.

Table 2. Demo User Interface Ports

Port Name	Active	Direction	Description
clk_in	N/A	Input	Reference clock connected to a dedicated PLL clock input (P30) of the LatticeECP3-95EA FPGA.
reset_n	Low	Input	Asynchronous reset connected to the GSRN button (B23). This resets the entire demo system including the DDR2 SDRAM Controller IP core when asserted.
switch[7:0]	N/A	Input	User test configuration input. See the Control and Observation Port Description section of this document for further information.
oled[7:0]	N/A	Output	Demo result LED indicator output. See the Control and Observation Port Description section of this document for further information.

Control and Observation Port Descriptions

Table 3. DIP Switch Definitions

Signal Name	DIP Switch Number	Assigned Function Control	Setting			Description
switch[0]	8	Burst Length Selection	Up			Set Burst Length to BL8.
			Down			Set Burst Length to BL4.
switch[1:2]	7, 6	On Die Termination (ODT) selection	Up	Up		75-Om ODT select
			Up	Down		150-Ohm ODT select
			Down	Up		50-Ohm ODT select
			Down	Down		No ODT selection
switch[3:5]	5, 4, 3	Maximum Command Size	Up	Up	Up	32 command burst
			Up	Up	Down	
			Up	Down	Up	
			Up	Down	Down	16 command burst
			Down	Up	Up	8 command burst
			Down	Up	Down	4 command burst
			Down	Down	Up	2 command burst
			Down	Down	Down	1 command burst
switch[6]	2	Data Mode	Up			PRBS data patterns are used for the DDR2 demo.
			Down			Sequential data patterns are used for the DDR2 demo.
switch[7]	1	Demo Mode Select	Up			Continuous write-then-read transactions. The DDR2 demo runs without pause until a system reset is applied.
			Down			Single read/write command.

Output LEDs

Eight LEDs are used to indicate the demo progress and results. The numbering of the LEDs starts from the left (oled[0]) to the right (oled[7]). The Assigned/Color column shows the LatticeECP3 ball numbers printed and the color of the LEDs on the LatticeECP3 Serial Protocol Board. Active/Expected column shows the working status and the expected status of the LEDs.

Table 4. Output LED Definitions

Name	Assigned/ Color	Function	Active/ Expected	Description
oled[0]	W32/Red	INIT-done indicator	ON/ON	This LED indicates the core initialization is successfully done
oled[1]	W31/Yellow	Core ready indicator	ON/ON	This LED indicates the core is ready to accept user commands
oled[2]	V29/Green	Write Indicator	ON/ON	This LED indicates that the core's write operation is properly working by detecting the data_rdy signal assertions.
oled[3]	W28/Blue	Read indicator	ON/ON	This LED indicates that the core's read operation is properly working by detecting the read_data_valid signal assertions.
oled[4]	W30/Blue	Heart-beat indicator	Blink/Blink	This LED indicates that the board is alive, and the core is receiving the clock input.
oled[5]	W29/Green	DDR2 transaction rate indicator	Blink/Blink	This LED indicates that DDR2 Write-then-Read operations are going on. The more read data that comes in, the faster this LED blinks.
oled[6]	W27/Yellow	Valid data indicator	Blink/Blink	This LED confirms that proper DDR2 read/write transactions are being performed with actual valid data. If the received data is null (all '0' or all '1') this LED will not blink.
oled[7]	W26/Red	Error Indicator	Blink/OFF	This LED will start blinking when the first data miss-match error is detected. A system reset must be applied to clear this indicator

Demo Package Directory Structure

The directory structure of DDR2 demo package is shown in Figure 2. The demo package includes three top-level folders: the core folder, resource folder and user_logic folder.

Core Folder

The core folder includes a DDR2 SDRAM Controller IP core configuration file (ddr2_ecp3.lpc). A complete DDR2 IP core can be regenerated using this file through the IPexpress™ tool.

Resource Folder

The resource folder includes the following subfolders:

- **Bitstream** – This folder includes a 32-bit demo bitstream. This bitstream is fully tested and can be used to verify the demo setup.
- **Doc** – This folder contains a user document that provides brief information about the demo procedure and setup, which can be used as a concise reference during a demo.

User_logic Folder

The user_logic folder includes the following subfolders:

- **Par** – This folder includes the implementation project files for the Lattice Diamond and other necessary files including the place and route (PAR) preference and the implementation strategy file.
- **Sim** – This folder includes the simulation script files for the ModelSim and Active-HDL simulation tools.
- **Src** – This folder includes all RTL source files used for the demo.
- **Testbench** – This folder includes the test bench file for the demo design (ddr2_demo_tb.v).

Figure 2. DDR2 Demo Package Directory Structure

Demo Procedure

Step 1. Core Generation

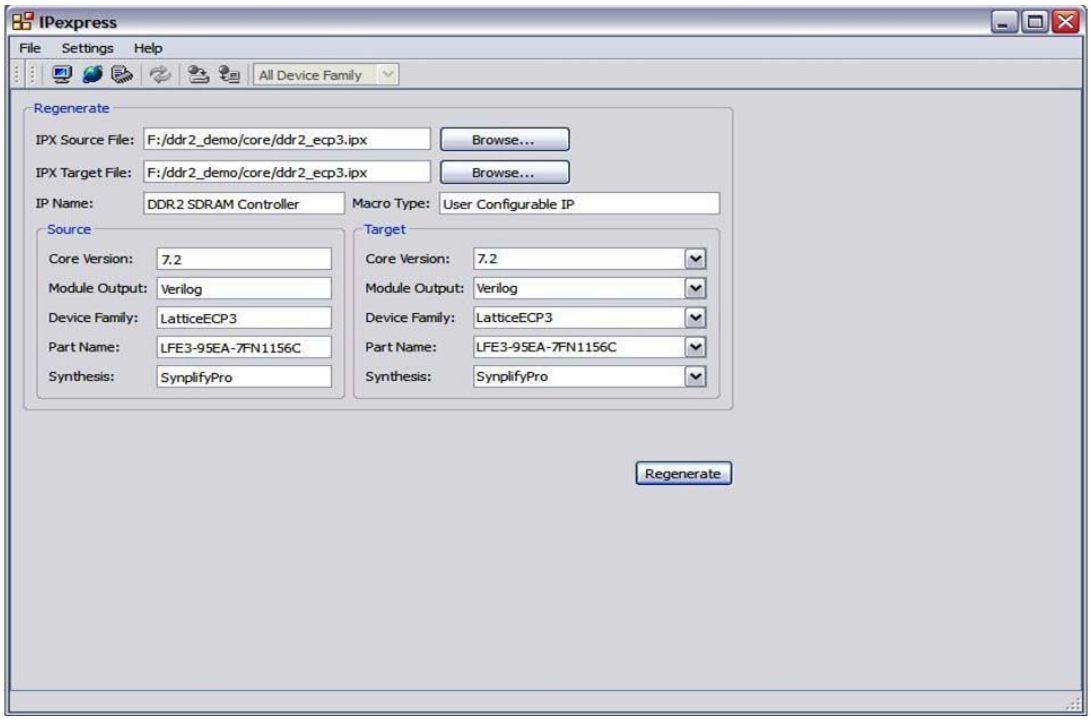
A default 32-bit DDR2 core LPC file is located under the Core folder.

a. Open the IPexpress tool and select the **Regenerate** icon.

b. Browse to the core folder where the .lpc file is located. Select the .lpc file and click **Open**.

c. Make sure the source and target devices are the same (family, package, speed) as shown in Figure 3. Click **Regenerate**.

Figure 3. IPexpress IP Core Regenerate Window



d. Once the DDR2 core configuration GUI is launched, click **Generate**. The DDR2 SDRAM Controller IP core will be generated inside the folder where the .lpc file is located.

*Note: If your DDR2 memory module requires different memory timing parameters, select the **Timing** tab and modify the desired parameters. Most DDR2 memory devices should not require timing changes.*

Step 2. Running Simulation

The demo package provides the simulation scripts for Active-HDL and ModelSim.

Active-HDL

a. Open the simulation script file (**ddr2_ecp3_demo.do**) and update the Lattice tool path names with your local folder name.

b. Launch Active-HDL Lattice Edition, then click **Cancel** in the Getting Started dialog box.

c. Change the directory by entering **cd [your_local_path]\ ddr2_demo\user_logic\sim\aldec** in the Console window.

d. Select **Tools > Execute Macro**, and then browse to the folder where the Active-HDL script (.do file) is located.

e. Select the **ddr2_ecp3_demo.do** file and then click **Open**.

f. Once the simulation is finished, check the status of the err_det signal along with other signals of interest. The err_det signal should remain low at all times for a successful demo.

ModelSim

a. Open the simulation script file (**ddr2_ecp3_demo.do**) and update the Lattice tool path names with your local folder name.

b. Launch the ModelSim simulator.

c. Select **File > Change Directory**, and then browse to the folder where the simulation script (**ddr2_ecp3_demo.do**) is located.

d. Select **Tools > Tcl > Execute Macro**, and then select the script file (**ddr2_ecp3_demo.do**) followed by clicking **Open**.

e. Once the simulation is finished, check the status of the err_det signal along with other signals of interest. The err_det signal should remain low at all times for a successful demo.

The simulation run time is set to 10 us by default. Changing the DIP switch settings in the test bench file will provide different operation mode simulation results.

Step 3. Running Place & Route (PAR)

A design preference file (ddr2_ecp3_spb.lpf) is located in the user_logic\par\[software] folder. Using a proper preference file is very important for a successful DDR2 implementation. When a different DDR2 bus size IP core is generated using the provided .lpc files, the corresponding .lpf file must be located in the par folder.

Diamond

a. Launch the Lattice Diamond design software.

b. Select **File > Open > Project** and browse to the par folder (**user_logic\par\diamond**).

c. Select the DDR2 demo project file for Diamond (**ddr2_ecp3_spb.ldf**) then click **Open**.

d. Double-click **Place & Route Design** in the **Process** pane. The software will run synthesis, and place and route.

e. Check the static timing results from the **Analysis Result** pane.

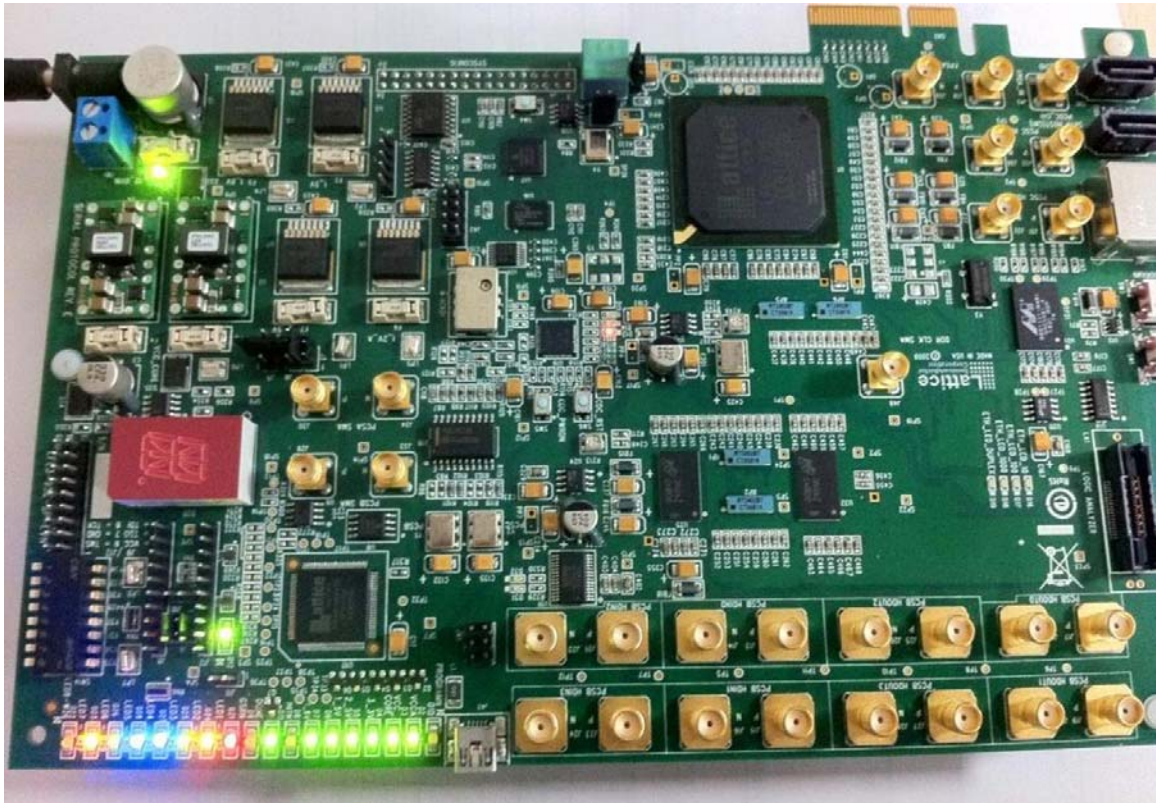
f. With a successful timing result obtained, double-click on **Bitstream File** in the **Process** pane to generate a bitstream file.

Step 4. Setting Up the DDR2 Demo

a. Connect a JTAG download cable to the Local JTAG connector (J12) on the board.

b. Turn the board power on by connecting the power adapter plug into the board power jack (J1). Proper set-up is shown in Figure 4.

Figure 4. LatticeECP3 Serial Protocol Board Setup for DDR2 Demo



Step 5. Running the Demo

Diamond Programmer

a. Launch the Diamond Programmer tool.

b. Scan the JTAG chain by selecting **Design > Scan**.

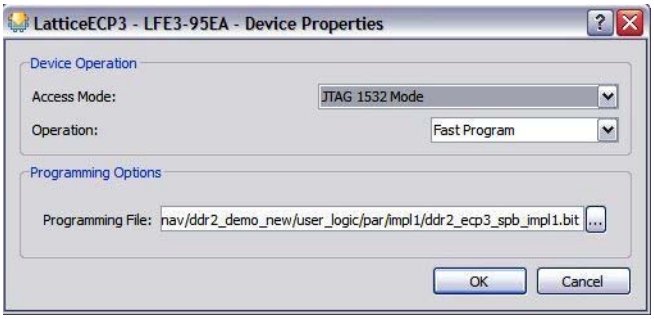
c. Double click the **Status** or **Operation** field to open the Device Properties box.

d. Make sure that the Device Operation mode is set to **JTAG 1532 Mode with Fast Program** (default setting).

e. Click the **Browse** button and browse to the project implementation folder where the generated bitstream file is located. Click **Open** as shown in Figure 5. Then click **OK**.

f. Click on the **Program** button from the toolbar or select **Design > Program** to download the bitstream.

Figure 5. Diamond Programmer Device Properties



g. Configure your demo to a test mode using the DIP switch (**dip_sw[7]**) setting as described previously.

h. Press the **GSRN** button (SW1) to initialize the core and the demo user logic.

i. Some of the demo modes are dynamically switchable, as described previously. Experiment with the DIP switch settings to test other modes.

j. Check the output LEDs to see if their outputs match with the expected result.

Technical Support Assistance

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Revision History

Date	Version	Change Summary
December 2011	01.0	Initial release.