GEN2 Serial RapidIO AND LOW COST, LOW POWER FPGAS

A Lattice Semiconductor White Paper

August 2011

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Introduction

As bandwidth requirements for applications such as wireless, wireline and medical/imaging processing continue to grow designers depend on the toolsets necessary to provide them with the real-time signal processing capabilities that are needed. In the wireless world, for example, for existing 3G overlays such as HSPA+ and EV-DO (i.e., 3G+) and the now emerging 4G deployments, the emphasis is on data throughput and backhaul requirements. These are needed to support the rapidly increasing subscriber base, and the seemingly endless number of video and data applications these technologies enable. This in turn requires high speed processing and, as importantly, a very reliable, high throughput and low latency interface protocol to support the needs of the various DSP farms, co-processing and bridging applications mandatory in these applications. And, as with most systems, cost and power are of the utmost importance as well. DSP and Network Processing Unit (NPU) devices, coupled with low cost, low power FPGAs that support Gen2 Serial RapidIO (SRIO), can provide an ideal platform for meeting these challenges.

Gen 2 SRIO

The RapidIO specification is a packet-based technology defined for endpoints, which originate and process the packets and switching that are used to connect other endpoints. As shown in Figure 1, the protocol stack is a three layer specification divided into a physical layer protocol, packet transport (routing) layer protocol and multiple transfer types at the logical layer.

Broadly viewed, the key additions to the Gen2 specification are support for 5/6Gbps serial data rates (SERDES) and the addition of a 2x lane configuration for these high speed serial channels (versus just a 1x/4x available in the previous v1.3 version of the specification). As already noted, a premium is being placed on performance without sacrificing a design's cost or power budget, and so the focus of this white paper is on the Gen2 specification's 2x capability. This is a key enhancement, because in many cases systems need more throughput than a single 3.125Gbps lane can provide, but a

4x lane configuration is overkill. This is where the 2x SERDES lane configuration now can provide an effective solution that allows designers the option to stay with a low cost, low power FPGA solution, such as the LatticeECP3, that can support most applications with up to a 4x lane configuration at speeds up to 3.125Gbps.

The programmability and flexibility of an FPGA comes into play at the Logical Layer, where multiple traffic passing techniques can be implemented. As Figure 1 shows, there are four data passing protocols. These are direct I/O access, message passing, GSM and data streaming. The Logical Layer can be customized, depending on the system architecture/requirements, to define how SRIO endpoints exchange data. Figure 1 shows the protocol stack as represented in the RapidIO specification.

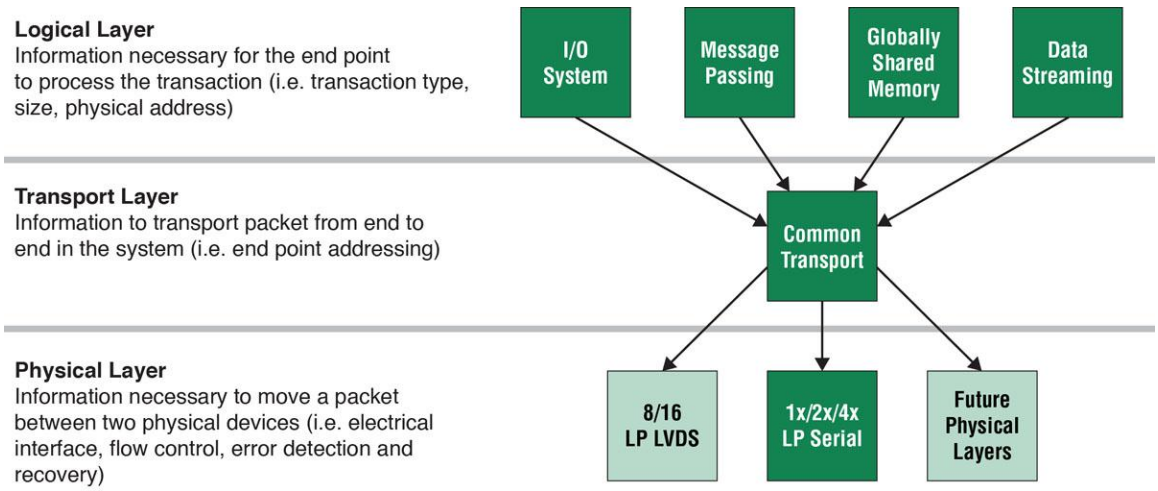

Figure 1 – RapidIO Protocol Stack

Figure 2 shows how the protocol stack can be implemented within a low cost programmable platform such as the LatticeECP3. The Physical and Transport Layers are implemented as a standard soft IP core, but much of the Logical Layer is left to the user to customize in order to meet specific design requirements.

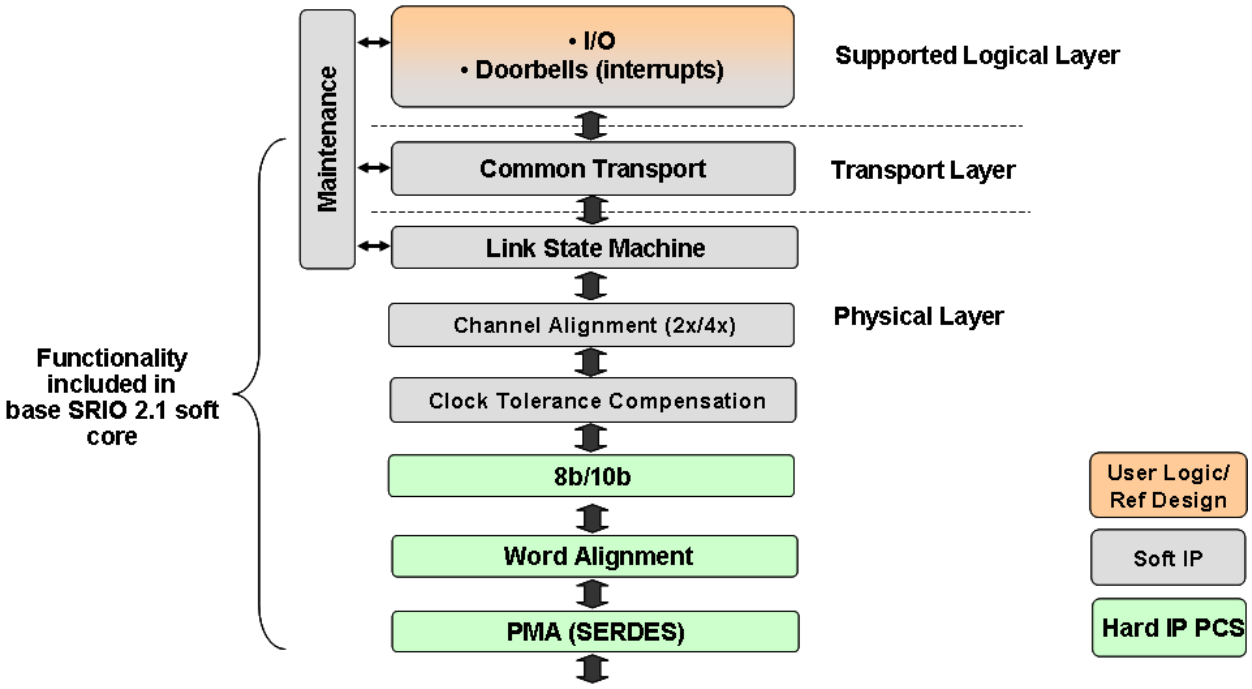

Figure 2 – Example of FPGA Implementation

The Role and Benefits of Low Cost, Low Power SRIO-Capable FPGAs

As mentioned above, much of the processing falls to DSPs and NPUs, but typically each of these has a different job to do. DSP applications, although processing intensive, tend to be more interrupt driven (e.g. doorbells) since they are implemented within a processing farm or are interfacing to an SRIO switch or endpoint -- perhaps even providing a bridging mechanism from SRIO to another SERDES-based protocol such as GbE or PCIe. NPUs, on the other hand, play more of a policing role, handling processing but primarily responsible for traffic shaping and queuing. Figure 3 shows examples of how a low cost, low power FPGA can assist in achieving a successful and efficient system solution.

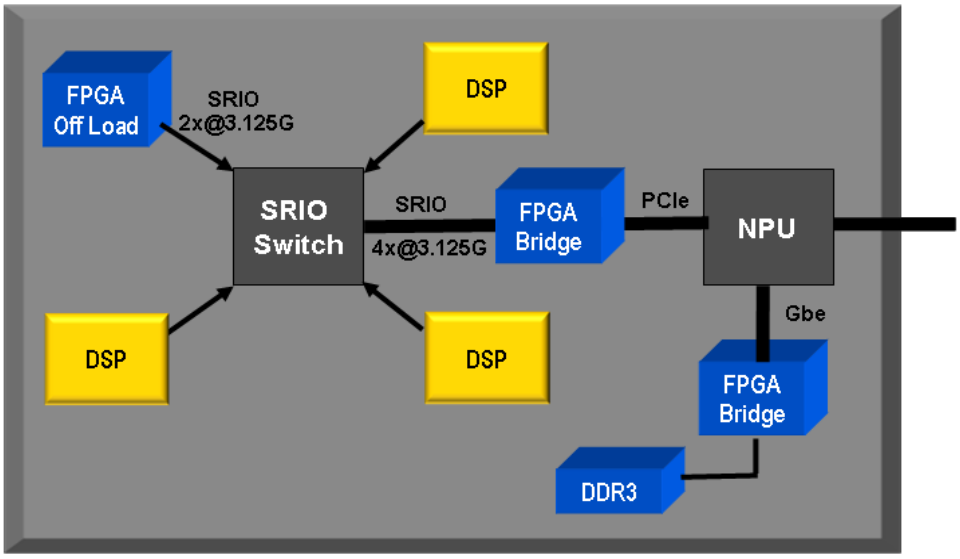

Figure 3 - Examples of FPGA Applications

The inherent flexibility and time-to-market advantages afforded by FPGAs over ASICs have long been appreciated, but until recently these advantages were available only by utilizing premium, high end devices, which compromised cost and power budgets. Under now, low cost, low power FPGAs were limited to “glue logic” and “bug fix” applications. Today, however, that is no longer the case, as the FPGA value proposition has broadened significantly. In order to support processing needs and maintain tight cost and power budgets, FPGA architectures have undergone evolutionary changes, significantly increasing their performance, features and logic densities, and doing so at a lower power and price point than traditional FPGAs. Enhanced features such as integrated SERDES, high speed embedded DSP blocks, DDR3 memory support and embedded memory capabilities are available and have become key components in processing designs. System engineers and design engineers are now able to utilize these programmable platforms for complex signal path applications implementing functions supporting RRH and baseband processing, as well as wireline and image processing applications, at reduced power and lower cost compared to traditional, high end SERDES-capable FPGAs.

Summary

System designers will continue to be under pressure to produce higher performance systems yet maintain lower build and operational costs. FPGAs have historically played key roles in system designs, but are now pushing forward to new levels of performance while assisting in lowering overall system build and operational costs. Feature rich, low cost FPGAs like the LatticeECP3 enable fast time-to-market and time-to-revenue, and the flexibility and performance to accommodate evolving standards. Systems/design engineers are now equipped with an exciting, improved toolset to overcome the challenges of an ever-evolving signal processing marketplace.

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