MANAGING IMAGE DATA IN AUTOMOTIVE INFOTAINMENT APPLICATIONS USING LOW COST PLDS

A Lattice Semiconductor White Paper

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Introduction

Infotainment systems help drivers navigate safely to their destination while entertaining passengers, and are no longer limited to high end vehicles: emerging driver assistance automotive systems are now making their way into the mainstream market. The front LCD displays need to dynamically switch from the GPS display to one of many camera views, or even a combination of images captured by several cameras housed around the vehicle. The image from the rear cameras assists in parallel parking, getting out of parking spaces and driveways safely, and avoiding collisions with oncoming vehicles. To extend driver visibility into cross traffic at busy intersections with limited visibility, the front camera views (two cameras placed on the vehicle body above the front tires) can be displayed. Some vehicles have the capability to provide an "around view image," which is basically a virtual 360 degree view around the vehicle coming from images captured by the front (tip of the hood), rear and two side cameras (by the side mirrors). These images may need to be scaled (resized) for different LCD sizes, adjusted and enhanced to improve the image quality.

New IC solutions are needed to manage the image data. ASICs have become prohibitively expensive and risky, and ASSPs are too inflexible. Programmable Logic Devices (PLDs) overcome these shortcomings, but pose the challenges of the interfaces used for image data, which have often required the use of high performance and hence high cost PLDs. This is changing. A new generation of low cost PLDs that offer high performance IO buffers is now available. These low cost PLDs provide efficient transmission, processing, manipulation and display of digital data while enabling product differentiation and helping to achieve time to market and cost-effectiveness goals.

Transporting Image Data

Image data in vehicles is transmitted using a variety of methods. One common approach is to use LVDS to build source synchronous interfaces.

A prevalent technique for video applications is the 7:1 LVDS (Low Voltage Differential Signaling) interface. *Channel Link*, *Camera Link*, *FPD-Link* and *FlatLink* are variants of this approach. LVDS is a high speed, low power, general purpose interface standard. It uses differential signaling that generates equal and opposite currents in the pair, which also help to lower overall emissions. In addition, LVDS uses current-mode drivers, which limit power consumption. National Semiconductor developed the *Channel Link*, and *FPD-Link* (Flat Panel Display Link) technology, based on LVDS, as a solution for flat panel displays to support data transmission from graphics controller to LCD panel. The technology was then extended to a method for general purpose data transmission. *Camera Link* is a standard based on 7:1 LVDS and uses up to 28-bit data and a clock rate up to 85 MHz for a total throughput of 2.38 Gpbs. Texas Instruments' *FlatLink* is offered in 21:3 or 28:4 configurations, with 4-bit, 6-bit, or 8-bit RGB supported.

Challenges Implementing 7:1 LVDS in Low Cost PLDs

The 7:1 LVDS interface typically uses three to five LVDS data lanes and one LVDS clock lane. Higher resolution displays would use four or five LVDS data lanes. In one clock period or cycle, there are 7 serial bits on each data lane, as illustrated in Figure 1.
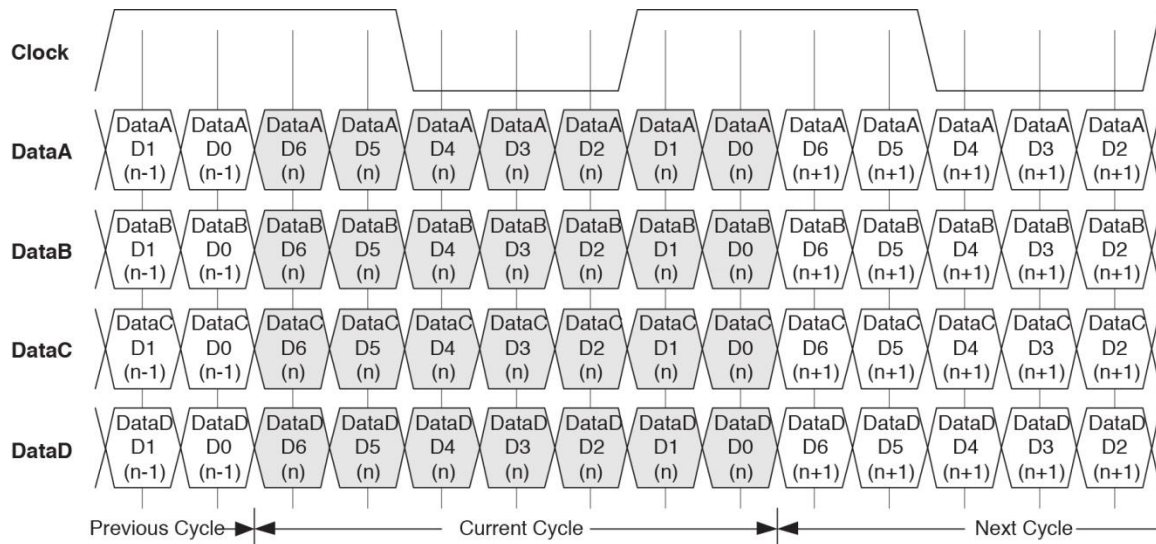
Figure 1- Timing of the 7:1 LVDS Interface

The challenges in implementing the 7:1 LVDS interface in a low cost PLD include the availability of high speed LVDS buffers and PLL for generating the de-serialization clock, the ability to capture the input data, efficient, accurate gearing and data formatting.

High Speed LVDS Buffers: The data and clock have to be received or transmitted to or from the PLD at relatively high speed. The exact speed depends on the resolution, frame rate and color depth used by the display. For example, 800x600 to 1024x768 displays require LVDS data to be transmitted from 40 MHz to 78.5 MHz for 60 Hz to 75 Hz refresh rates. This translates to LVDS data rates of 280 Mbps to 549 Mbps. Higher resolution displays, such as the 1280x1024 60 Hz, require data to be transmitted with a 108 MHz clock. For these systems, the data will transmit at 756 Mbps.

Clock Generation: The general approach is to receive the incoming clock and use a PLL to multiply it by 7 times to clock each bit of data. In reality, this is quite difficult because the clock has to run extremely fast. Since a typical display interface clock rate is 60-100 MHz or higher, multiplying this by 7 yields a frequency of 420-700 MHz. At these clock rates, any image manipulation and processing would be impossible in a low cost PLD.

Data Capture, Gearing and Formatting: The registers that follow the LVDS input buffer must accurately capture the data. Tight control of the clock and data relationship is important to capture the incoming high speed data stream. It is also necessary to gear (reduce) the speed of the data before it is passed on to the PLD fabric. If the input capture circuitry operates on only one edge of the clock, seven phase-shifted versions of the low speed clock should be generated and used to capture the input data with seven different registers. The challenges of clock generation and distribution discourage this approach for a PLD implementation. The clock must have relatively low jitter, since its jitter must be accounted for in the overall timing budget. Similarly, the skew of the clock distribution network used to provide this clock to input or output registers must be accounted for in any timing analysis.

Implementation Example of 7:1 LVDS in MachXO2 Device

The MachXO2 PLD has been architected with specific features to support the 7:1 LVDS interface. These features include high performance LVDS I/O buffers, double data rate (DDR) I/O registers, gearing logic and high precision PLL with dedicated 3.5 clock divider. These features and capabilities provide a complete solution. MachXO2 devices provide up to 21 data channels. Figure 2 shows the *receiver* and *transmitte*r for four data channels.
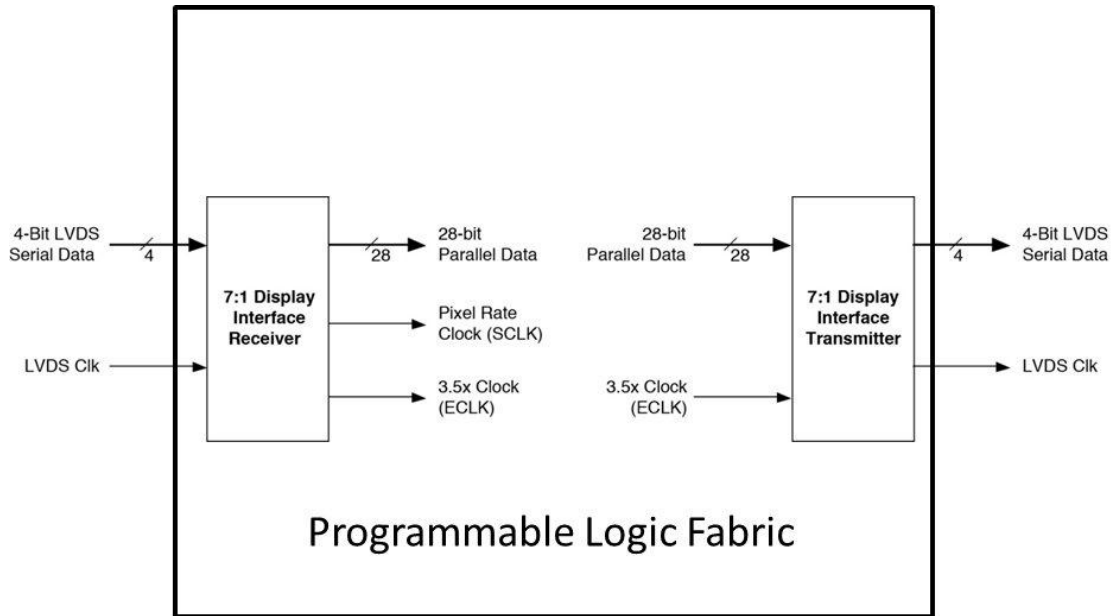
Figure 2- Receiver and Transmitter in MachXO2

In Figure 2*,* the *receiver module* of the MachXO2 device receives four data channels, and the clock through the LVDS I/O buffers. These buffers operate up to 303 MHz (606 Mbps), supporting high resolution and display refresh rates with up to an 85 MHz pixel rate (SXGA). The PLL is used to multiply the clock by 3.5. This faster phase-shifted clock (ECLK) is then distributed via a low skew edge clock net to the DDR capture registers. The LVDS data is fed to the DDR registers with 7:1 gearing function. The gearing allows demuxing of the I/O data clocked with the high speed edge clock (ECLK) to the slower speed FPGA clock rate (SCLK).

This 7:1 LVDS solution includes logic for auto-aligning the PLL output clock to the optimum position for sampling the input LVDS data stream, plus logic for auto-aligning the PLDs clock to the input data word, These 'soft' logic pieces work in concert with the 'hard' primitive resources to provide the full Display Interface solution.

The transmitter module of the MachXO2 PLD receives 28 bits of parallel data and the fast DDR clock (ECLK). The parallel data is fed to the Display I/O Logic Cell with 7:1 gearing function. The gearing allows the multiplexing of the input data clocked in with the low speed system clock (SCLK) to the higher speed DDR output edge clock rate (ECLK).

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Summary

Increasing digital content in the form of numerous image sources (several cameras), rear seat displays and navigation systems is making its way into the mainstream market.

7:1 LVDS interfaces are expected to remain popular in imaging applications such as vehicle infotainment, due to cost and power advantages.

The MachXO2 devices can be deployed in the driver assistance automotive systems to manage the display and manipulation (scale, rotate, etc.) of the images from the cameras. The MachXO2 devices can dynamically switch between displaying the image from one camera to the other, or as a combination of the two.

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