Scalable Low-Voltage Signaling with LatticeSC/M Devices

July 2011 Application Note AN8085

Introduction

Differential signaling has become increasingly popular in network and telecommunications markets for a number of reasons. It offers many advantages including reduced noise, faster circuit speed, and reduced power consumption. The following overview of some mature signaling schemes such as LVDS and RSDS is necessary to clearly understand the evolutionary benefits of Scalable Low-Voltage Signalling (SLVS).

In traditional LVDS systems, a differential transmitter injects a small 3.5 mA current into one trace or the other, depending on the logic level to be sent. The current passes through a 100-ohm resistor at the receiving end and then returns in the opposite sdirection along the other trace of the differential pair. The voltage difference across the resistor is therefore about 350 mV (700 mV p-p). The receiver senses the polarity of this voltage to determine the logic level.

The small amplitude of the signal reduces the effects of capacitance and inductance, and reduces the amount of radiated electromagnetic noise. LVDS channels have a low susceptibility to noise because distant noise sources tend to add the same amount of voltage (called common-mode noise) to both lines, so the difference between the voltages remains the same. The low common-mode voltage is the average of the voltages on the two traces of about 1.25V. The common mode is set by the transmitter as an off-set voltage from ground. The 350 mV differential voltage causes the LVDS to consume static power in the LVDS load resistor based on the 1.25V off-set and 350mV differential voltage swing.

Scalable Low-Voltage Signaling (SLVS) is based on a point-to-point signaling method defined in the JEDEC JESD8-13 (SLVS-400) standard. This standard evolved from the traditional LVDS standard and relies on the advantage of its use of smaller voltage swings and a lower common-mode voltage. The 200 mV (400 mV p-p) SLVS swing contributes to a reduction in power and is commonly used with RSDS (Reduced-Swing Differential Signaling) standards. The RSDS standard only reduces the swing from 350 mV to 200 mV with the same 1.25V common-mode offset of LVDS standards, however a lower common mode differentiates SLVS. The common-mode is set very low (200 mV nominal) providing a considerable decrease in quiescent power. The combination of smaller signal swing and low common mode produces much lower power utilization.

LatticeSC/M Solution

The LatticeSC™ and LatticeSCM™ FPGA devices utilize both built-in and board resources required to build an SLVS interface to industry standard devices. The flexibility and speed of the I/O provides easy implementation of SLVS conforming buses with up to 1Gbps performance.

The LatticeSC/M inputs can receive up to 2 Gbps data streams in traditional LVDS systems. The LVDS input specifications of the LatticeSC/M are shown in Table 1. The features of the LVDS inputs conform to the signaling requirements to directly connect to SLVS transmitters.

Table 1. LatticeSC/M Input to SLVS Output Conformance Specifications

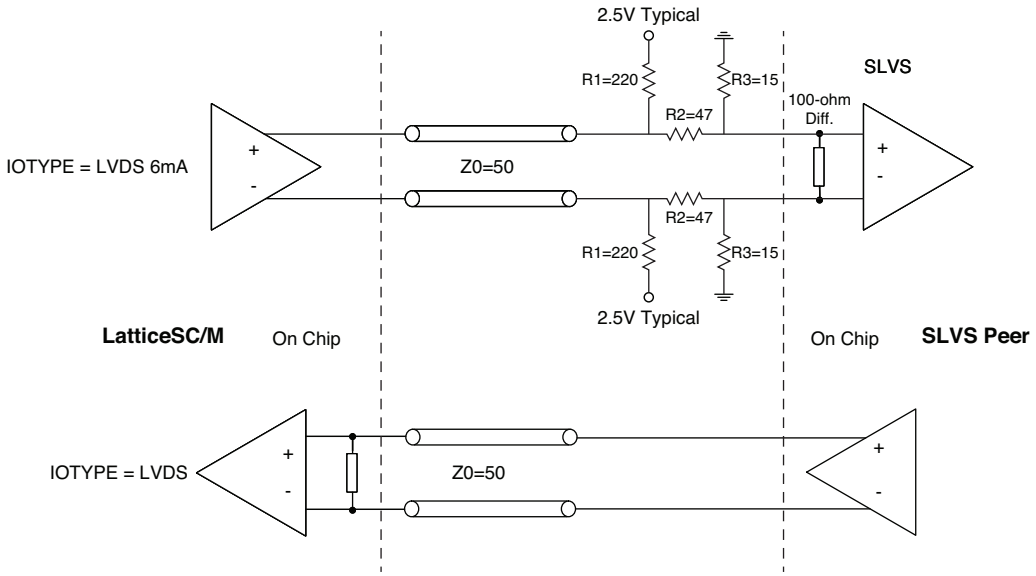
Characteristic	LatticeSC/M LVDS Input	SLVS Output	Units
VCM (min.)	50	150	mV
VCM (max.)	2350	250	mV
Differential Voltage (min.)	100	140	mV
Differential Voltage (max.)	2400	270	mV

SLVS, like LVDS, requires a load termination at the receiver but does not specify that the termination is internal or external to the receiver. The LatticeSC/M device has built-in differential termination with selectable values of OFF,

120, 150, 220, 420. The internal differential terminations are available for inputs on all sides of the device. See the LatticeSC/M Family Data Sheet for additional information about on-die termination. The built-in terminations provide cleaner board interconnections and robust system performance.

The output driver of the LatticeSC/M LVDS uses a combination of external resistors to emulate the SLVS requirements. Differential drive current is pin-by-pin programmable to 3.5 mA, 2 mA, 4 mA, and 6 mA. The 6 mA DIFF-CURRENT setting closely matches the current drive requirements for the SLVS interface. Using the LVDS output driver and 6mA option, the LatticeSC/M utilizes the on-board resistor network to adjust the swing and common-mode required by the SLVS receiver. See Figure 1.

Figure 1. LatticeSC/M SLVS Interface



As shown in Table 2, the LatticeSC/M output emulation resistor structure provides signaling levels which meet the SLVS specifications.

Table 2. LatticeSC/M Output to SLVS Input Specification Conformance

Characteristic	LatticeSC/M LVDS Output Without External Terminations	LatticeSC/M LVDS Output With External Terminations	SLVS Input	Units
VCM (min.)	1120	150	70	mV
VCM (max.)	1375	280	330	mV
Differential Voltage (min.)	250	180	140	mV
Differential Voltage (max.)	450	280	450	mV

The HSPICE simulation shown in Figures 2 through 5 was used to verify the interface levels and performance of the solutions. Lattice provides HSPICE models of the LVDS buffers. The simulation results below show worst-case conditions of the Lattice SLVS interface solution.

Figure 2. HSPICE Simulation Topology

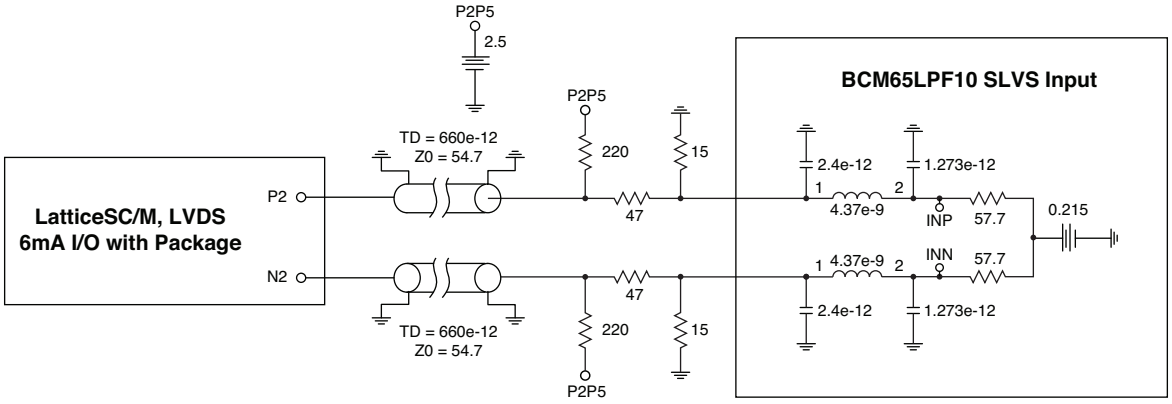


Figure 3. Typical HSPICE Simulation Waveform

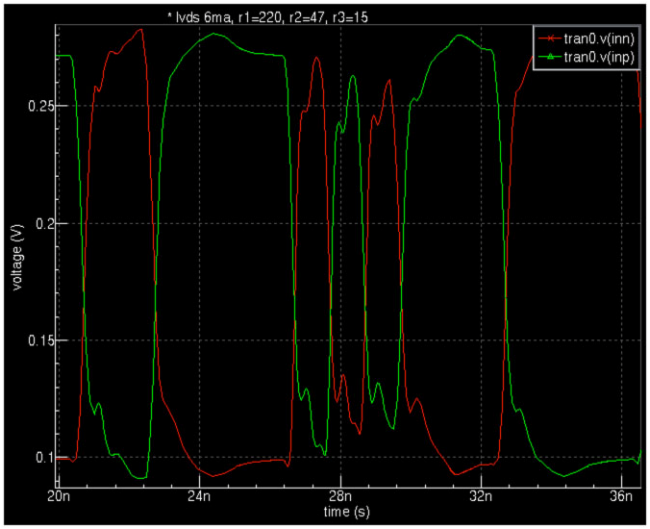


Figure 4. Slow HSPICE Simulation Waveform

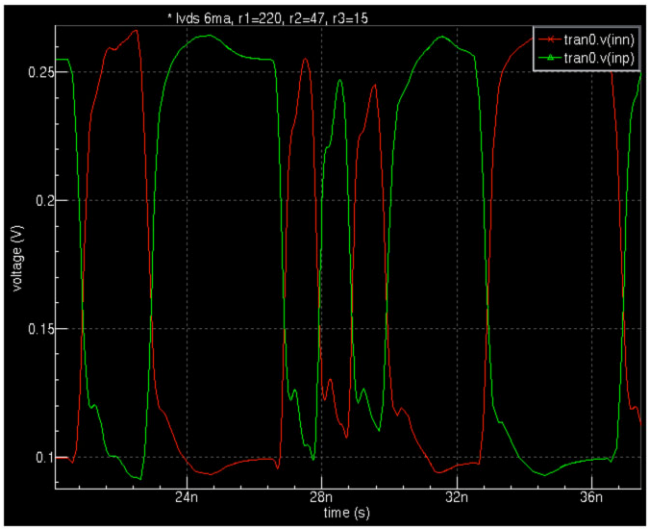
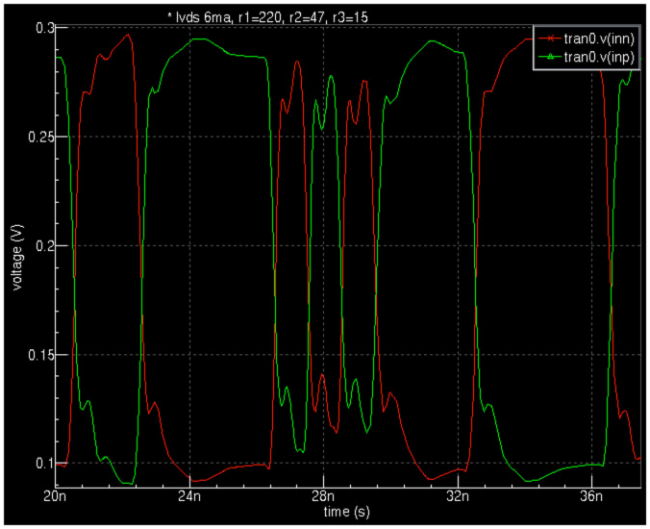


Figure 5. Fast HSPICE Simulation Waveform



The data in Table 3 and Figures 6 through 9 represents output measurements taken on a device using the terminations as mentioned above. The actual common-mode and voltage swings were measured with a 500 MHz signal while varying the power supplies (+/- 5%) and temperature.

Table 3. Hardware Measured Results

Test Conditions	Single-Ended VCM	P-P Differential Swing	Units
Low Voltage/85°C	165	210	mV
Nominal Voltage/Room Temperature	188	235	mV
High Voltage/0°C	206	260	mV
High Voltage /-40°C	223	266	mV

Figure 6. Low Voltage at 85°C

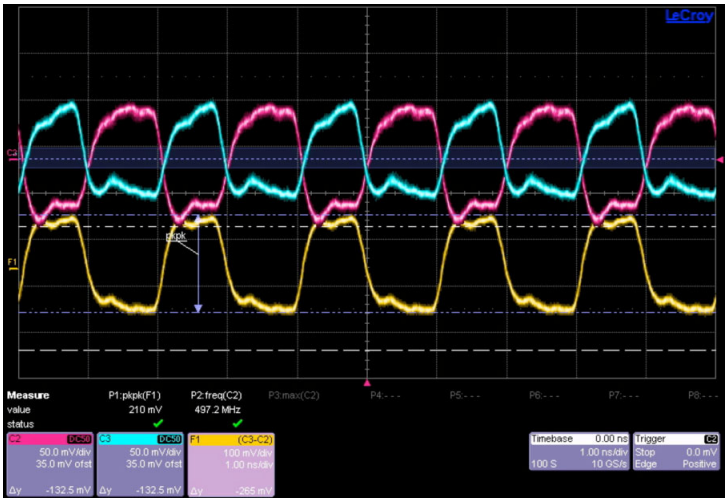


Figure 7. Nominal Voltage at Room Temperature

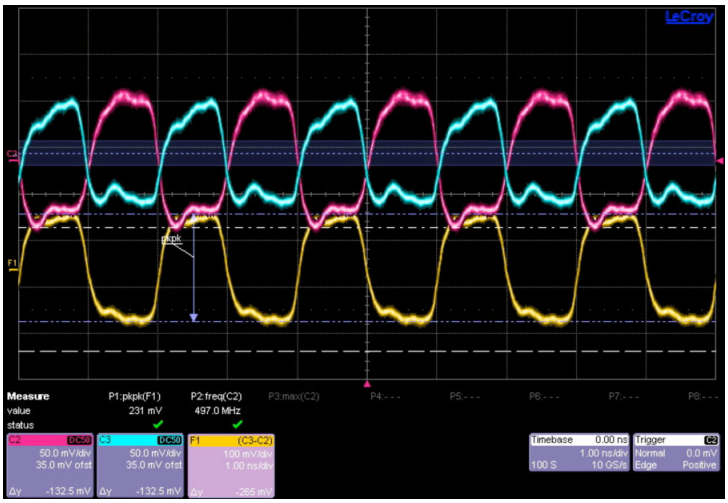


Figure 8. High Voltage at 0°C

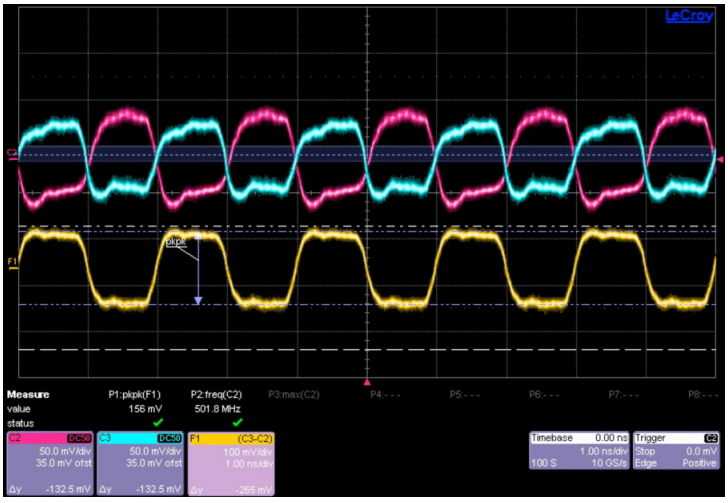
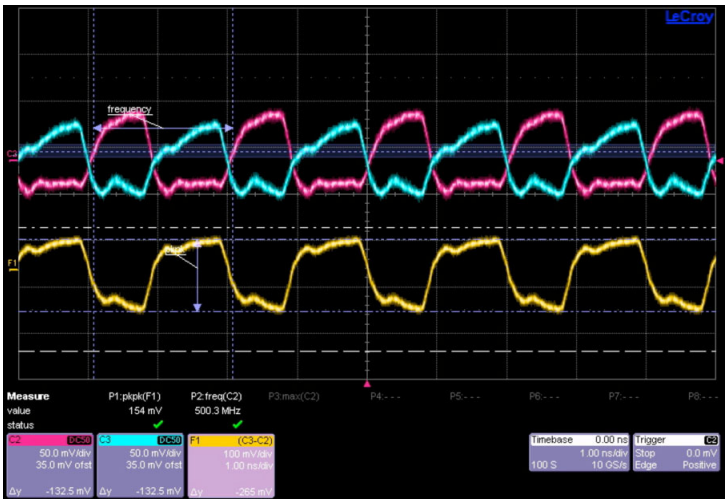


Figure 9. High Voltage at -40°C



Conclusion

This technical note is based on the following LatticeSC/M SLVS design considerations:

1. Differential inputs in any bank
2. Use of built-in differential terminations.
3. Differential outputs permitted on True-LVDS output pairs as noted in LatticeSC/M Family Data Sheet.
4. External termination resistors required on output signals to emulate the proper SLVS levels.

The LatticeSC/M SLVS solution works well in DC-balanced and unbalanced situations up to 500 MHz. The wide input common-mode range and embedded termination resistor performs well in a SLVS interface and provides a seamless connection between devices. The flexibility of the LatticeSC/M LVDS outputs allows a robust interconnection with SLVS devices. Through design analysis and hardware validation, the LatticeSC/M solution is a proven interface to SLVS devices.

Technical Support Assistance

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Revision History

Date	Version	Change Summary
July 2011	01.0	Initial release.