LatticeECP3: First PCIe 2.0 Compliant Low Cost FPGA

LatticeECP3 PCIe IP Core Solution Enables Lowest Cost, Lowest Power Single-Chip Programmable PCIe 2.0 Endpoint

LatticeECP3™ is the first and only PCI Express 2.0 compliant low-cost FPGA. The PCI Express 2.0 specification allows operation at a lower speed than PCI Express 1.1 (2.5 Gbps), but the loop bandwidth characteristics are different and more rigorous. Now designers who need PCI Express 2.0 compliance, but do not need the PCI Express link to operate at 5 Gbps, can use the low-cost LatticeECP3 FPGA in PCI Express 2.0 compliant systems.

The PCI SIG PCI Express 2.0 Integrators List has been updated to include the LatticeECP3 x4 endpoint IP. As a subset of the x4 endpoint IP, the LatticeECP3 x1 endpoint IP is also qualified.
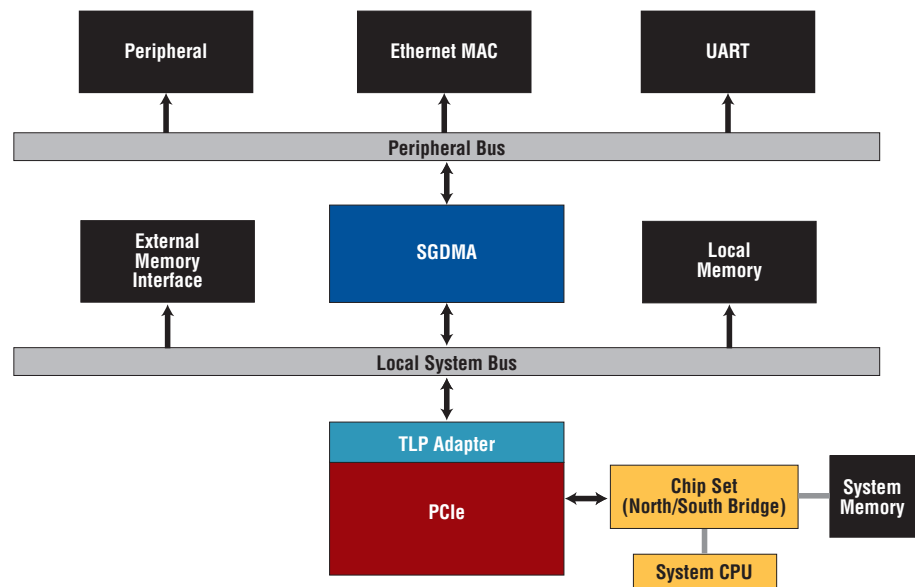
The LatticeECP3 FPGA features:

- **Low-cost digital SERDES**
  - Compliant to PCI Express 2.0 (at 2.5 Gbps) electrical specifications
- **Up to 16 channels per device**
  - Useful for multi-protocol bridging
- **Complete end-to-end solution**
  - PIPE-compliant PCS
  - PCI Express x1 and x4 soft IP available
- **Very low power (110 mW per channel typical at 3.2 Gbps)**
- **Low-power, high-value FPGA fabric**
  - High-end features at low cost

Trellisys IP
Lattice has partnered with Trellisys, Ltd. to provide the PCI Express Bus Functional Model (BFM) verification IP at no additional cost. The Trellisys PCI Express BFM:

- **Supports Both Verilog and VHDL**
  - Verified on both the Aldec Active-HDL and Riviera-PRO simulators
  - Delivered as pre-compiled code in the PCI Express IP core installer through the IPexpress flow within Lattice Diamond® 1.2 (or later versions)

Example PCI Express Endpoint System Using Lattice IP

IP Suites for LatticeECP3

Lattice IP Suites are economical packages of multiple IP cores tailored to specific applications. These comprehensive solutions help designers quickly implement popular functions, such as high-speed data transfer, Ethernet networking, high-speed memory interfaces, signal processing, video pixel processing, and more.

The PCI Express IP Suite includes the PCI Express IP, as well as related IP cores like DDR3 and DMA controllers. This IP suite can be purchased for $99 for a limited time as part of a special promotion. The regular list price of the IP Suite will be $995 after the limited promotion.

LatticeECP3 PCI Express Evaluation Platforms

A number of hardware platforms are available to help designers evaluate and develop with the LatticeECP3 PCI Express solution. All platforms feature:

- Compliant to PCI Express 2.0 endpoint
- PCI SIG Compliance Workshop certified
- Soft Physical, Data Link and Transaction layers, and 4 KB data payload size
- Low LUT usage (5K LUTs) PCI Express x1 configuration
- Reference design to support TLP termination, interrupts, ingress/egress datapath and WISHBONE bus interface

The LatticeECP3 Versa Development Kit and LatticeECP3 PCI Express Development Kit combine application-specific evaluation boards, evaluation PCI Express IP, relevant reference designs and host software and drivers in one comprehensive package.

The LatticeECP3 Serial Protocol Board allows designers to quickly and seamlessly evaluate the Lattice PCI Express Solutions portfolio, and to use it as a basis for their own PCI Express development.

Platform	PCI Express Interfaces	Other Interfaces	Memory Interfaces
LatticeECP3 PCIe Development Kit	PCIe x1 & x4 Card Edge Finger	None	DDR2 Component (18-Bit)
LatticeECP3 Serial Protocol Board	PCIe x4 Card Edge Finger	SMAs for SERDES (4 Channels) SMAs for LVDS I/O RJ-45 Connector	DDR3 Component (8-Bit) DDR2 Component (18-Bit)
LatticeECP3 Versa Development Kit	PCIe x1 Card Edge Finger	SMA for SERDES (1 Channel) 2 RJ-45 Connectors	DDR3 Component (32-Bit)

Learn More

For more information about how the PCI Express 2.0 compliant LatticeECP3 FPGA can bring value to your design projects, visit the Lattice website or contact your local Lattice sales representative.